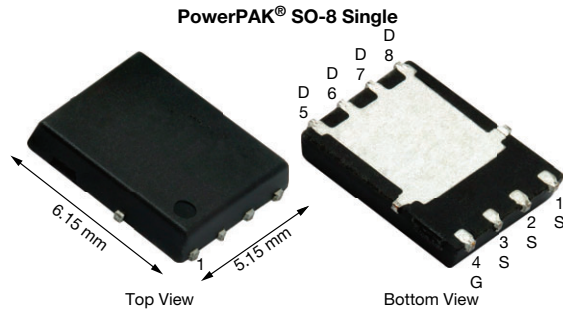


N-Channel 30 V (D-S) MOSFET With Schottky Diode



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0027
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0040
Q_g typ. (nC)	17.5
I_D (A) ^{a, g}	60
Configuration	Single

FEATURES

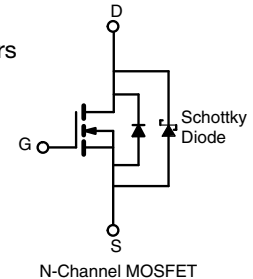
- TrenchFET[®] Gen IV power MOSFET
- SkyFET[®] with monolithic Schottky diode
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Personal computers and servers
- Synchronous buck
- Synchronous rectification
- DC/DC conversion



ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRC06DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20, -16	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	60 ^g
		$T_C = 70$ °C	60 ^g
		$T_A = 25$ °C	32 ^{b, c}
		$T_A = 70$ °C	25.6 ^{b, c}
Pulsed drain current ($t = 300$ μ s)	I_{DM}	100	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	7.1 ^{b, c}
Single pulse avalanche current	I_{AS}	15	mJ
Single pulse avalanche energy	E_{AS}	11.25	
Maximum power dissipation	P_D	$T_C = 25$ °C	50
		$T_C = 70$ °C	32
		$T_A = 25$ °C	5 ^{b, c}
		$T_A = 70$ °C	3.2 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.9	2.5	

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 70 °C/W
- Package limit



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30	-	-	V
Drain-source breakdown voltage (transient) ^c	$V_{DS(t)}$	$V_{GS} = 0\text{ V}$, $I_{D(aval)} = 15\text{ A}$, $t_{transient} \leq 50\text{ ns}$	36	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	-	2.1	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = +20, -16\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	-	0.02	0.20	mA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	-	0.13	1	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$	-	0.0022	0.0027	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	-	0.0032	0.0040	
Forward transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$	-	120	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	2455	-	pF
Output capacitance	C_{oss}		-	350	-	
Reverse transfer capacitance	C_{rss}		-	60	-	
C_{rss}/C_{iss} ratio			-	0.025	0.050	
Total gate charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$	-	38.5	58	nC
		$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 15\text{ A}$	-	17.5	27	
Gate-source charge	Q_{gs}		-	6.3	-	
Gate-drain charge	Q_{gd}		-	2.8	-	
Output charge	Q_{oss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$	-	29	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.4	1.15	2	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	12	24	ns
Rise time	t_r		-	14	28	
Turn-off delay time	$t_{d(off)}$		-	23	46	
Fall time	t_f		-	8	16	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	29	58	
Rise time	t_r		-	50	100	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	t_f		-	9	18	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	60	A
Pulse diode forward current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	100	
Body diode voltage	V_{SD}	$I_S = 5\text{ A}$	-	0.47	0.7	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	-	31	62	ns
Body diode reverse recovery charge	Q_{rr}		-	19	38	nC
Reverse recovery fall time	t_a		-	16	-	ns
Reverse recovery rise time	t_b		-	15	-	

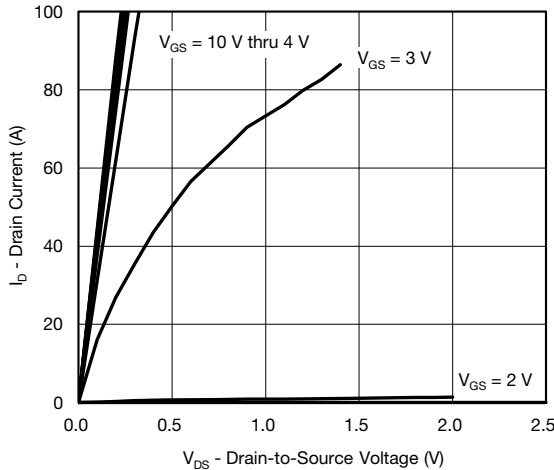
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. $T_{CASE} = 25\text{ }^\circ\text{C}$; Expected voltage stress during 100 % UIS test. Production data log is not available

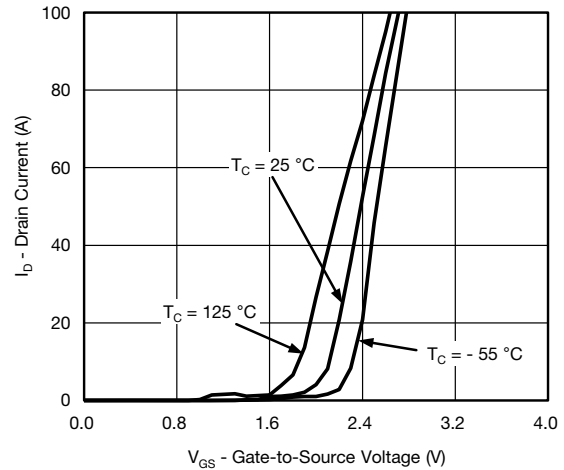
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



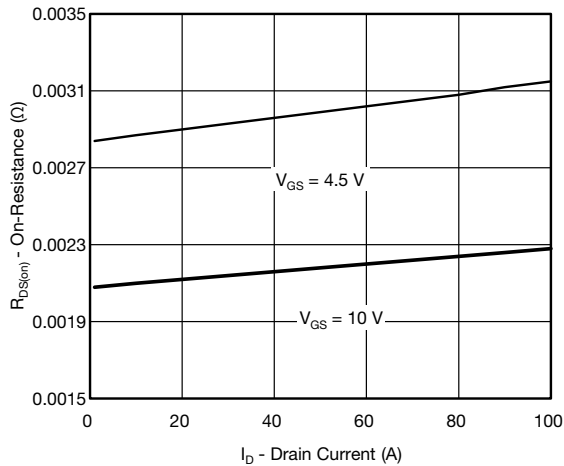
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



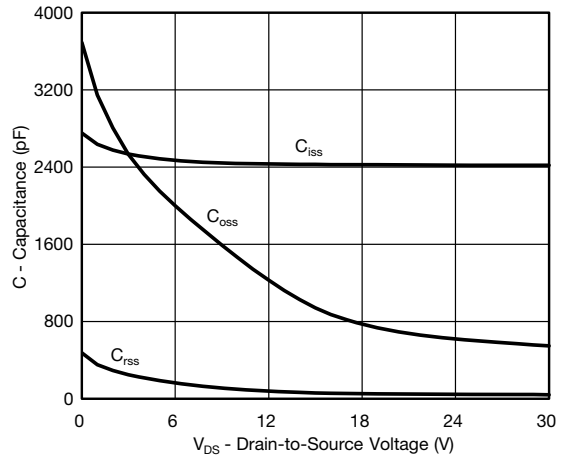
Output Characteristics



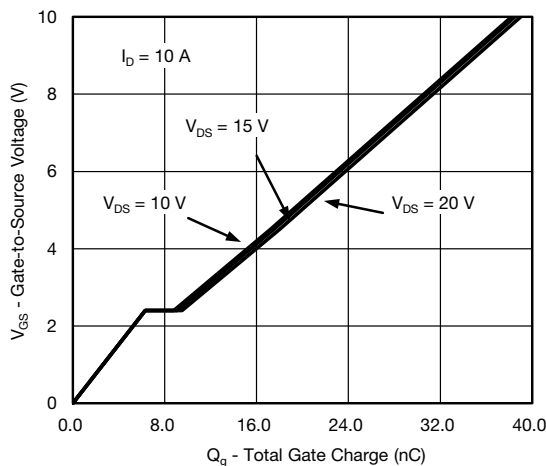
Transfer Characteristics



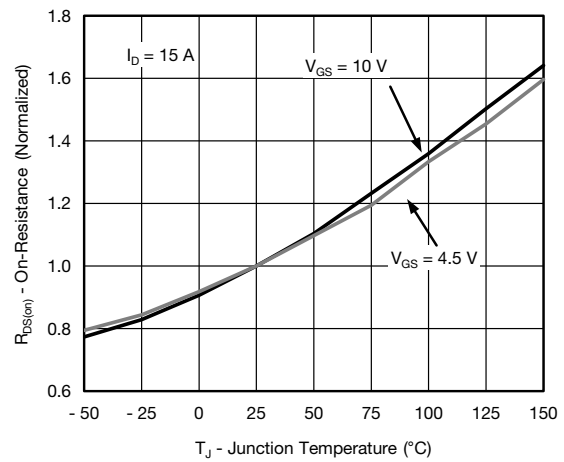
On-Resistance vs. Drain Current



Capacitance

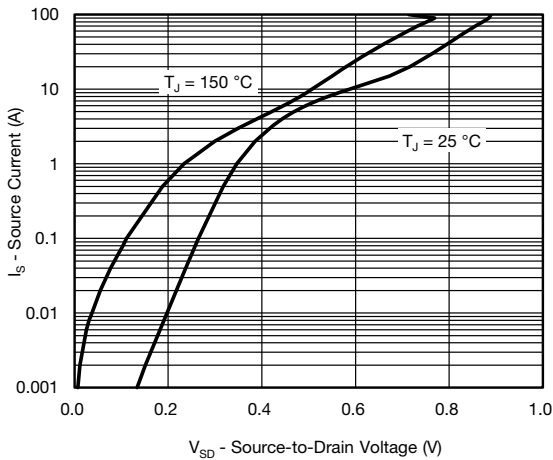


Gate Charge

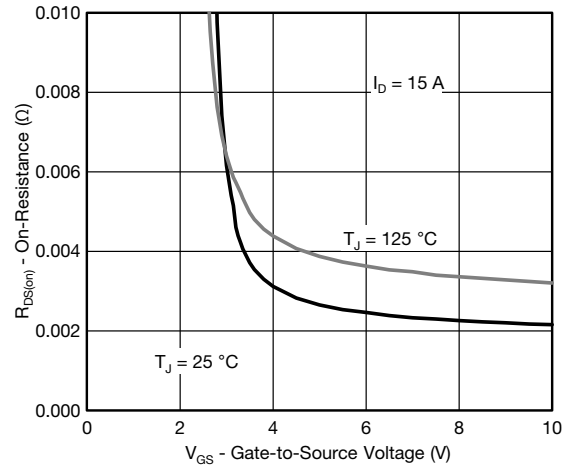


On-Resistance vs. Junction Temperature

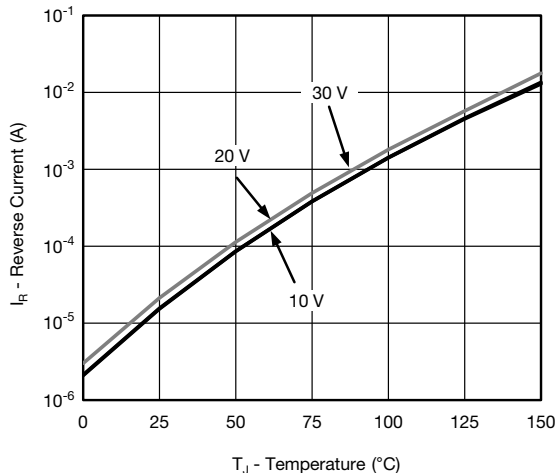
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



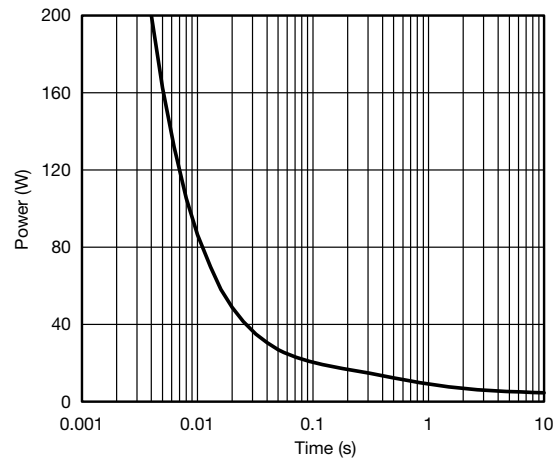
Source-Drain Diode Forward Voltage



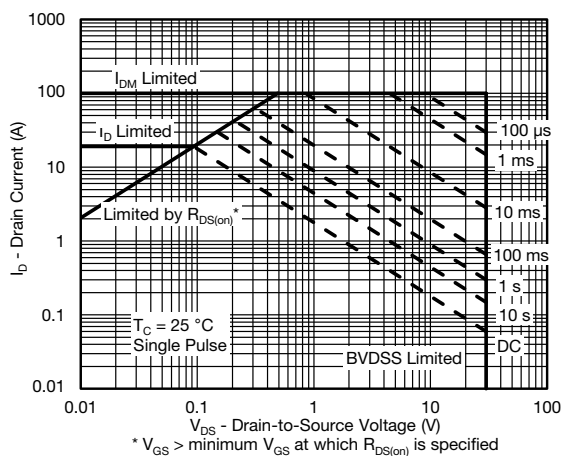
On-Resistance vs. Gate-to-Source Voltage



Reverse Current vs. Junction Temperature



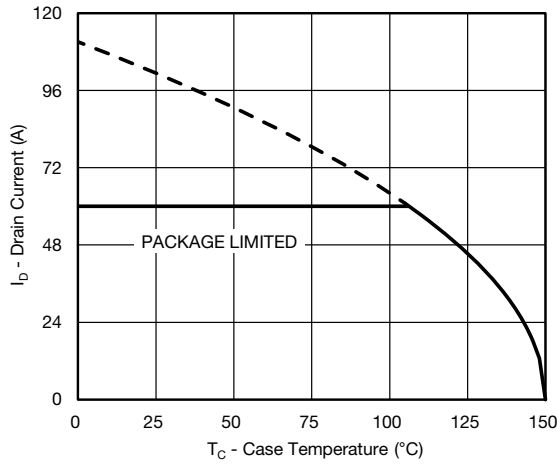
Single Pulse Power, Junction-to-Ambient



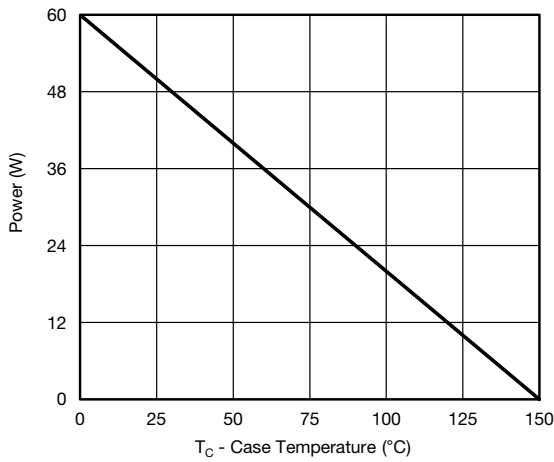
Safe Operating Area



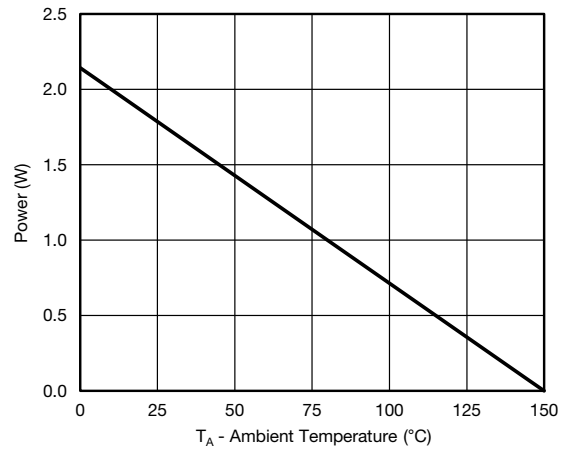
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating^a



Power, Junction-to-Case



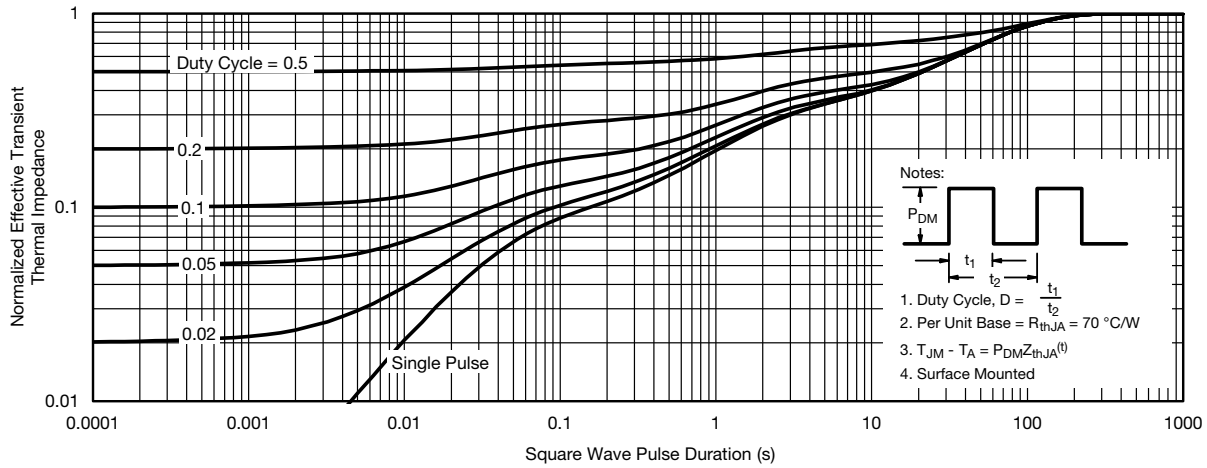
Power, Junction-to-Ambient

Note

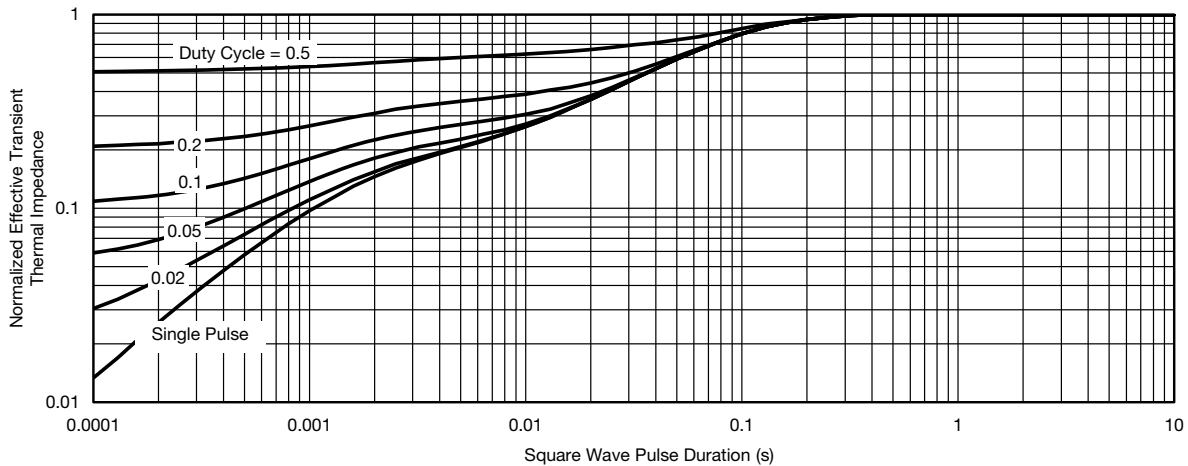
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62942.



PowerPAK[®] SO-8, (Single/Dual)



- Notes**
1. Inch will govern.
 2. Dimensions exclusive of mold gate burrs.
 3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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