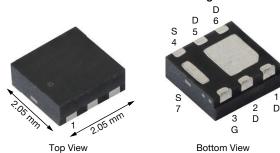
Vishay Siliconix

Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® SC-70W-6L Single



Marking Code: Q2XXXX

PRODUCT SUMMARY 100 $R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$ 0.099 $R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$ 0.079 9 Configuration Single

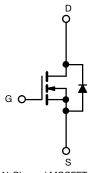
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- · Wettable flank terminals
- 100 % R_a and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





HALOGEN FREE



N-Channel	MOSFET

ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA700CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	V	
Gate-source voltage		V_{GS}	± 20	V	
Continuous drain current	T _C = 25 °C ^a	- I _D	9		
	T _C = 125 °C		5.2		
Continuous source current (diode conduction) ^a		I _S	9	А	
Pulsed drain current ^a		I _{DM}	24		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	7.3		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	2.66	mJ	
Maximum power dissipation	T _C = 25 °C	р	13.6	W	
	T _C = 125 °C	P _D	4.5] vv	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount c	R_{thJA}	90	°C/W	
Junction-to-case (drain)		R_{thJC}	11	C/ VV	

Notes

- a. Package limited
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
 c. When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable terminals. The end of the lead terminal is plated with tin
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



Vishay Siliconix

PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	.,	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V	
Gate-source leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
Zero gate voltage drain current		$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1		
	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	-	-	50	μΑ	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	-	-	250		
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	10	-	-	Α	
Drain-source on-state resistance a	, ,	V _{GS} = 10 V	I _D = 3 A	-	0.056	0.079		
	5	V _{GS} = 10 V	I _D = 3 A, T _J = 125 °C	-	-	0.077		
	R _{DS(on)}	V _{GS} = 10 V	I _D = 3 A, T _J = 175 °C	-	-	0.090	Ω	
		V _{GS} = 4.5 V	I _D = 3 A	-	0.070	0.099		
Forward transconductance b	9 _{fs}	V_{DS}	= 15 V, I _D = 3 A	-	9.0	-	S	
Dynamic ^b		•			•	I.		
Input capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	271	380	pF	
Output capacitance	C _{oss}	$V_{GS} = 0 V$		-	140	200		
Reverse transfer capacitance	C _{rss}			-	12	17		
Total gate charge c	Qg			-	6.2	9.5	nC	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 50 \text{ V}, I_{D} = 2 \text{ A}$	-	1.2	-		
Gate-drain charge ^c	Q _{gd}			-	1.3	-		
Gate resistance	R_g	f = 1 MHz		0.5	1.1	1.6	Ω	
Turn-on delay time c	t _{d(on)}		$V_{DD} = 50 \text{ V}, R_1 = 25 \Omega$		6.0	10	ns ns	
Rise time ^c	t _r	V _{DD} =			4	7		
Turn-off delay time c	t _{d(off)}	$I_D \cong 2 \text{ A, } V_{GEN} = 10 \text{ V, R}_g = 1 \Omega$		-	14	22		
Fall time ^c	t _f			-	5	8		
Source-Drain Diode Ratings and Charact	eristics ^b	1				L		
Pulsed current a	I _{SM}			-	-	24	Α	
Forward voltage	V _{SD}	I _F = 4.5 A, V _{GS} = 0 V		-	0.86	1.2	V	
Body diode reverse recovery time	t _{rr}			-	24	48	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 2 A, di/dt = 100 A/μs		-	20	40	nC	
Reverse recovery fall time	ta			-	15	-		
Reverse recovery rise time	t _b			-	9	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-1.5	-	Α	

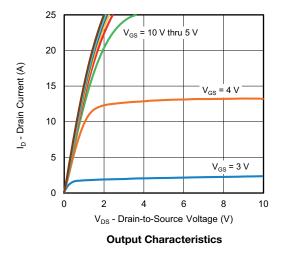
Notes

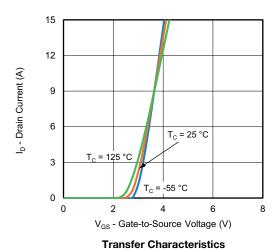
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

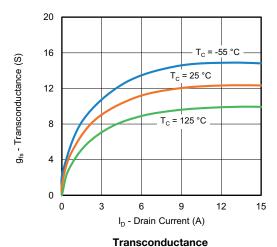
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

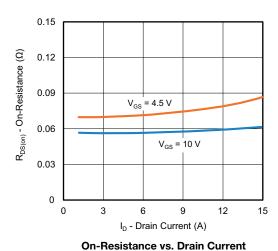


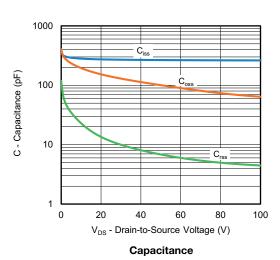
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

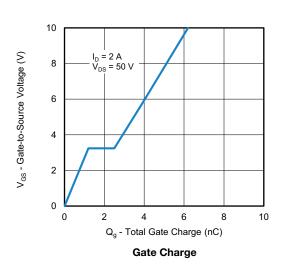






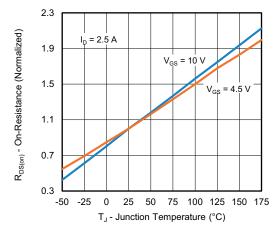




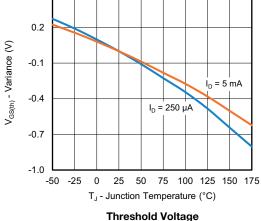




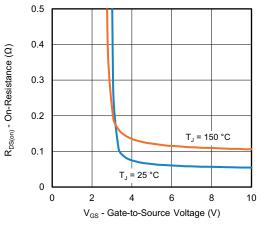
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



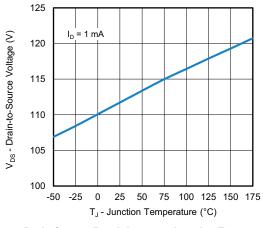
On-Resistance vs. Junction Temperature



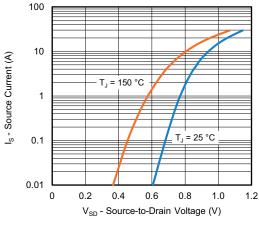
0.5



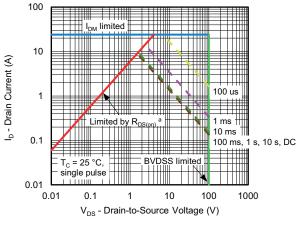
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



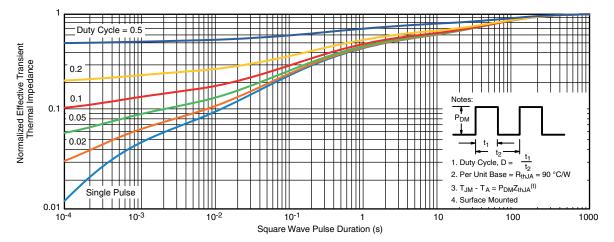
Source Drain Diode Forward Voltage



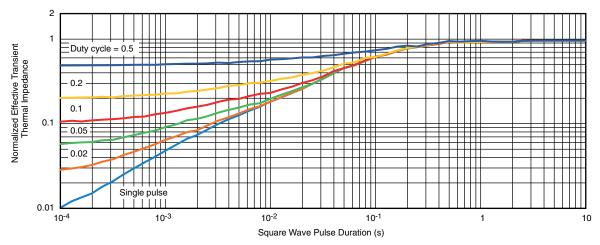
Safe Operating Area



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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