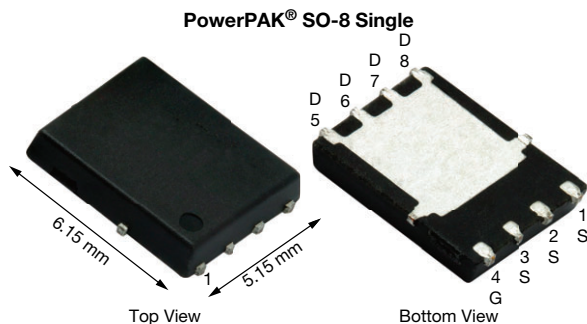


# N-Channel 150 V (D-S) MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	150
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0108
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 7.5$ V	0.0115
$Q_g$ typ. (nC)	27
$I_D$ (A)	59.7
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SIR572DP-T1-RE3
Alternate manufacturing location	SIR572DP-T1-BE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	150	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 150^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	59.7	A	
	$T_C = 70^\circ\text{C}$	47.8		
	$T_A = 25^\circ\text{C}$	14.8 <sup>b, c</sup>		
	$T_A = 70^\circ\text{C}$	11.8 <sup>b, c</sup>		
Pulsed drain current ( $t = 100\ \mu\text{s}$ )	$I_{DM}$	180		
Continuous source-drain diode current	$T_C = 25^\circ\text{C}$	84.1		
	$T_A = 25^\circ\text{C}$	5.1 <sup>b, c</sup>		
Single pulse avalanche current	$L = 0.1\ \text{mH}$	20		
Single pulse avalanche energy	$E_{AS}$	20	mJ	
Maximum power dissipation	$T_C = 25^\circ\text{C}$	92.5	W	
	$T_C = 70^\circ\text{C}$	59.2		
	$T_A = 25^\circ\text{C}$	5.7 <sup>b, c</sup>		
	$T_A = 70^\circ\text{C}$	3.6 <sup>b, c</sup>		
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150		
Soldering recommendations (peak temperature) <sup>c</sup>		260		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$t \leq 10\ \text{s}$	$R_{thJA}$	19	22	$^\circ\text{C/W}$
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.1	1.35	

## Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10\ \text{s}$
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 62.5  $^\circ\text{C/W}$
- $T_C = 25^\circ\text{C}$

## FEATURES

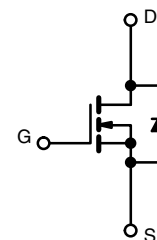
- TrenchFET<sup>®</sup> Gen V power MOSFET
- Very low  $R_{DS} \times Q_g$  figure-of-merit (FOM)
- Tuned for the lowest  $R_{DS} \times Q_{oss}$  FOM
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
FREE

## APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converters
- Power supplies
- Motor drive control



N-Channel MOSFET

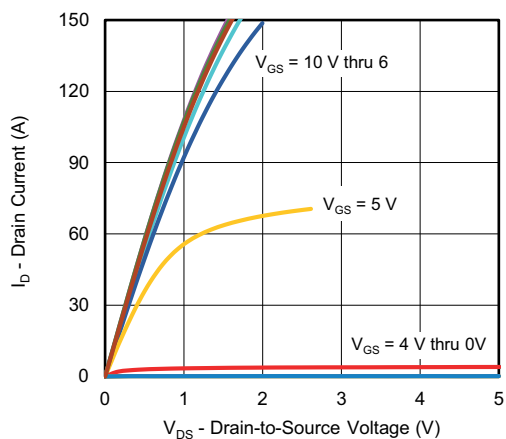
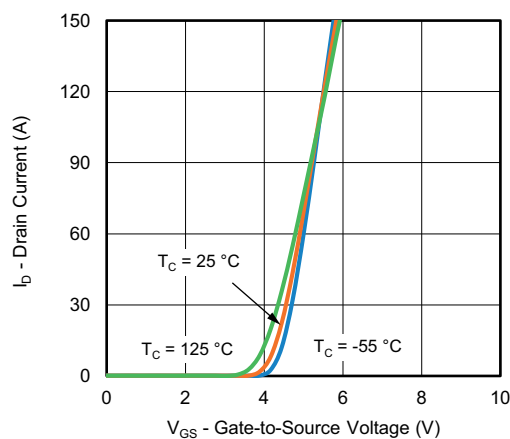
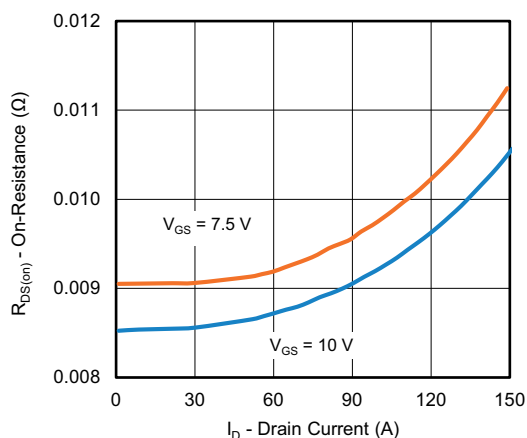
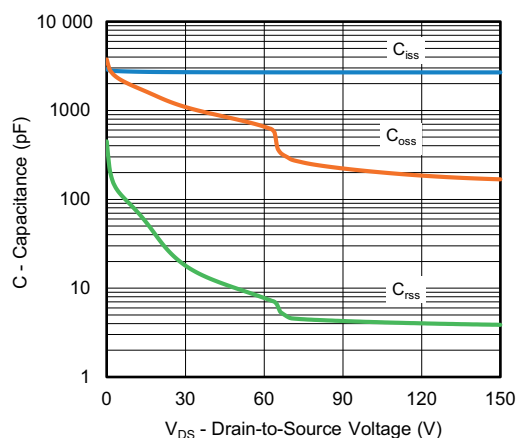
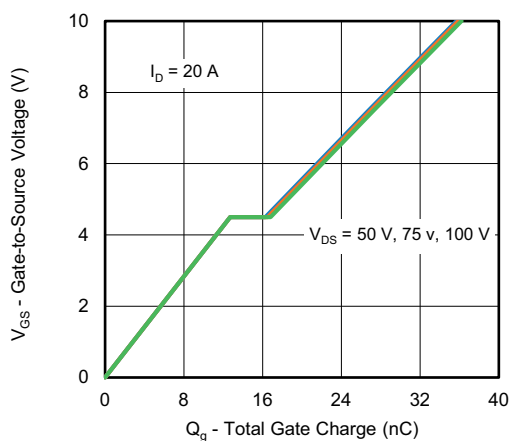
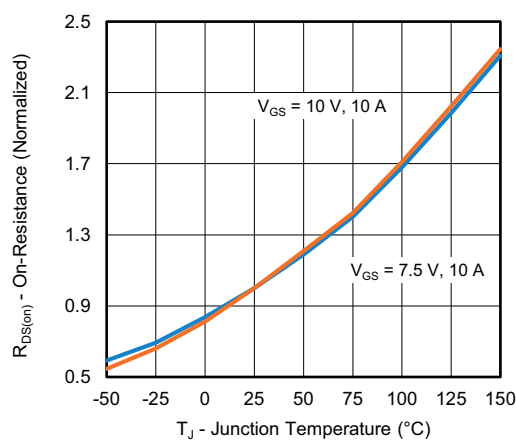


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	150	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 10 mA	-	112	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	-6.7	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	-	4	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> =10 V	40	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.0086	0.0108	Ω
		V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 10 A	-	0.0091	0.0115	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	-	50	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2733	-	pF
Output capacitance	C <sub>oss</sub>		-	250	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	4.5	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	35.9	54	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 10 A	-	27	41	
Gate-drain charge	Q <sub>gd</sub>		-	12.7	-	
Output charge	Q <sub>oss</sub>		-	3.8	-	
Gate resistance	R <sub>g</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V	-	84	-	Ω
Turn-on delay time	t <sub>d(on)</sub>	f = 1 MHz	0.4	1.05	1.8	
Rise time	t <sub>r</sub>	V <sub>DD</sub> = 75 V, R <sub>L</sub> = 7.5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	17	34	
Turn-off delay time	t <sub>d(off)</sub>		-	20	40	
Fall time	t <sub>f</sub>		-	30	60	
Turn-on delay time	t <sub>d(on)</sub>		-	15	30	
Rise time	t <sub>r</sub>	V <sub>DD</sub> = 75 V, R <sub>L</sub> = 7.5 Ω, I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 7.5 V, R <sub>g</sub> = 1 Ω	-	21	42	
Turn-off delay time	t <sub>d(off)</sub>		-	62	124	
Fall time	t <sub>f</sub>		-	29	58	
Fall time	t <sub>f</sub>		-	15	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	84.1	A
Pulse diode forward current	I <sub>SM</sub>		-	-	180	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	-	0.76	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	73	146	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	154	308	nC
Reverse recovery fall time	t <sub>a</sub>		-	56	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	17	-	

**Notes**

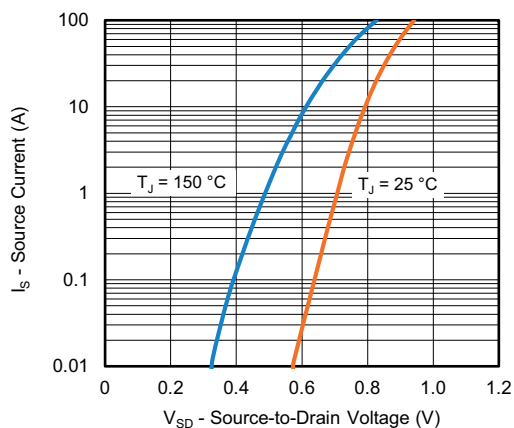
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

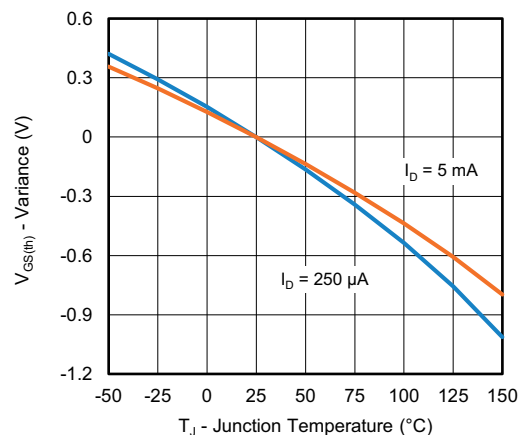
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**



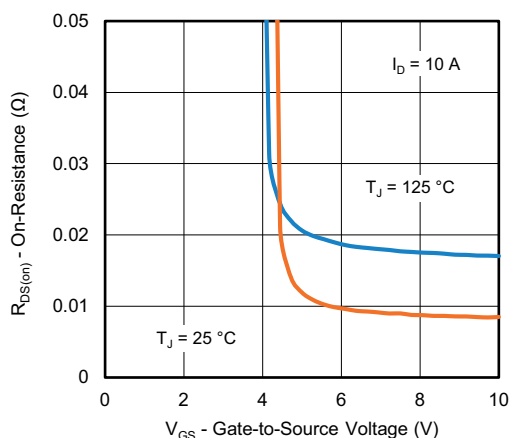
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



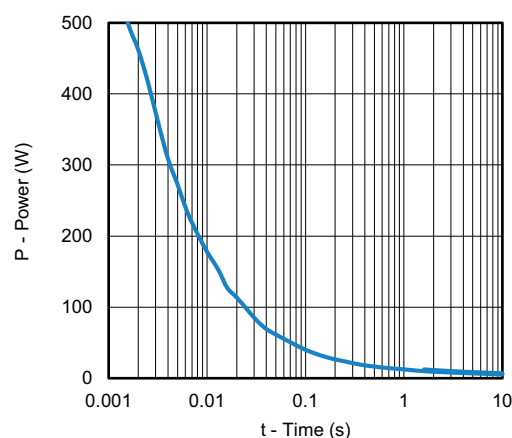
**Source-Drain Diode Forward Voltage**



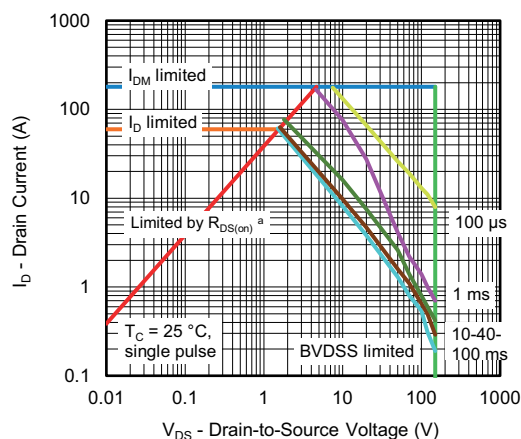
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



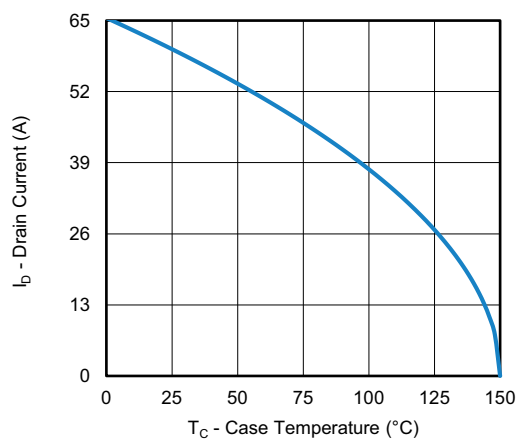
**Safe Operating Area, Junction-to-Case**

**Note**

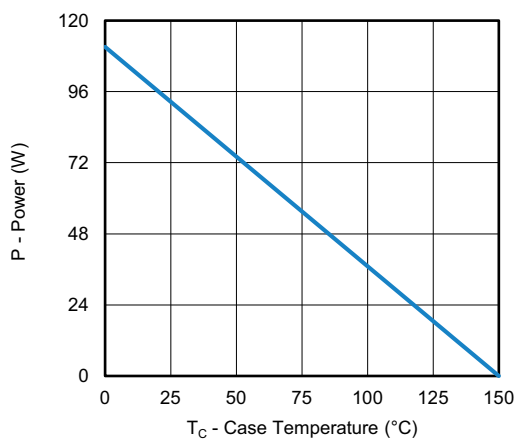
- a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



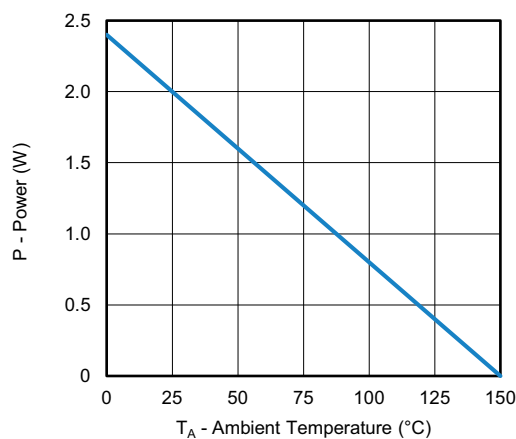
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



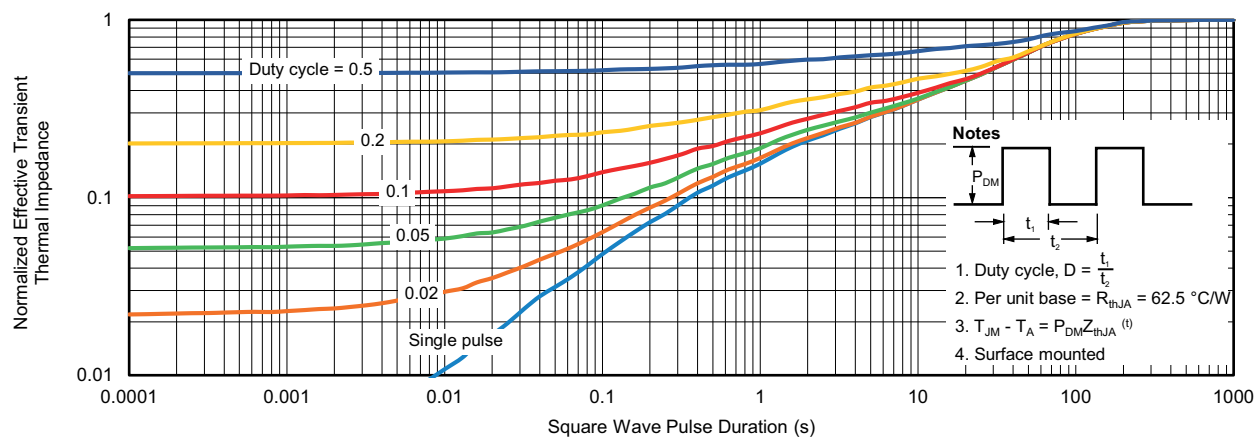
**Power, Junction-to-Ambient**

**Note**

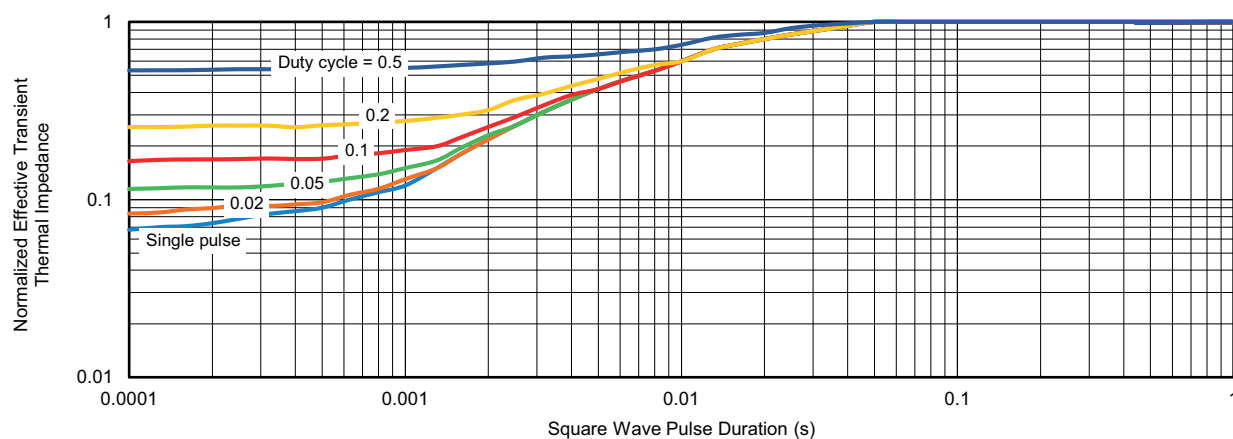
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63033](http://www.vishay.com/ppg?63033).

## PowerPAK® SO-8, (Single/Dual)



### Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17						
DWG: 5881						

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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