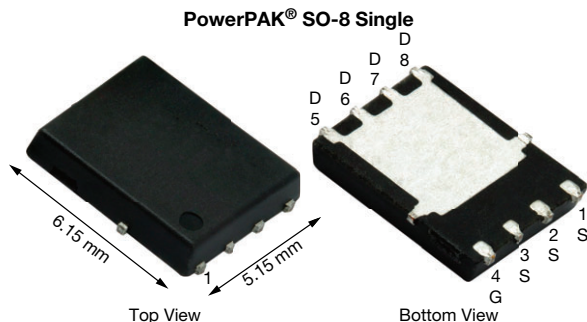


N-Channel 100 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0041
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0056
Q_g typ. (nC)	25.1
I_D (A)	110
Configuration	Single

FEATURES

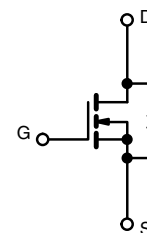
- TrenchFET® Gen V power MOSFET
- Ultra-low $R_{DS} \times Q_g$ FOM product
- Optimized Q_{gd}/Q_{gs} ratio
- Excellent efficiency performance in power supplies
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Primary side switch
- OR-ing and hot swap switch
- Motor drive control
- Battery management



N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SIR5102DP-T1-RE3
Alternate manufacturing location	SIR5102DP-T1-BE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	110
		$T_C = 70$ °C	88
		$T_A = 25$ °C	27 ^{b, c}
		$T_A = 70$ °C	21.5 ^{b, c}
Pulsed drain current ($t = 100$ μ s)	I_{DM}	300	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	94
		$T_A = 25$ °C	5.6 ^{b, c}
Single pulse avalanche current	I_{AS}	45	
Single pulse avalanche energy	E_{AS}	101	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	104
		$T_C = 70$ °C	66.6
		$T_A = 25$ °C	6.25 ^{b, c}
		$T_A = 70$ °C	4 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	15	20	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.9	1.2	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- $T_C = 25$ °C

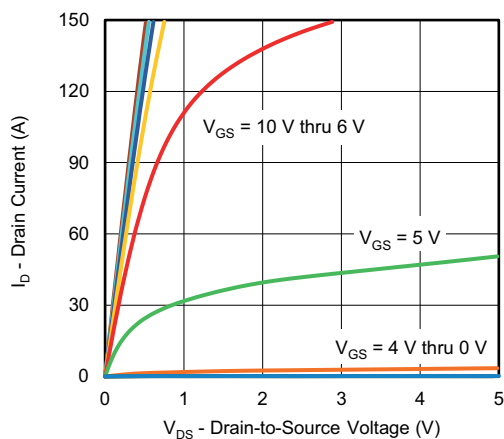
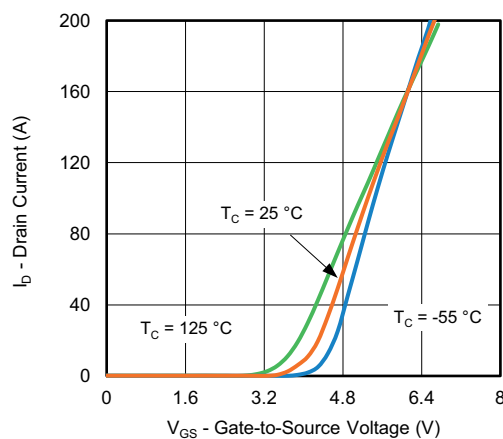
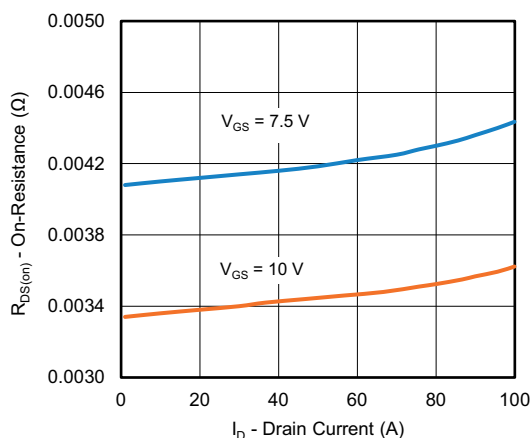
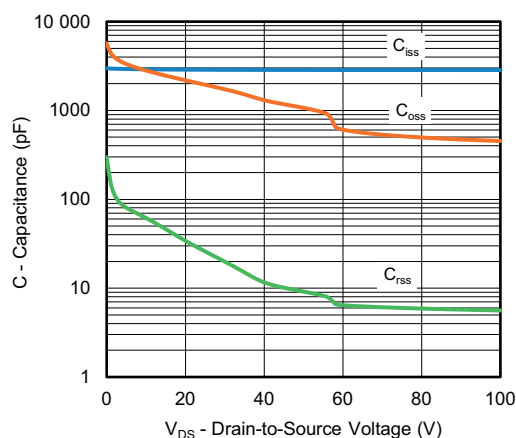
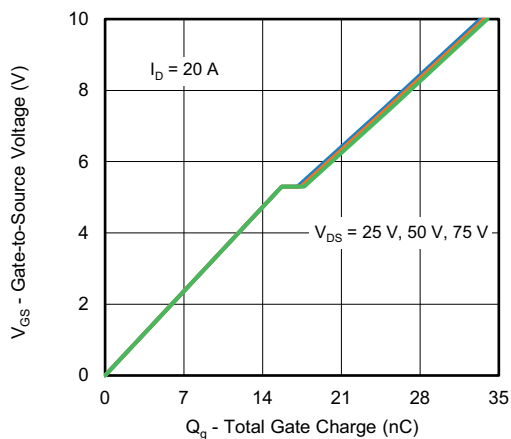
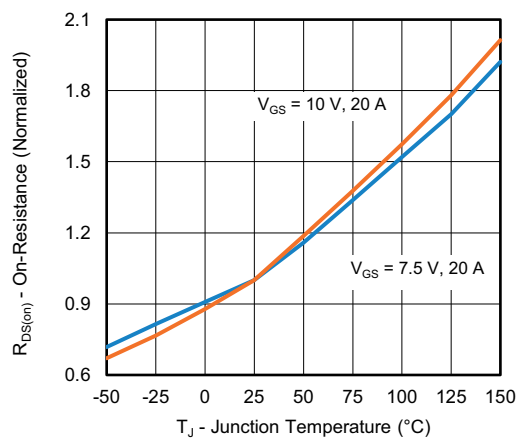


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	58	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-7.0	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.0034	0.0041	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.0041	0.0056	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	-	57	-	S
Dynamic ^b						
Input capacitance	C _{iSS}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	2850	-	pF
Output capacitance	C _{oss}		-	1050	-	
Reverse transfer capacitance	C _{rss}		-	9.2	-	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	-	33.7	51	nC
Gate-source charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 20 A	-	25.1	38	
Gate-drain charge	Q _{gd}		-	15.7	-	
Output charge	Q _{oss}		-	1.7	-	
Gate resistance	R _g	V _{DS} = 50 V, V _{GS} = 0 V	-	106.5	-	Ω
		f = 1 MHz	0.5	1.15	2	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 2.5 Ω, I _D ≅ 20 A, V _{GEN} = 10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	10	20	
Turn-off delay time	t _{d(off)}		-	26	52	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 2.5 Ω, I _D ≅ 20 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	19	38	
Rise time	t _r		-	14	28	
Turn-off delay time	t _{d(off)}		-	25	50	
Fall time	t _f		-	12	24	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	94	A
Pulse diode forward current	I _{SM}		-	-	300	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.74	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C	-	53	106	ns
Body diode reverse recovery charge	Q _{rr}		-	67	134	nC
Reverse recovery fall time	t _a		-	25	-	ns
Reverse recovery rise time	t _b		-	28	-	

Notes

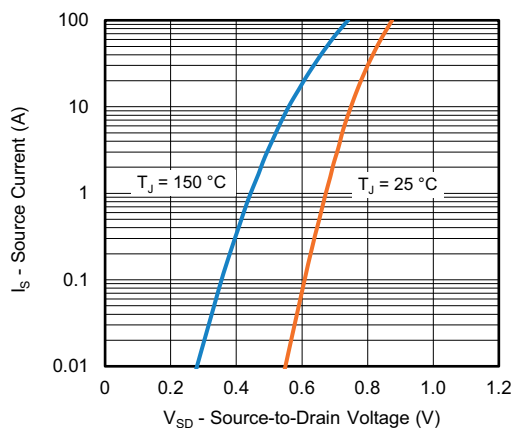
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

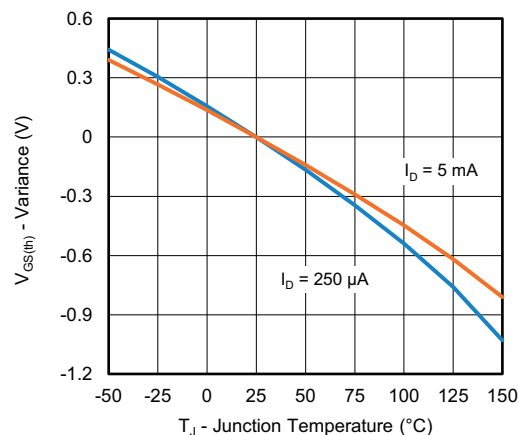
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



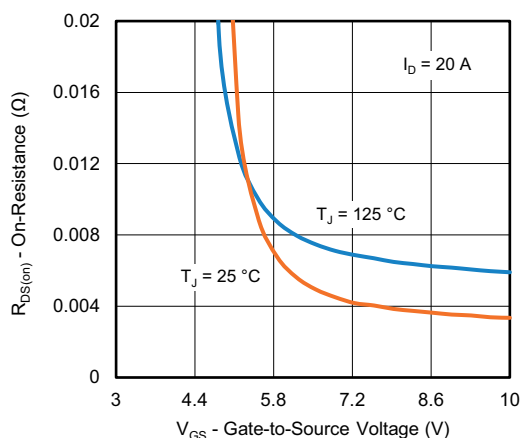
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



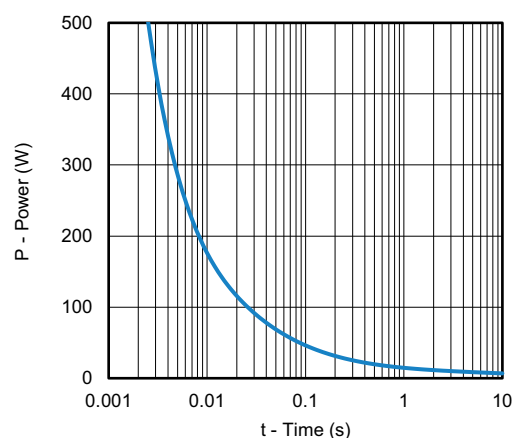
Source-Drain Diode Forward Voltage



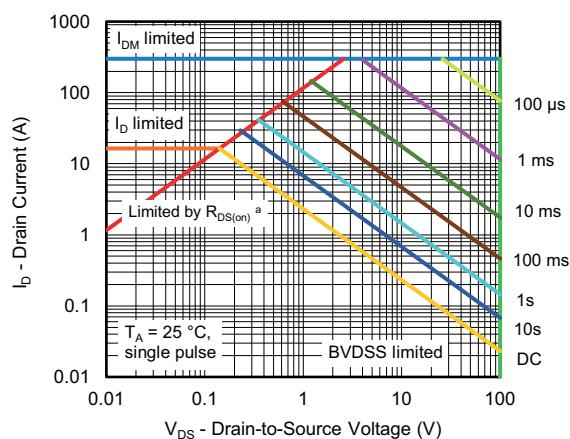
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



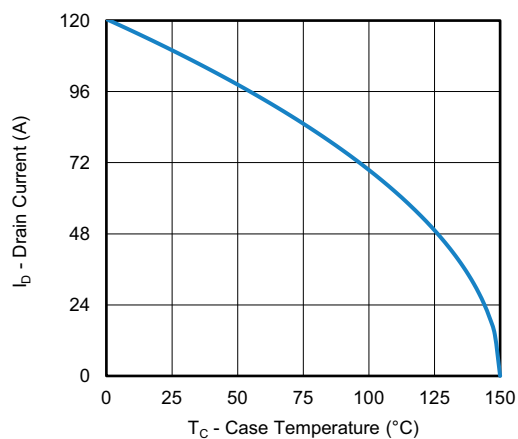
Safe Operating Area, Junction-to-Ambient

Note

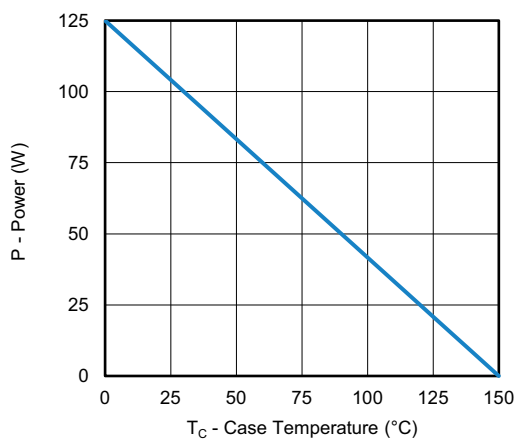
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



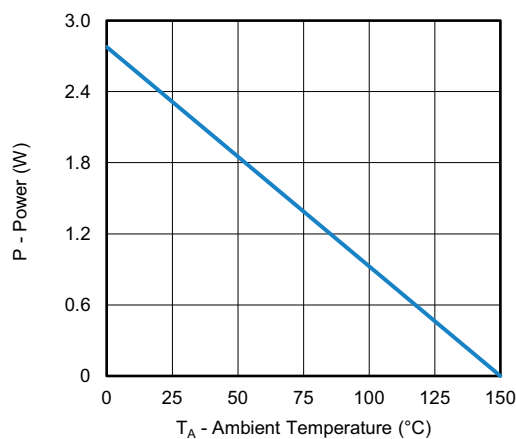
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



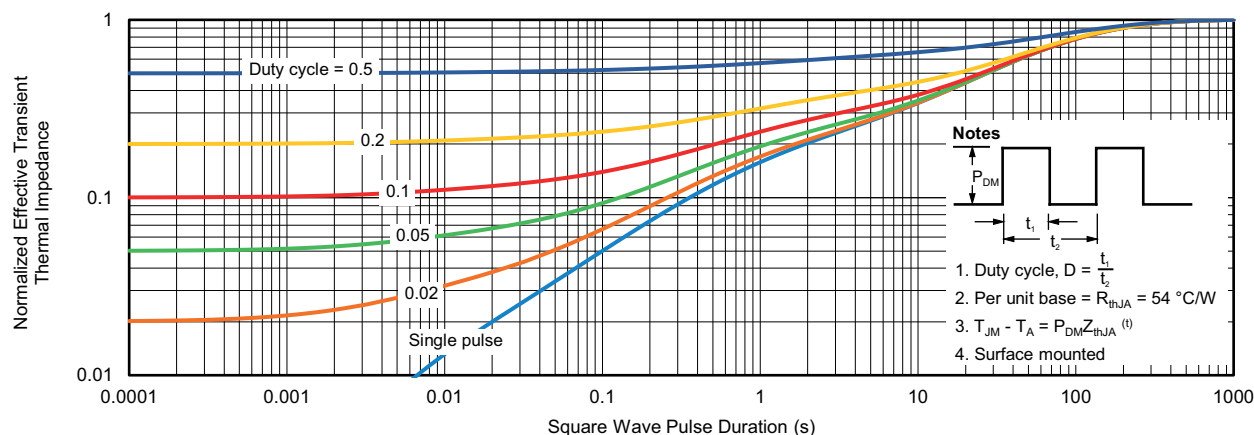
Power, Junction-to-Ambient

Note

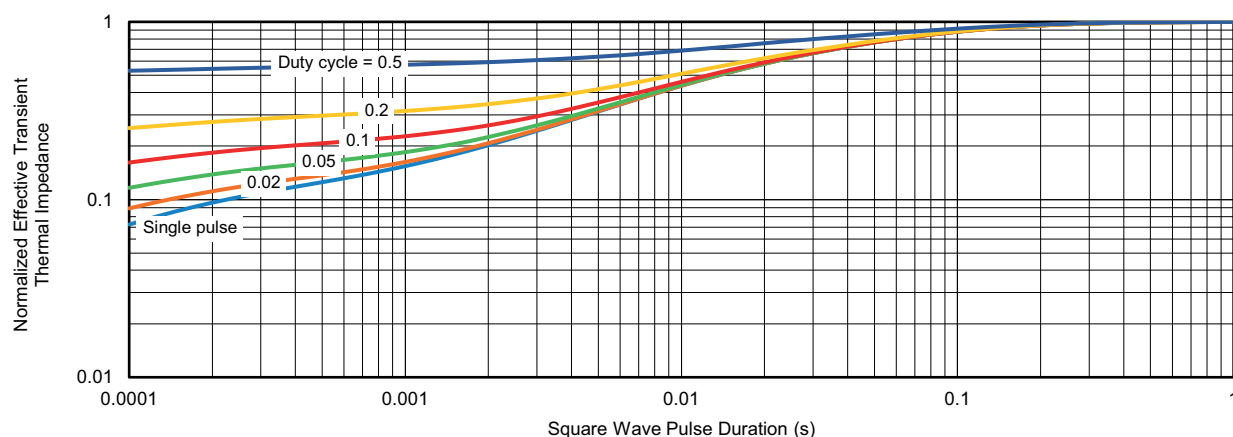
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63056.

PowerPAK® SO-8, (Single/Dual)



Notes

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: S17-0173-Rev. L, 13-Feb-17						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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