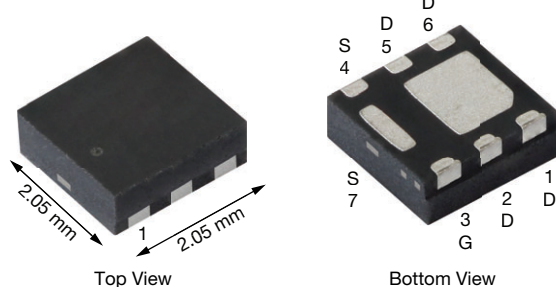


Automotive P-Channel 40 V (D-S) 175 °C MOSFET

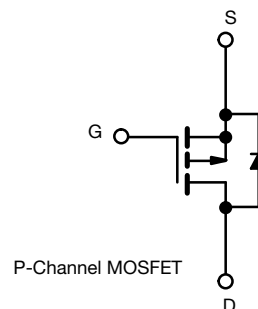
PowerPAK® SC-70W-6L Single

Marking Code: QRXXXX

PRODUCT SUMMARY

V_{DS} (V)	-40
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.0395
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.0545
I_D (A)	-9
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Wettable flank terminals
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE


P-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA405CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-40	V
Gate-source voltage ^f	V_{GS}	± 20	
Continuous drain current	I_D	$T_C = 25$ °C ^a	-9
		$T_C = 125$ °C	-7.9
Continuous source current (diode conduction) ^a	I_S	-9	A
Pulsed drain current ^b	I_{DM}	-36	
Single pulse avalanche current	I_{AS}	-13.5	
Single pulse avalanche energy	E_{AS}	9.11	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	13.6
		$T_C = 125$ °C	4.5
Soldering recommendations (peak temperature) ^{d, e}		260	°C
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	90	°C/W
Junction-to-case (drain)	R_{thJC}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Not intended for continuous use with positive gate voltage > 3 V. Operation in the range 3 V $< V_{GS} \leq 12$ V is limited to 25 % duty



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -40 V	-	-	-1	μA
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 125 °C	-	-	-50	
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 175 °C	-	-	-150	
On-state drain current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≥ -5 V	-8	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V	I _D = -5 A	-	0.0326	0.0395	Ω
		V _{GS} = -10 V	I _D = -5 A, T _J = 125 °C	-	-	0.0616	
		V _{GS} = -10 V	I _D = -5 A, T _J = 175 °C	-	-	0.0727	
		V _{GS} = -4.5 V	I _D = -4 A	-	0.0453	0.0545	
Forward transconductance ^b	g _{fs}	V _{DS} = -10 V, I _D = -7 A		-	18	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	-	1142	1700	pF
Output capacitance	C _{oss}			-	83	125	
Reverse transfer capacitance	C _{rss}			-	70	105	
Total gate charge ^c	Q _g	V _{GS} = -10 V	V _{DS} = -20 V, I _D = -8 A	-	22.6	34	nC
Gate-source charge ^c	Q _{gs}			-	4.4	-	
Gate-drain charge ^c	Q _{gd}			-	4.1	-	
Gate resistance	R _g	f = 1 MHz		3.3	6.6	9.9	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = -20 V, R _L = 8 Ω I _D ≡ -2.5 A, V _{GEN} = -10 V, R _g = 1 Ω		-	9	15	ns
Rise time ^c	t _r			-	4	8	
Turn-off delay time ^c	t _{d(off)}			-	32	50	
Fall time ^c	t _f			-	6	10	
Source-Drain Diode Ratings and Characteristics							
Pulsed current ^a	I _{SM}			-	-	-36	A
Forward voltage	V _{SD}	I _F = -5 A, V _{GS} = 0		-	-0.85	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -2 A, di/dt = 100 A/μs		-	14	30	ns
Body diode reverse recovery charge	Q _{rr}			-	9	20	nC
Reverse recovery fall time	t _a			-	9	-	ns
Reverse recovery rise time	t _b			-	5	-	
Body diode peak reverse recovery current	I _{RM(REC)}			-	-1.5	-	A

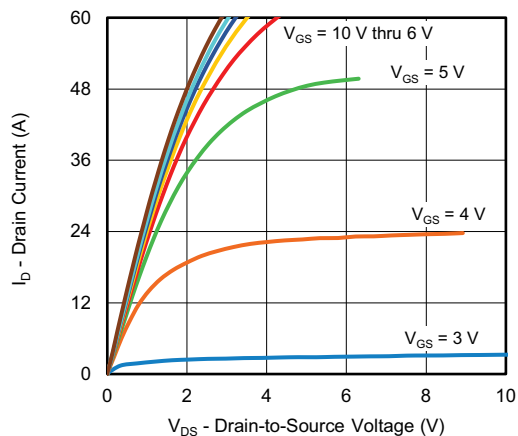
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

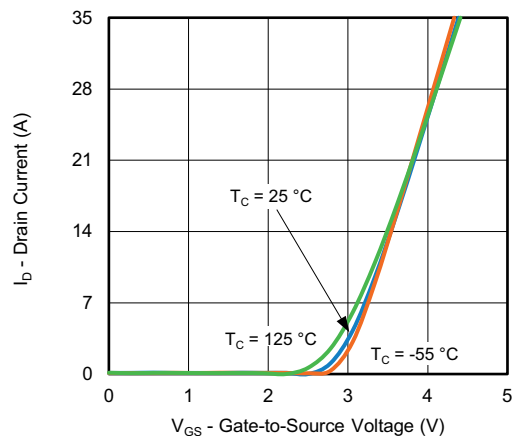
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



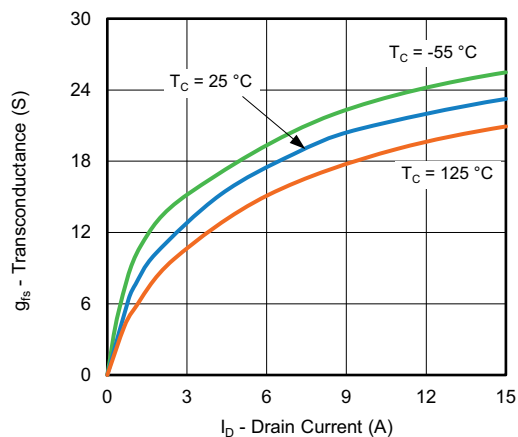
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



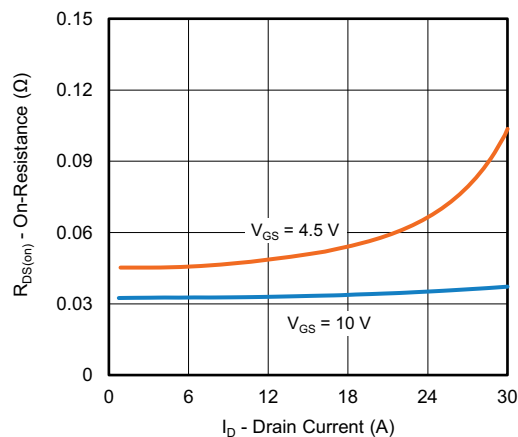
Output Characteristics



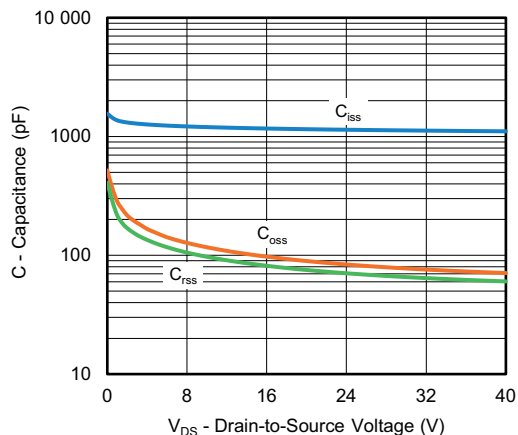
Transfer Characteristics



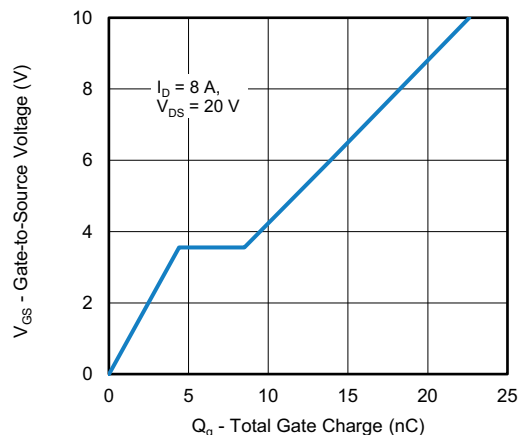
Transconductance



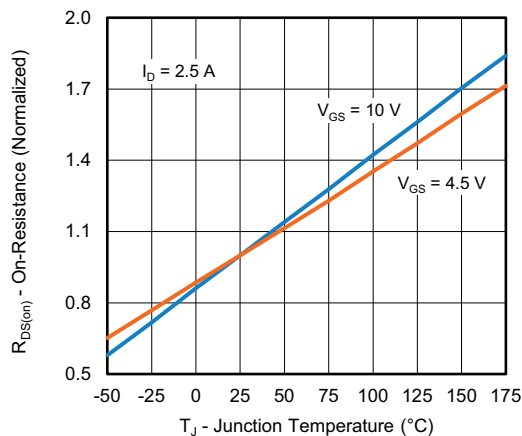
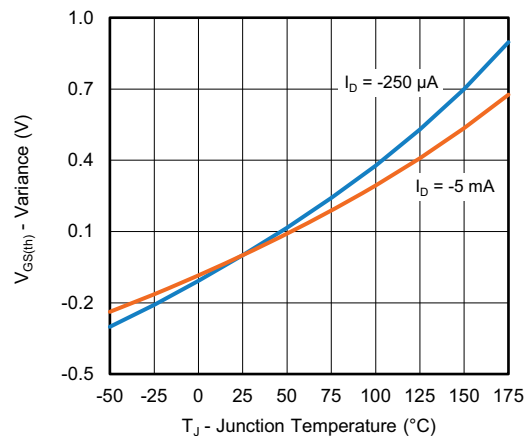
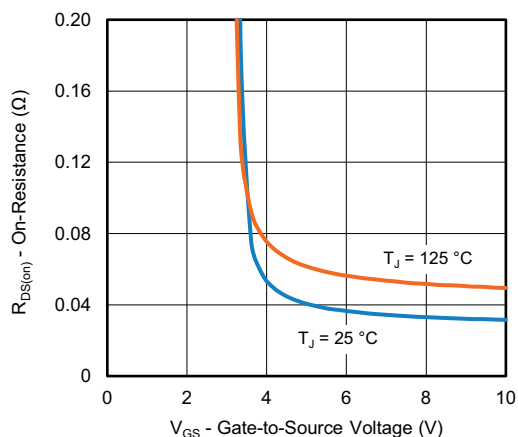
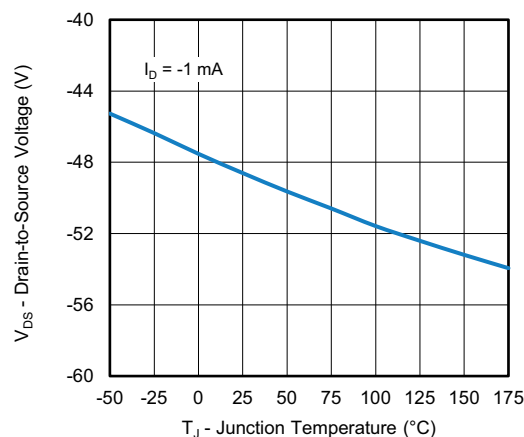
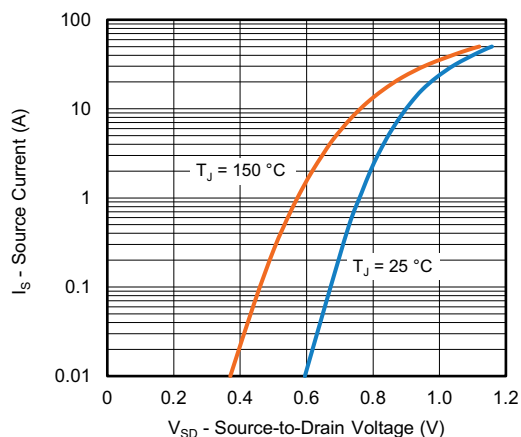
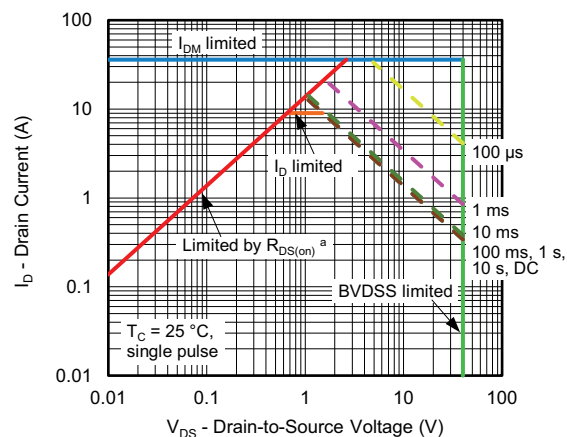
On-Resistance vs. Drain Current



Capacitance



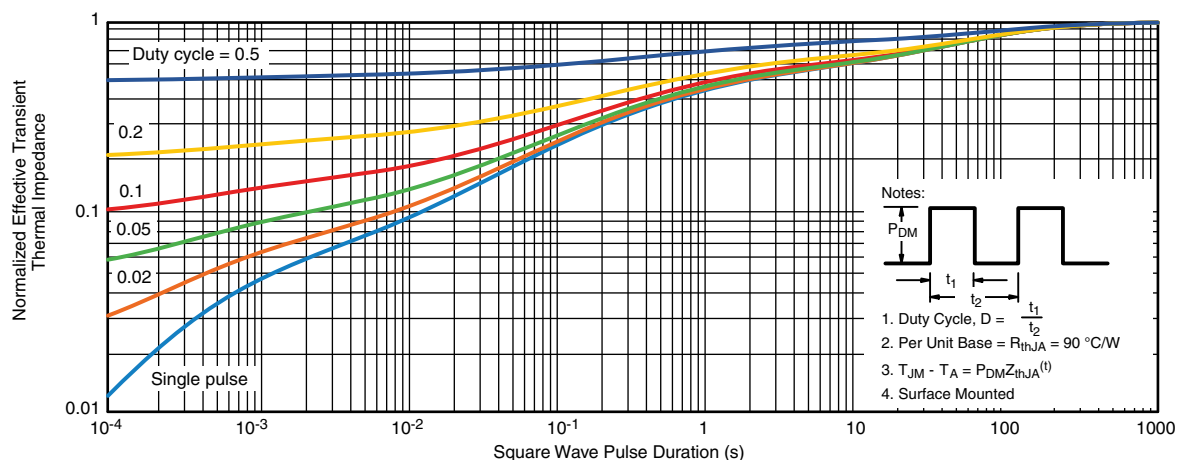
Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Drain Source Breakdown vs. Junction Temperature

Source-Drain Diode Forward Voltage

Safe Operating Area
Note

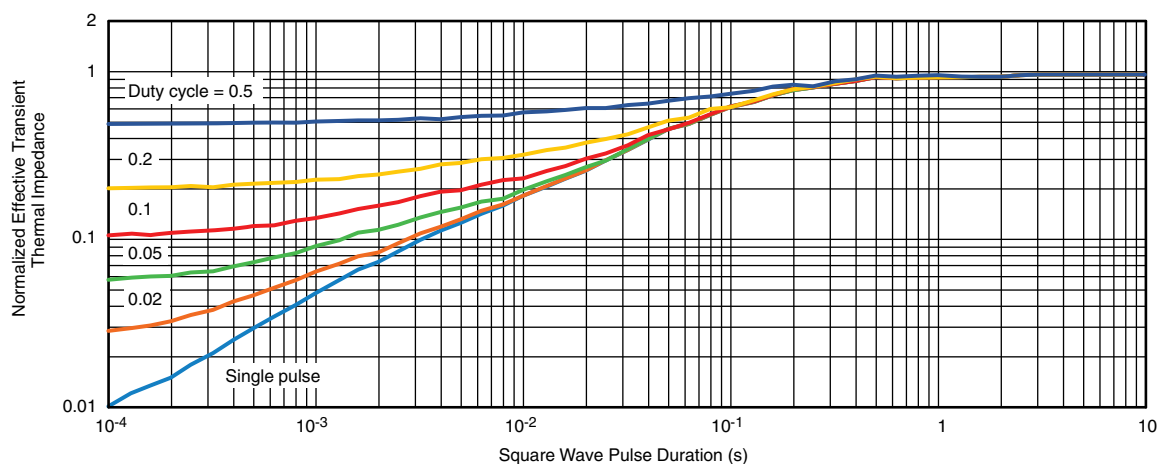
- $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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