

# 3.5 A, 78 mΩ, 2.8 V to 23 V True Reverse Current Blocking eFuse With Programmable Current Limit and OVP

## OPERATION DESCRIPTION

The SIP32433A and SIP32433B are single-channel eFuses that integrate multiple control and protection features, which provide increased controllability and reliability, with simplified designs and minimal external components.

The SIP32433A and SIP32433B protect both power sources and downstream circuitry connected to the switch from overloads, short circuits, voltage surges, and excessive inrush currents.

The output current limit can be set by a single external resistor.  $V_{IN}$  overvoltage protection and undervoltage lockout threshold levels can be set with an external resistor network.  $V_{IN}$  inrush current requirements can be set with a single external soft start capacitor.

Upon switch-off due to latchable faults, the SIP32433A will latch the power switch off and the PGD will remain low. The switch can restart by resetting the EN or  $V_{IN}$ . The SIP32433B will auto retry if there is no OTP or OVP fault. The retry delay time is 32 times the soft start time set by the CSS.

The switch is characterized for operation over a junction temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## APPLICATIONS

- Industrial
- IoT and smart home
- Medical and healthcare equipment
- Network and telecom equipment
- Data storage, solid state drives
- Computing
- PLC
- Lighting
- Gaming consoles

## FEATURES

- 2.8 V to 23 V operation voltage
- 28 V max. voltage rating with 24 V internal OVP
- 78 mΩ typical switch resistance
- 0.3 A to 3.5 A current limit setting range
- Current limit accuracy of  $\pm 8\%$
- Fast short circuit protection response
- OCP triggering without overhead current
- Programmable turn-on slew rate
- Turn-on delay: 190  $\mu\text{s}$
- Adjustable OVP (and fixed 24 V OVP at  $V_{IN}$ )
- Adjustable UVLO
- Over-temperature protection
- ESD / HBM:  $> 2\text{ kV}$
- ESD / CDM:  $> 750\text{ V}$
- PGD: power good indicator output
- Compact TDFN10 3 mm x 3 mm package (for AEC-Q100 qualified automotive applications, please refer to SIPQ32433)
- 6 A uni-directional parts available with [SIP32434](#)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## TYPICAL APPLICATION CIRCUIT

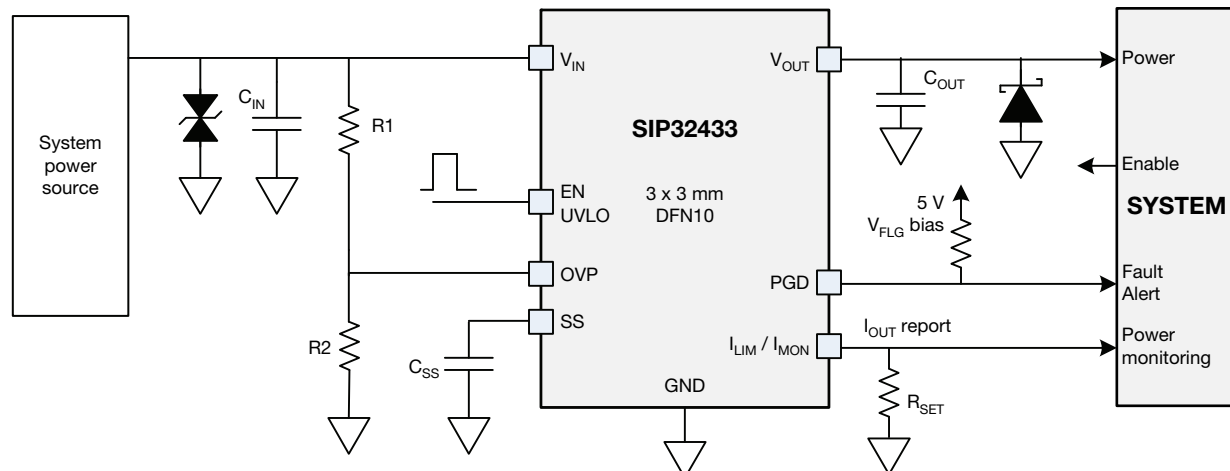


Fig. 1 - Application Circuit



ORDERING INFORMATION						
PART NUMBER	OCP RESPONSE	$R_{DS(on)}$ (m $\Omega$ )	TRUE REVERSE CURRENT BLOCKING	REPORT	MARKING CODE	PACKAGE
SIP32433ADN-T1E4	Latch	78	Yes	PG	2433A	DFN10 3 mm x 3 mm
SIP32433BDN-T1E4	Auto-retry	78	Yes	PG	2433B	DFN10 3 mm x 3 mm
SIP32433AEVB	Evaluation board					
SIP32433BEVB	Evaluation board					

**Note**

- For AEC-Q100 qualified automotive applications, please refer to SIPQ32433ADN-T1E4 and SIPQ32433BDN-T1E4

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	CONDITION	LIMIT	UNIT	
Input voltage ( $V_{IN}$ )	Reference to GND	-0.3 to +28	V	
Output voltage ( $V_{OUT}$ )	Reference to GND	-0.3 to +28		
		-5 V for +5 $\mu$ s		
EN voltage	Reference to GND	-0.3 to +24		
OVP	Reference to GND	-0.3 to +6		
SS	Reference to GND	-0.3 to +6		
$I_{LIM}$		-0.3 to +6		
PGD		-0.3 to +6		
Maximum continuous switch current		3.5		A
Thermal resistance ( $\theta_{thJA}$ )		44.8		$^{\circ}$ C/W
ESD rating	HBM	$\pm$ 1	kV	
ESD rating	CDM	$\pm$ 1		
Latch up current	Per JESD78E, Class II	100	mA	
Temperature				
Operating junction temperature		-40 to +150	$^{\circ}$ C	
Storage temperature		-65 to +150		

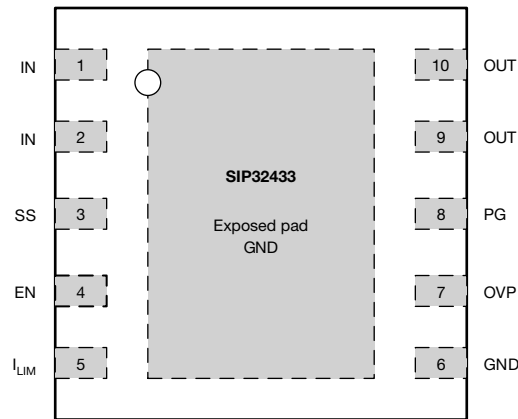
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
ELECTRICAL	LIMIT	UNIT
Input voltage ( $V_{IN}$ )	2.8 to 23	V
Operating junction temperature	-40 to +125	$^{\circ}$ C



ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = 12\text{ V}$ , $T_J = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , $V_{EN(H)} = 2.4\text{ V}$ , $C_{OUT} = 0.1\text{ }\mu\text{F}$ , $R_{LIM} = 4.1\text{ k}\Omega$	LIMITS			UNIT
			MIN.	TYP.	MAX.	
<b>Power Supply</b>						
Power input voltage	$V_{IN}$	Operating input voltage range	2.8	-	28	V
Quiescent current	$I_{Q(ON)}$	$EN = 1.8\text{ V}$ , $V_{IN} = 2.8\text{ V}$ to $28\text{ V}$ , $V_{OUT}$ open	-	250	340	$\mu\text{A}$
Shutdown current	$I_{Q(SD)}$	$V_{IN} = 2.8\text{ V}$ to $28\text{ V}$ , $EN = 0\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	-	0.6	5	
OVP switch-off current	$I_{Q(OVP)}$	$V_{IN} = 2.8\text{ V}$ to $28\text{ V}$ , $EN = 2.4\text{ V}$ , $OVP = 1.4\text{ V}$	-	1	-	
<b><math>V_{IN}</math> ULVO</b>						
Switch $V_{OUT}$ leakage	$I_{UVLO\_OUT}$		-100	-	+100	nA
Switch $V_{IN}$ leakage	$I_{UVLO\_IN}$		-	-	5	$\mu\text{A}$
<b>Overvoltage Protection</b>						
OVP threshold	$V_{OVP}$	$V_{IN} = 12\text{ V}$ , OVP rising	1.14	1.2	1.26	V
OVP hysteresis	$OVP_{HST}$		60	105	140	mV
OVP leakage	$I_{OVP}$	$V_{OVP} = 1.2\text{ V}$ on the pin, $T_A = 25\text{ }^\circ\text{C}$	-	40	100	nA
IN pin internal fixed OVP	$IN_{OVP}$	$T_A = 25\text{ }^\circ\text{C}$	23	24	25.6	V
<b>EN / UVLO</b>						
EN on threshold	$V_{UVPR}$	$V_{EN}$ rising	-	1.25	-	V
EN off threshold	$V_{UVPF}$	$V_{EN}$ falling	-	1.05	-	
EN / UVLO leakage		$V_{EN} = 1.2\text{ V}$	-0.25	-	+0.25	$\mu\text{A}$
<b>Overcurrent Protection</b>						
Current limit voltage threshold	$V_{OCP}$	Voltage that triggers the OCP shown on $I_{LIM}$ pin	-	0.6	-	V
Current limit accuracy	$I_{OCP}$	$V_{IN} - V_{OUT} = 1\text{ V}$ , $R_{SET} = 4.1\text{ k}\Omega$	1.39 3.32	1.5 3.5	1.6 3.68	A
Current limit setting range		Minimum $R_{SET} = 1.77\text{ k}\Omega$	0.25	-	3.5	
Current limit hold-up time	$t_{LIM}$	Current limiting timeout, if no OTP	4	6	8	ms
<b>Power Switch</b>						
On resistance	$R_{DS(ON)}$	$V_{IN} = 3\text{ V}$ to $22\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 25\text{ }^\circ\text{C}$ $V_{IN} = 3\text{ V}$ to $22\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $T_J = 85\text{ }^\circ\text{C}$	- -	78 -	100 130	$\text{m}\Omega$
Output leakage at switch off		$V_{IN} = 28\text{ V}$ , $V_{EN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , sourcing	-	-	5	
<b>PGD, Power Good</b>						
PGD pull-down resistance	$R_{PG}$	$V_{IN} = 5\text{ V}$ , output pin = $0.1\text{ V}$	-	5.2	10	$\Omega$
PGD oII leakage	$I_{PG}$	Biased with $5\text{ V}_{DC}$	-	0.01	1	$\mu\text{A}$
<b>Switching Characteristics</b>						
<b>EN / UVLO</b>						
Switch turn-on delay time	$T_{ON\_DLY}$	From EN / UVLO voltage, $V_{UVPR}$ to $V_{OUT}$ reaches 10 % $V_{IN}$ , $R_L = 10\text{ }\Omega$ , $C_L = 10\text{ }\mu\text{F}$ , $C_{SS}$ open	-	190	-	$\mu\text{s}$
Shutdown delay	$T_{OFF\_DLY}$	From EN / UVLO low to $V_{OUT} = 0.9 \times V_{IN}$ , $R_L = 10\text{ }\Omega$ , $C_L = 10\text{ }\mu\text{F}$ , $C_{SS}$ open	-	10	-	
<b>OVP Timing</b>						
OVP off time	$t_{OVP}$	$R_L = 100\text{ }\Omega$ , $C_L = 0\text{ }\mu\text{F}$ , OVP steps from $1\text{ V}$ to $1.4\text{ V}$ ; measured from OVP pin voltage crossing $1.2\text{ V}$ threshold to $V_{OUT} = 0.9 \times V_{IN}$	-	0.3	1	$\mu\text{s}$
Internal OVP off time	$t_{OVP\_INT}$	$R_L = 100\text{ }\Omega$ , $C_L = 0\text{ }\mu\text{F}$ , $V_{IN}$ steps from $22\text{ V}$ to $26\text{ V}$ ; measured from $V_{IN}$ pin voltage crossing $24\text{ V}$ threshold to $V_{OUT} = 0.9 \times V_{IN}$	-	1.5	-	
Flag reporting delay		PGD pull up to $5\text{ V}$ through a $100\text{ k}\Omega$ ; delay time from OVP pin voltage step to PGD is below $0.5\text{ V}$	-	-	2	
<b>Overcurrent protection</b>						
Moderate overcurrent protection	$t_{OCP}$	Load current is 120 % of current limit threshold	-	1.1	-	$\mu\text{s}$

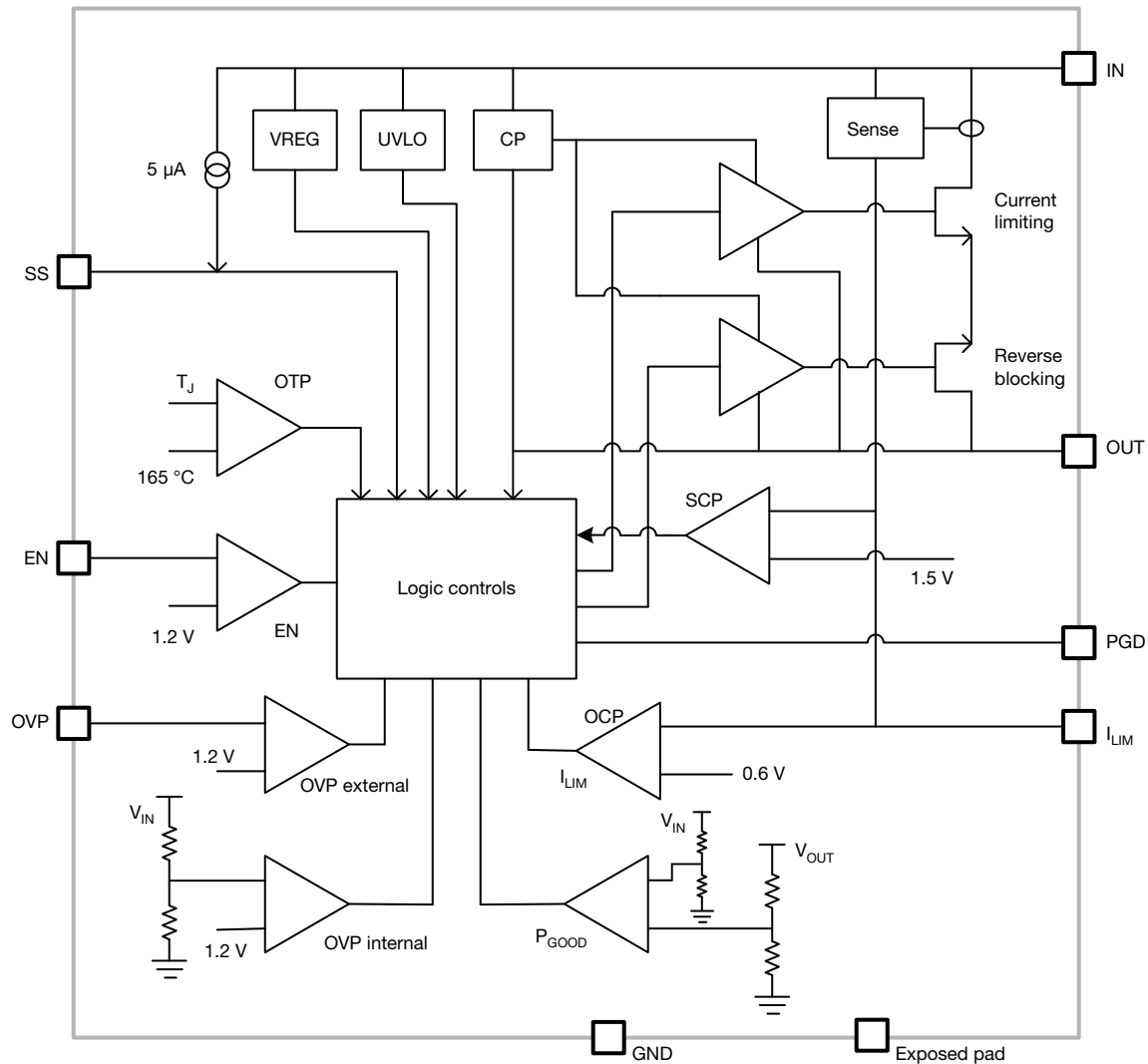
<b>ELECTRICAL SPECIFICATIONS</b>						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED $V_{IN} = 12\text{ V}$ , $T_J = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}$ , $V_{EN(H)} = 2.4\text{ V}$ , $C_{OUT} = 0.1\text{ }\mu\text{F}$ , $R_{LIM} = 4.1\text{ k}\Omega$	LIMITS			UNIT
			MIN.	TYP.	MAX.	
<b>Soft Start Control</b>						
Output rise up time	$t_R$	$V_{IN} = 12\text{ V}$ , $R_L = 10\text{ }\Omega$ , $C_L = 10\text{ }\mu\text{F}$ , $V_{OUT}$ from 10 % to 90 % $V_{IN}$ , $C_{SS}$ open	-	350	-	$\mu\text{s}$
		$V_{IN} = 12\text{ V}$ , $R_L = 10\text{ }\Omega$ , $C_L = 10\text{ }\mu\text{F}$ , $V_{OUT}$ from 10 % to 90 % $V_{IN}$ , $C_{SS} = 22\text{ nF}$	-	4.7	-	ms
SS charge current			-	5	-	$\mu\text{A}$
<b>Auto Retry</b>						
Auto retry time	$t_{RTY}$	Delay time of restart after all faults are removed; this is defined as the number of cycles of soft start time set by $C_{SS}$	-	32	-	
<b>Thermal Shutdown</b>						
Thermal shutdown		Temperature increases	-	165	-	$^\circ\text{C}$
Thermal shutdown hysteresis			-	45	-	$^\circ\text{C}$

**PACKAGE OUTLINE**

**Fig. 2 - Pin Out Drawing (top view)**

<b>PIN DESCRIPTION</b>		
PIN #	NAME	FUNCTION
1, 2	$V_{IN}$	Power switch input pins; two pins are fused inside the package
3	SS	A capacitor from this pin to GND sets output voltage slew rate
4	EN / UVLO	Active high switch control input; $V_{THL} < 0.3\text{ V}$ , $V_{THH} > 1.4\text{ V}$
5	$I_{LIM} / I_{MON}$	A resistor from this pin to GND sets the overload and short-circuit current limit; the pin can be used for current reporting, referring to the voltage developed over the current limit setting resistor
6	GND	Ground
7	OVP	Input for setting the programmable overvoltage protection threshold. An overvoltage event turns-off the internal FET and asserts FLT to indicate the overvoltage fault
8	PGD	Open drain output, when $V_{OUT}$ is $\geq 95\%$ $V_{IN}$ , and none of the following faults are triggered: OT, OC, OV
9, 10	$V_{OUT}$	Power switch output pins; two pins are fused inside the package
Exposed pad	GND	The package's central exposed pad must be connected to the ground plane; optimal PCB thermal design will enhance device performance

**FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE**

TRUTH TABLE	
EN	SWITCH
1	ON
0	OFF


**Fig. 3 - Device Block Diagram**

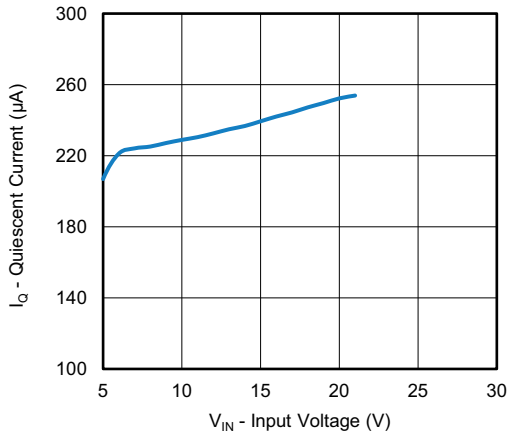


Fig. 4 - Quiescent Current vs. Input

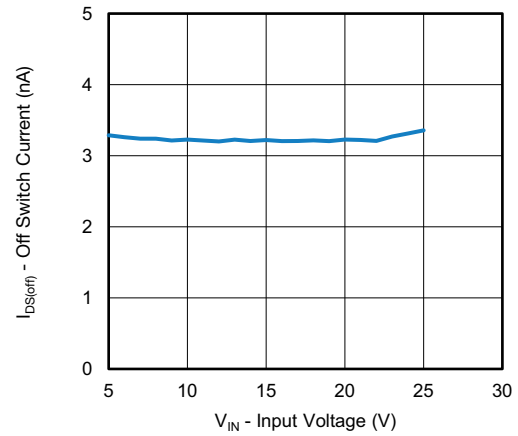


Fig. 7 - Switch Off Current vs. Input

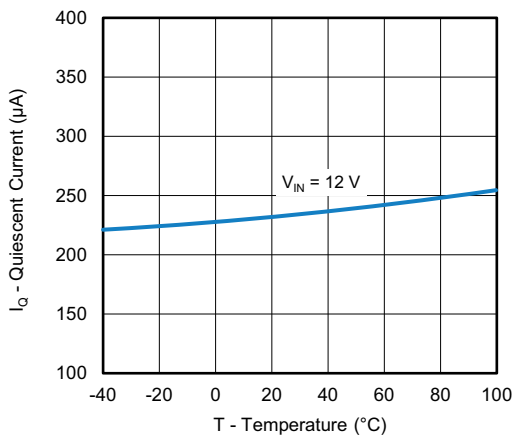


Fig. 5 - Quiescent Current vs. Temperature

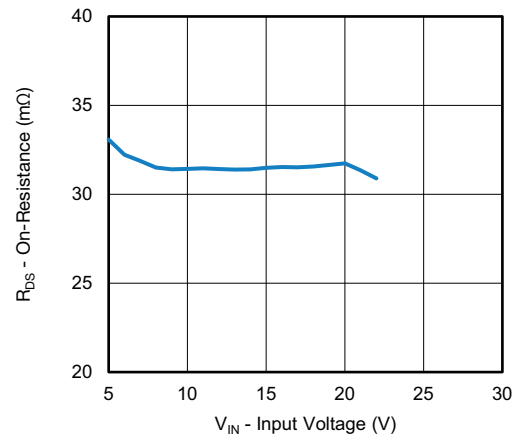


Fig. 8 - On Resistance vs. Input

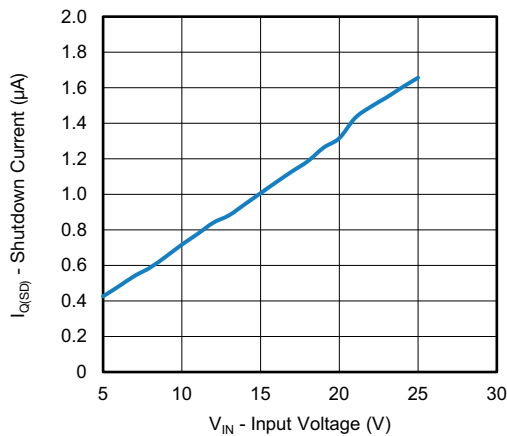


Fig. 6 - Shutdown Current vs. Input

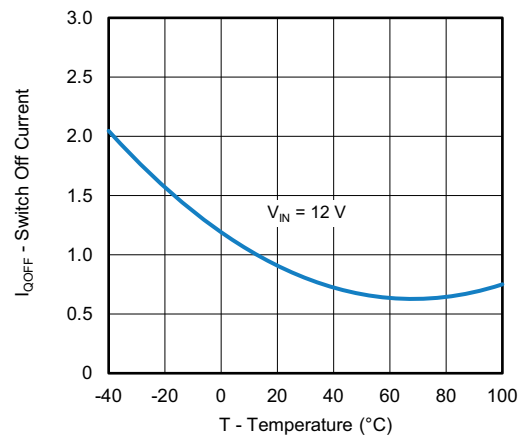


Fig. 9 - Shutdown Current vs. Temperature

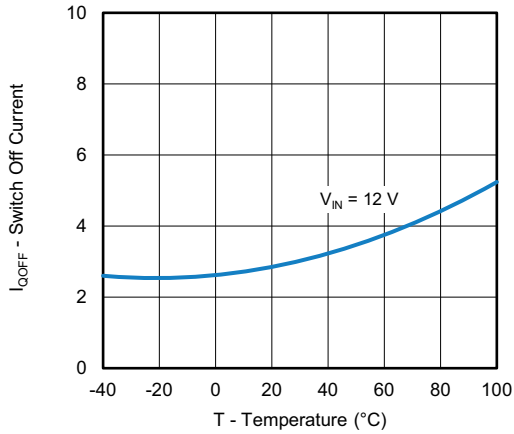


Fig. 10 - Switch Off Current vs. Temperature

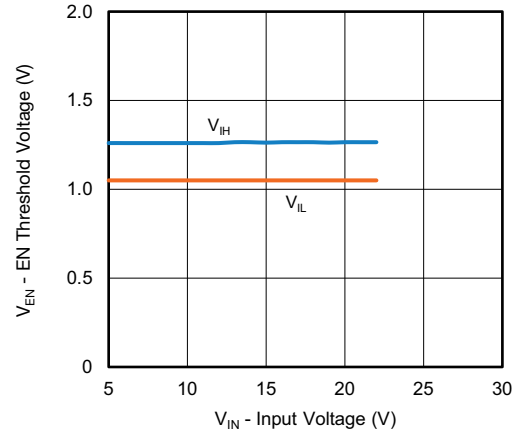


Fig. 13 - Threshold Voltage vs. Input Voltage V<sub>IN</sub>

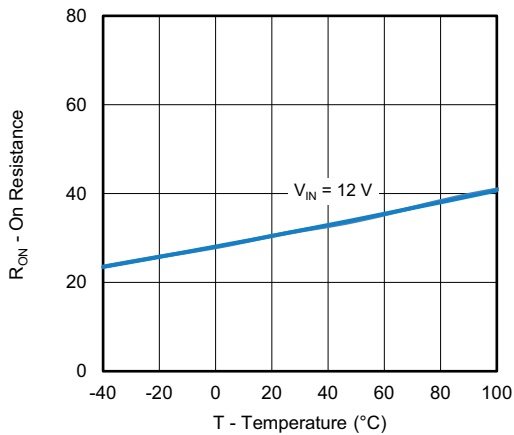


Fig. 11 - On Resistance vs. Temperature

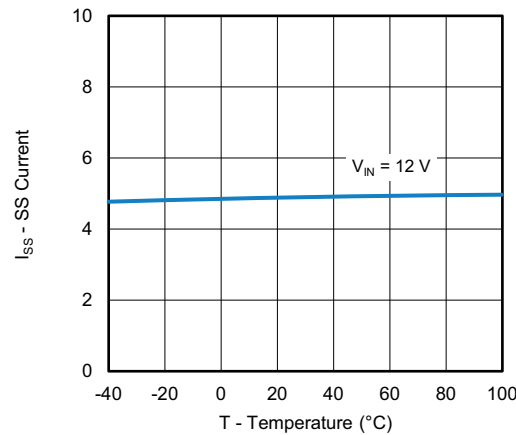


Fig. 14 - Soft Start Current vs. Temperature

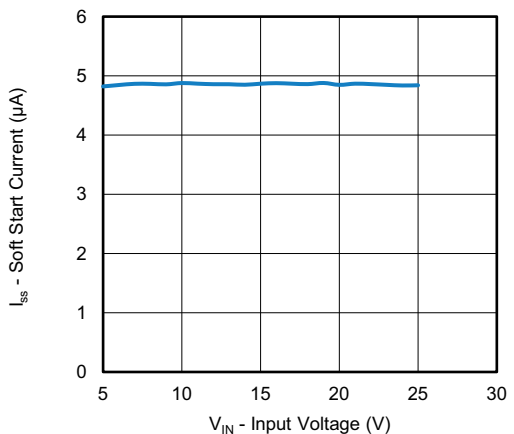


Fig. 12 - Soft Start Current vs. Input Voltage V<sub>IN</sub>

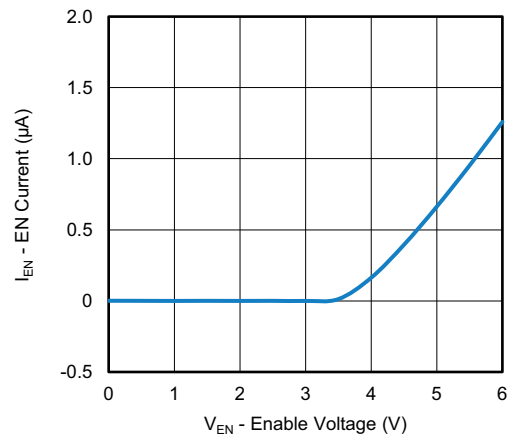


Fig. 15 - EN Current vs. EN Voltage

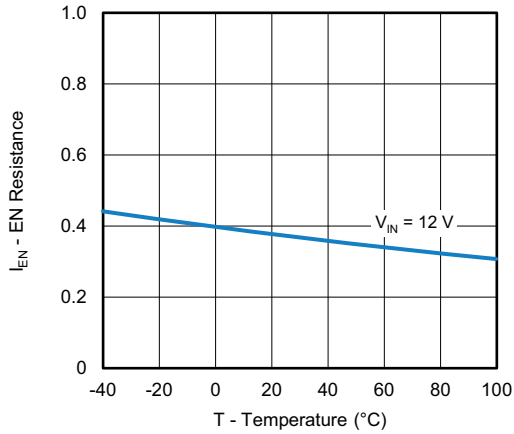


Fig. 16 - Enable Resistance vs. Temperature

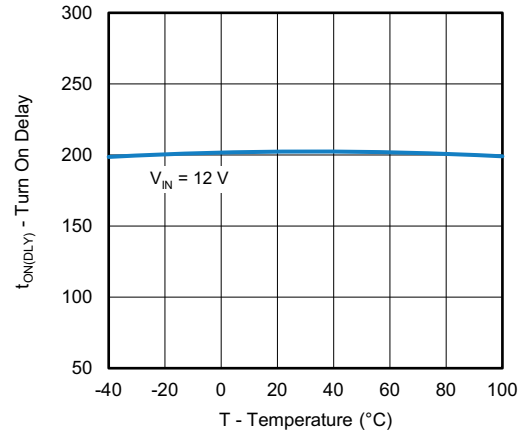


Fig. 18 - Turn On Delay Time vs. Temperature

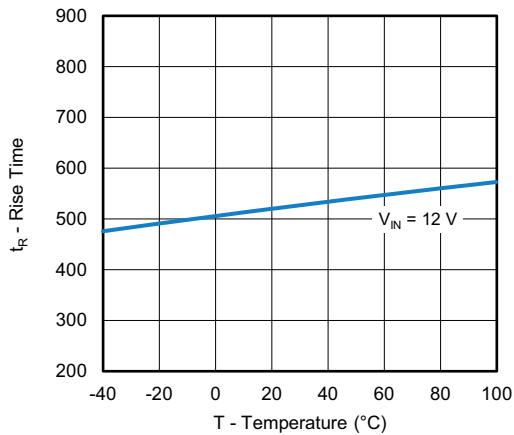


Fig. 17 - Rise Time vs. Temperature

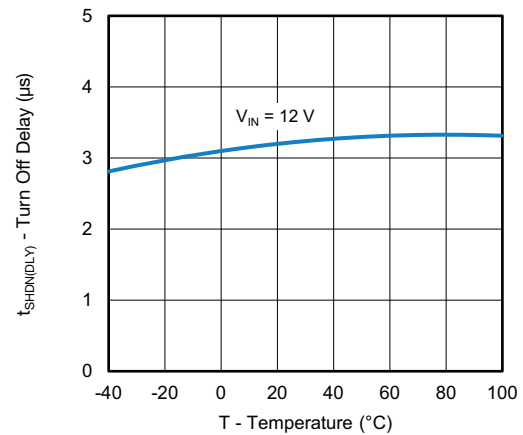
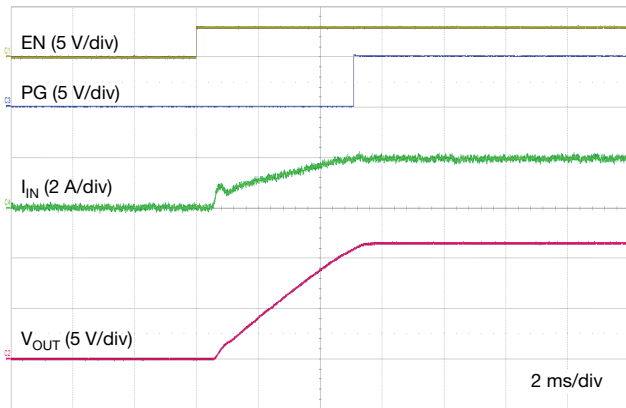


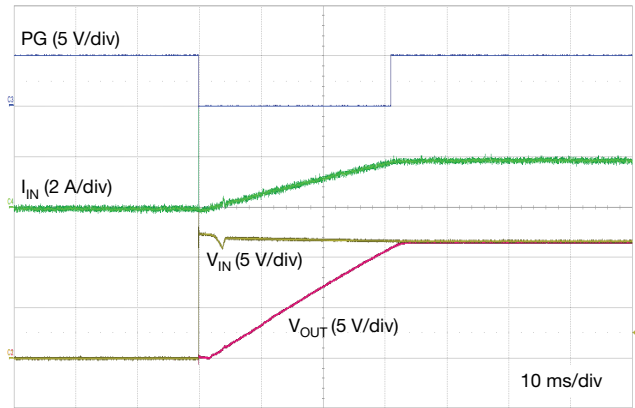
Fig. 19 - Turn Off Delay Time vs. Temperature



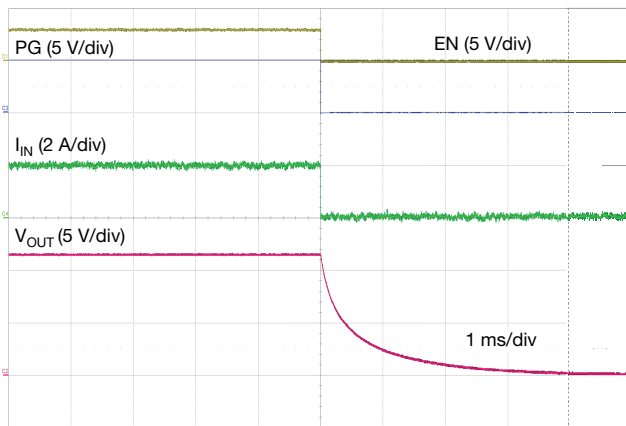
**TYPICAL CHARACTERISTICS**



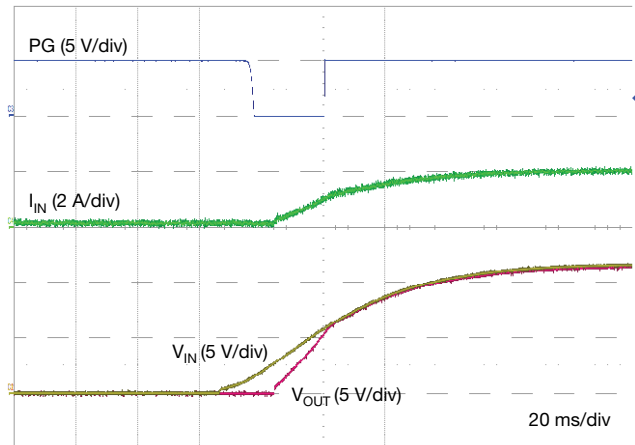
**Fig. 20 - Turn On by EN**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$



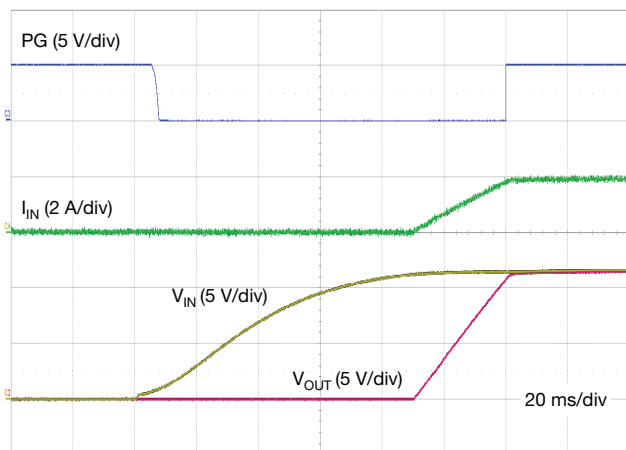
**Fig. 23 - Turn On by Hot-Plug of  $V_{IN}$**   
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$   
 EN Voltage Divider Resistors,  $1\ \text{M}\Omega$  and  $133\ \text{k}\Omega$



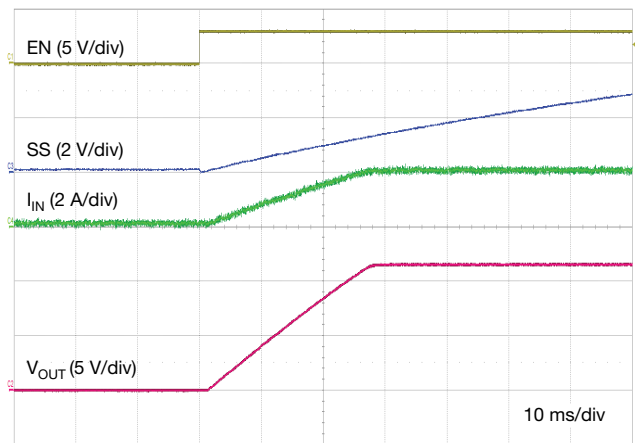
**Fig. 21 - Turn Off by EN**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$



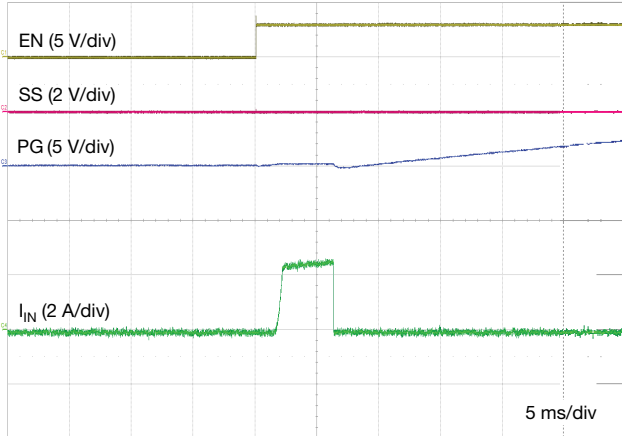
**Fig. 24 - Turn On by  $V_{IN}$  When EN is 3 V**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$



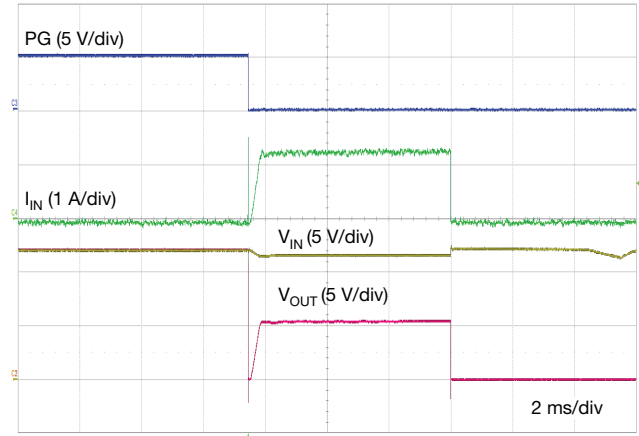
**Fig. 22 - Turn On by  $V_{IN}$**   
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$   
 EN Voltage Divider Resistors,  $1\ \text{M}\Omega$  and  $133\ \text{k}\Omega$



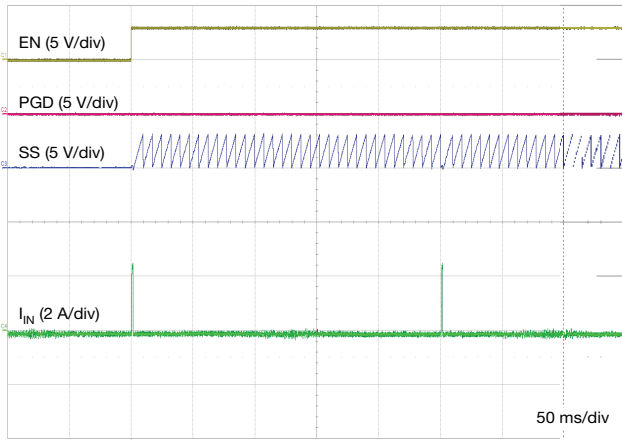
**Fig. 25 - Turn On by EN Into Resistive Load**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $C_{SS} = 133\ \text{nF}$ ,  $R_{LIM} = 2.49\ \text{k}\Omega$



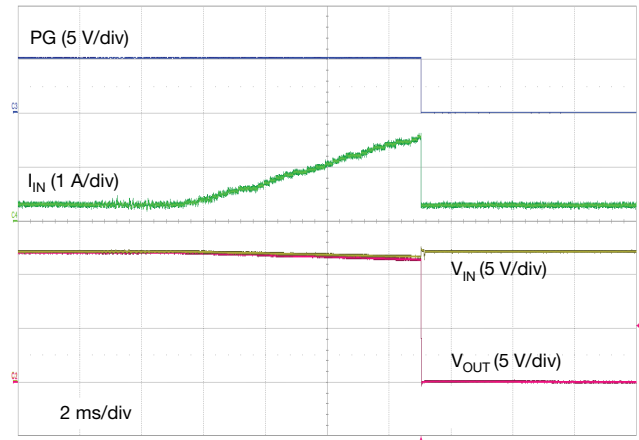
**Fig. 26 - Turn On Into Output Short**  
 $V_{IN} = 12\text{ V}$ ,  $C_{SS} = 133\text{ nF}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$



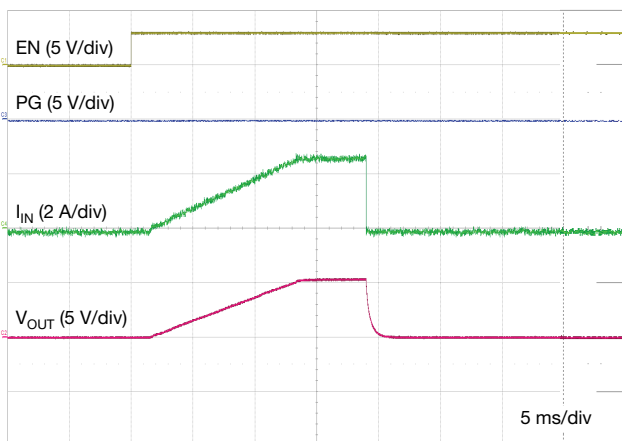
**Fig. 29 -  $V_{OUT}$  Short With a  $2\ \Omega$  Load**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 2\ \Omega$ ,  $C_L = 0\ \mu\text{F}$ ,  $C_{SS} = 133\text{ nF}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$



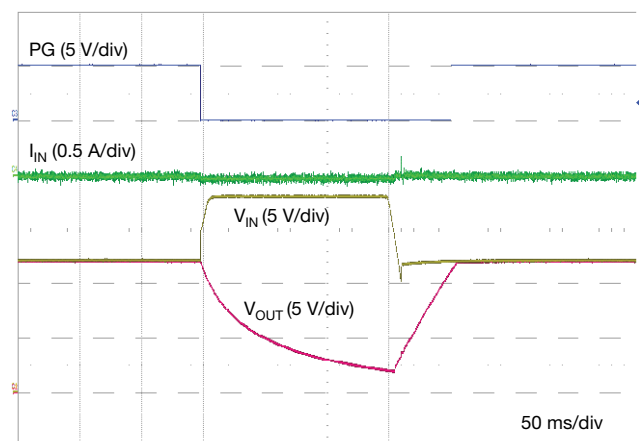
**Fig. 27 - Turn On Into Output Short, Auto-Retry**  
 $V_{IN} = 12\text{ V}$ ,  $C_{SS} = 133\text{ nF}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$



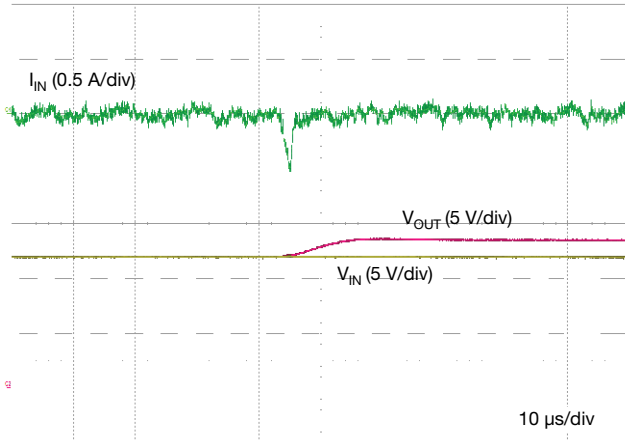
**Fig. 30 - Output Current Protection Increase Load Current Slowly**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 2\ \Omega$ ,  $C_L = 47\text{ nF}$ ,  $C_{SS} = 133\text{ nF}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$



**Fig. 28 - Turn On by EN Into OCP Load**  
 $V_{IN} = 12\text{ V}$ ,  $R_L = 2\ \Omega$ ,  $C_L = 47\ \mu\text{F} \times 3$ ,  $C_{SS} = 133\ \mu\text{F}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$



**Fig. 31 - Over Voltage Protection**  
 $R_L = 1\text{ k}\Omega$ ,  $C_L = 100\ \mu\text{F}$ ,  $C_{SS} = 133\text{ nF}$ ,  $R_{LIM} = 2.49\text{ k}\Omega$ ,  
 OVP Set to 18 V



**Fig. 32 - True Reverse Current Blocking**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT}$  Raised Up to  $13.5\text{ V}$

## OVERVIEW

The SIP32433A and SIP32433B are eFuses with comprehensive integrated control features that simplify the design and increase the reliability of the circuitry connected to the switch.

The 32 mΩ switches are designed to operate in the 2.8 V to 23 V range. An internally generated gate drive voltage ensures good  $R_{ON}$  linearity over the input voltage operating range.

The devices start their operation by checking the  $V_{IN}$ ,  $V_{OUT}$ , OVP, and EN / UVLO pins. When the voltages are in the ranges without exceeding under- or over-voltage protection thresholds, the PGD open drain switch is off. A high level on the EN / UVLO pin enables the internal MOSFET to start conducting and allows current to flow from IN to OUT. When EN / UVLO is held low, the internal MOSFET is turned off.

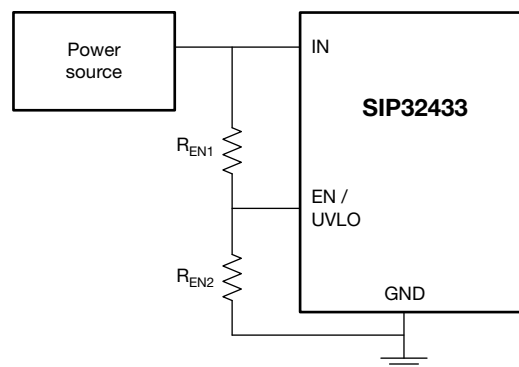
After a successful turn-on sequence, the device now actively monitors its load current, input voltage, and protects the load from harmful over-current, and over-voltage conditions. A built-in thermal sense circuit will detect junction over temperature and shut down the switch for safety.

## SWITCH ON / OFF, AND UNDER-VOLTAGE LOCK OFF PROTECTION - UVLO

EN / UVLO pin controls the on / off of the power switch. When EN / UVLO is at a logic high the switch is on. When EN / UVLO is at a logic low, the switch is off.

The SIP32433A and SIP32433B implement under-voltage protection on the EN / UVLO to turn off the output. It is a user-defined under-voltage protection setting to flexibly select the proper minimum applied voltage for the downstream load or the device's proper operation.

The diagram shows how a resistor divider from supply to GND can be used to set the UVLO set point for a given voltage supply level.



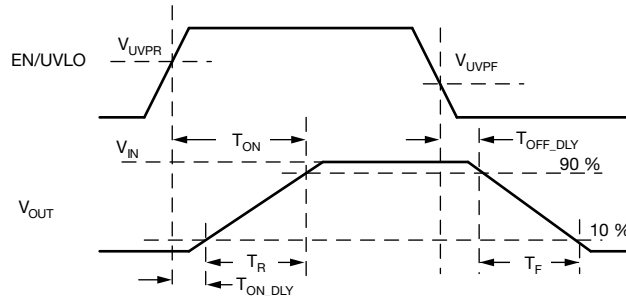
**Fig. 33**

The resistors must be sized large enough to minimize the constant leakage from supply to ground through the resistor divider network. At the same time, keep the current through the resistor network sufficiently larger than the leakage current on the EN / UVLO pin to minimize the error in the resistor divider ratio.

$$R_{EN1} = \frac{R_{EN2}(V_{IN} - V_{UVPR})}{V_{UVPR}}$$

Where  $V_{UVPR}$  is 1.25 V.

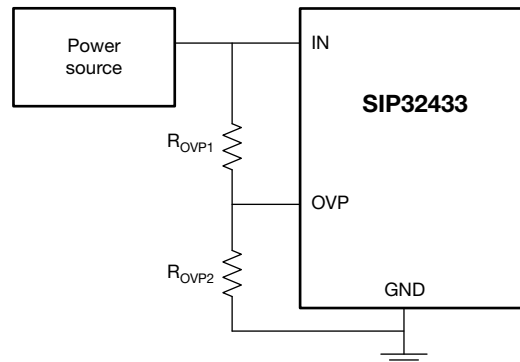
UVLO turn off delay ( $T_{OFF\_DLY}$ ) is typically 550  $\mu$ s and turn on delay  $T_{ON\_DLY}$  is typically 500  $\mu$ s.



**Fig. 34 - Switching Times**

### OVER-VOLTAGE PROTECTION (OVP)

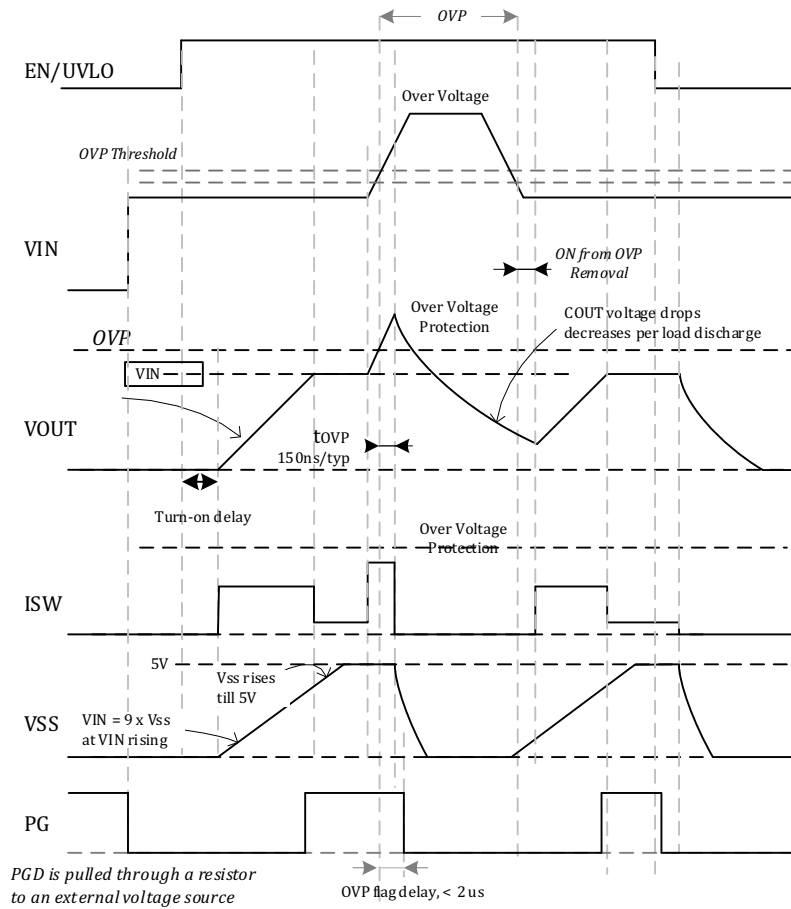
The SIP32433A and SIP32433B implement overvoltage protection (OVP) on both the  $V_{IN}$  and OVP pins to protect the output load in the event of an input over-voltage. When the input exceeds the over-voltage protection thresholds  $V_{OVP(R)}$  or the  $IN_{OVP}$ , which is typically 24 V, the device turns off the output within  $t_{OVP}$ , while the PGD asserts in the meantime. As long as an over-voltage condition is present on the input, the device stays disabled and the output will be turned off. Over-voltage is a non-latchable fault. Once the input voltage returns to the normal operating range, the device attempts to start up normally.



**Fig. 35**

$$\frac{R_{OVP1}}{R_{OVP2}} = \frac{V_{IN(OVP)} - 1.2 \text{ V}}{1.2 \text{ V}}$$

OVP voltage divider resistors total resistance should not be over 2.5 M $\Omega$ .



**Fig. 36 - Over-Voltage Protection**

**INRUSH CURRENT, AND OVER-CURRENT PROTECTION**

The SIP32433A and SIP32433B incorporate two protections against over-current:

- Adjustable slew rate (SR) for inrush current control
- Adjustable over-current protection / active current limit to protect against overload conditions

The over-current protection (OCP) is active also during soft start. The over-current protection circuit controls the switch impedance to limit the current to the level programmed by the R<sub>SET</sub> resistor.

If the over-current condition persists for more than 6 ms (typ.), the switch shuts off and alert the drain FLG is asserted, pulling the pin to GND.



### SLEW RATE CONTROL

An inrush current happens when the switch turns on into a large output capacitance. If the inrush current is not controlled, it can damage the input connectors and / or cause the system power supply to droop, leading to unexpected restarts elsewhere in the system.

The SIP32433A and SIP32433B provide integrated output slew rate control to manage the inrush current during start-up. This is achieved by forcing the  $V_{OUT}$  to follow the voltage on a soft start capacitor. A constant current source of 5  $\mu A$  charges the  $C_{SS}$ , generating a linear ramp up voltage on  $C_{SS}$ .

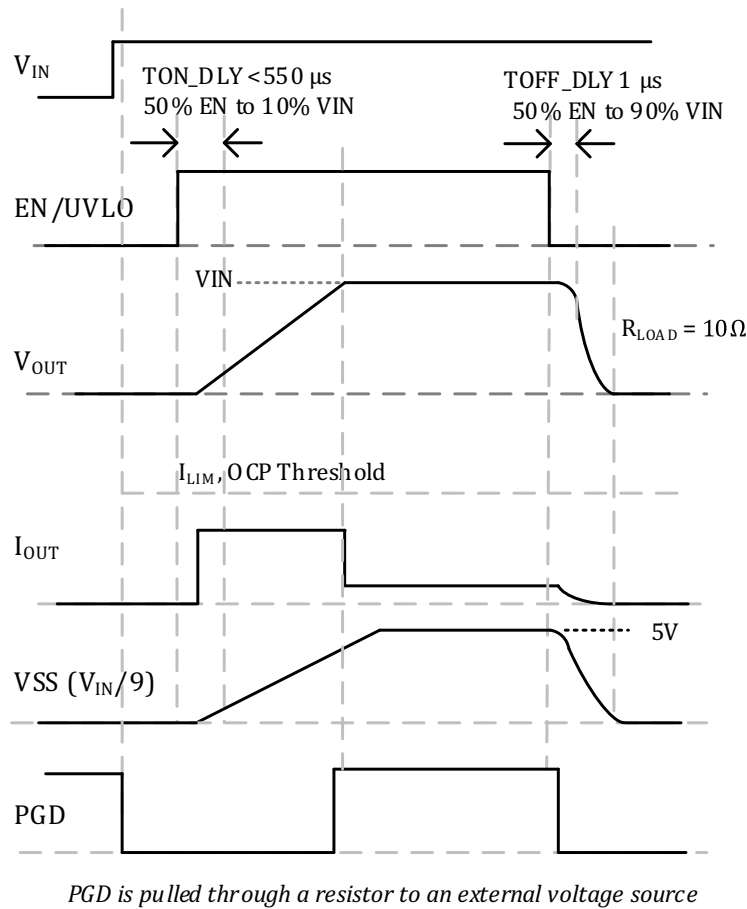
The inrush current is proportional to the load capacitance and rising slew rate. The following equation can be used to calculate the slew rate required to limit the inrush current ( $I_{INRUSH}$ ) for a given load capacitance ( $C_{OUT}$ ):

$$SR (V/ms) = \frac{I_{INRUSH} (mA)}{C_{OUT} (\mu F)}$$
$$T_{SS} = \frac{V_{IN}}{SR} = V_{IN} \times \frac{C_{OUT} (\mu F)}{I_{INRUSH} (mA)}$$

An external capacitor can be connected to the soft start (SS) pin to control the rising slew rate and lower the inrush current during turn-on. The output voltage follows the required  $C_{SS}$  capacitance to produce a given slew rate, which can be calculated using the following formula:

$$C_{SS} = \frac{(I_{SS} \times 9)}{SR}$$

The fastest output slew rate is achieved by leaving the soft start pin open.


**Fig. 37**

## CURRENT LIMIT SETTING

The SIP32433A and SIP32433B actively monitor the current flow through the switch and provide a quick response to over-current conditions by actively regulating the current to a set limit. The current limit is set by connecting a resistor between the  $I_{LIM}$  pin and GND.  $R_{SET}$  can be calculated by the following formula for a desired current limit:

$$SR \text{ (V/ms)} = \frac{I_{INRUSH} \text{ (mA)}}{C_{OUT} \text{ (}\mu\text{F)}}$$

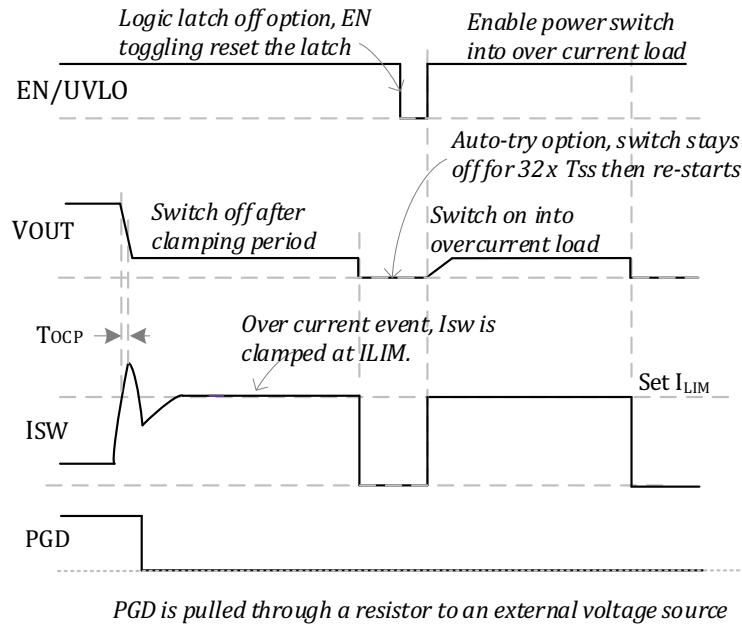
$$R_{SET} = \frac{0.6 \text{ V}}{I_{LIM}} \times 10\,300$$

When the load current exceeds the threshold ( $I_{LIM}$ ), the parts respond within 1  $\mu\text{s}$  (typ.) to turn off the switch and then regulate the switch gate voltage to limit the output current to the set  $I_{LIM}$  level. During this brief period before the over-current protection circuit is engaged, the parts will see a surge current, especially under a severe output short condition. The magnitude of the surge current developed during the period when the over-current protection is not engaged is determined by impedance in the loop from the input current source to ground and the response time. This impedance is the sum total of the current source impedance, the path resistance and inductance, and the load impedance.

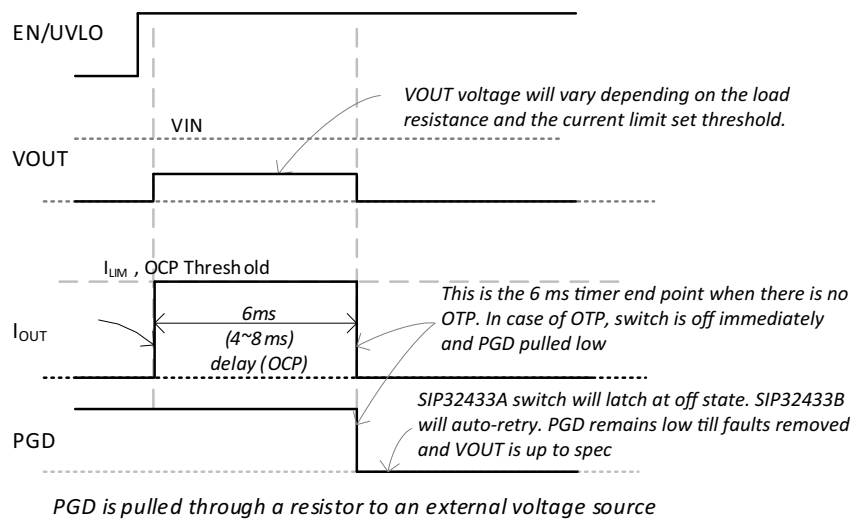
If the over-current condition persists for more than 6 ms / typ., the switch shuts off. When  $V_{OUT}$  falls below 95 % of  $V_{IN}$ , the PGD is pulled low. The device will exit current limiting when the load current falls below  $I_{LIM}$  before the end of the current limit period. The control circuit will increase the gate drive in the same manner as the soft start when the switch exits from the current limit mode.

The current limit mode could result in excessive power on the switch, which increases the  $T_J$  quickly. The SIP32433A and SIP32433B have OTP, providing an enhanced level of protection.

Once the device is off due to OCP or OTP faults, the SIP32433A stays in the latch-off state and the SIP32433B auto-retries after 32 times of the programmed soft start time. They can be reset by toggling  $V_{IN}$  or EN / UVLO.



**Fig. 38 - Over-Current Protection**



**Fig. 39 - Turn On Into Over-Current Load**



**True Reverse Current Blocking**

The  $I_{limit} / I_{mon}$  pin can also be used for current reporting. The output path should be of high impedance, to prevent any disruption to the current limit circuitry. 0.6 V output reflect 2 A current; 0.3 V represents 1 A.

The SIP32433A and SIP32433B feature TRCB (true reverse current blocking). When  $V_{OUT}$  is detected higher than  $V_{IN}$  by  $V_{RCB}$  (20 mV typ.) the switch is turned off. The TRCB response time  $t_{RCB}$  is 300 ns ( $V_{OUT} - V_{IN} = 100$  mV) and 3  $\mu$ s ( $V_{OUT} - V_{IN} = 3$  mV). TRCB is a non-latchable fault. Once  $V_{OUT}$  falls below the TRCB recovery threshold ( $V_{RCBR}$  20 mV typically), the switch will turn on without soft start procedure. The SIP32419B also blocks the current from  $V_{OUT}$  to  $V_{IN}$  when  $V_{IN}$  is short to GND. When the switch is disabled, current flow is blocked in both directions.

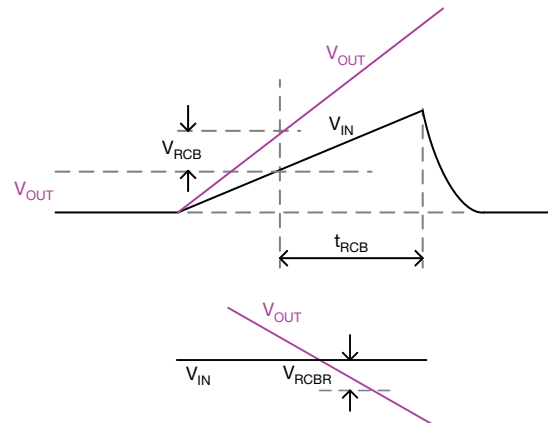
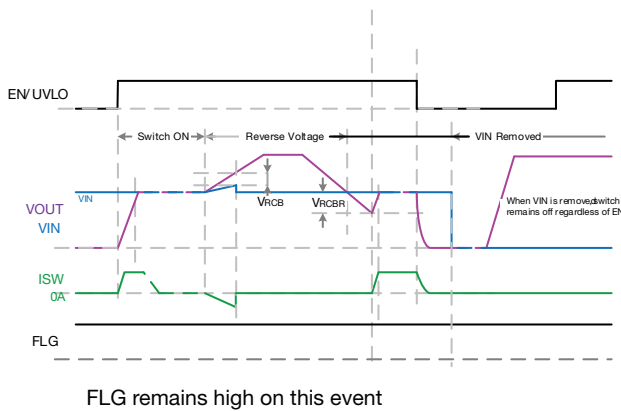


Fig. 41 - Reverse Protection



FLG remains high on this event

Fig. 40 - Reverse Protection

**OTP, OVER-TEMPERATURE PROTECTION**

Over-temperature protection turns off the power switch when the die temperature reaches the OTP threshold of 165 °C. The hysteresis is 45 °C. When the die temperature drops below 120 °C, it is allowed to turn on again.

**PGD, POWER GOOD REPORTING**

PGD is an open drain output. A pull-up resistor must be connected pulling to 3 V or 5 V. It is asserted low when  $V_{OUT}$  is below 95 % of  $V_{IN}$ , or an over-current, over-voltage, or over-temperature fault condition occurs.

**INPUT CAPACITOR**

While bypass capacitors at the input pins are not required, a 2.2  $\mu$ F or larger capacitors for  $C_{IN}$  is recommended in almost all applications. The bypass capacitors should be placed as physically close to the device's input pins and ground to be effective to minimize transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries. For hot-plug applications, where input path inductance is negligible, this input capacitor can be minimized or eliminated.

**OUTPUT CAPACITOR**

The SIP32433A and SIP32433B do not require an output capacitor for proper operation. A proper value  $C_{OUT}$  is recommended to accommodate load transient per circuit design requirements. There are no ESR or capacitor type requirements.

Protection

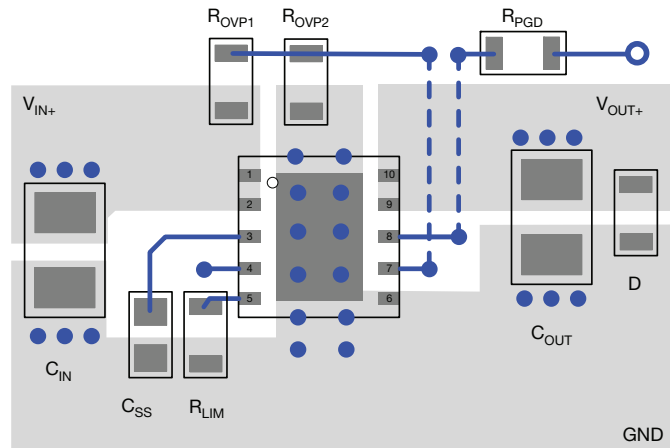
**LAYOUT GUIDELINES**

The SIP32433A and SIP32433B are protection switches designed to maintain a constant output load current upon over-current fault. Optimized layout with efficient heat sinking is critical. It is recommended to put as much copper as possible to the devices' central exposed pad which is connected to ground. Connect all ground planes with all possible thermal VIAs.

The circuit setting components should be laid close to their connection pins. The components include current limit setting resistor, soft start setting capacitor, and resistors connected to EN / UVLO and OVP pins.

Protection devices such as input TVS or output Schottky diodes must be located close the pins to be protected and routed with short traces to reduce inductance.

Below is a layout example.



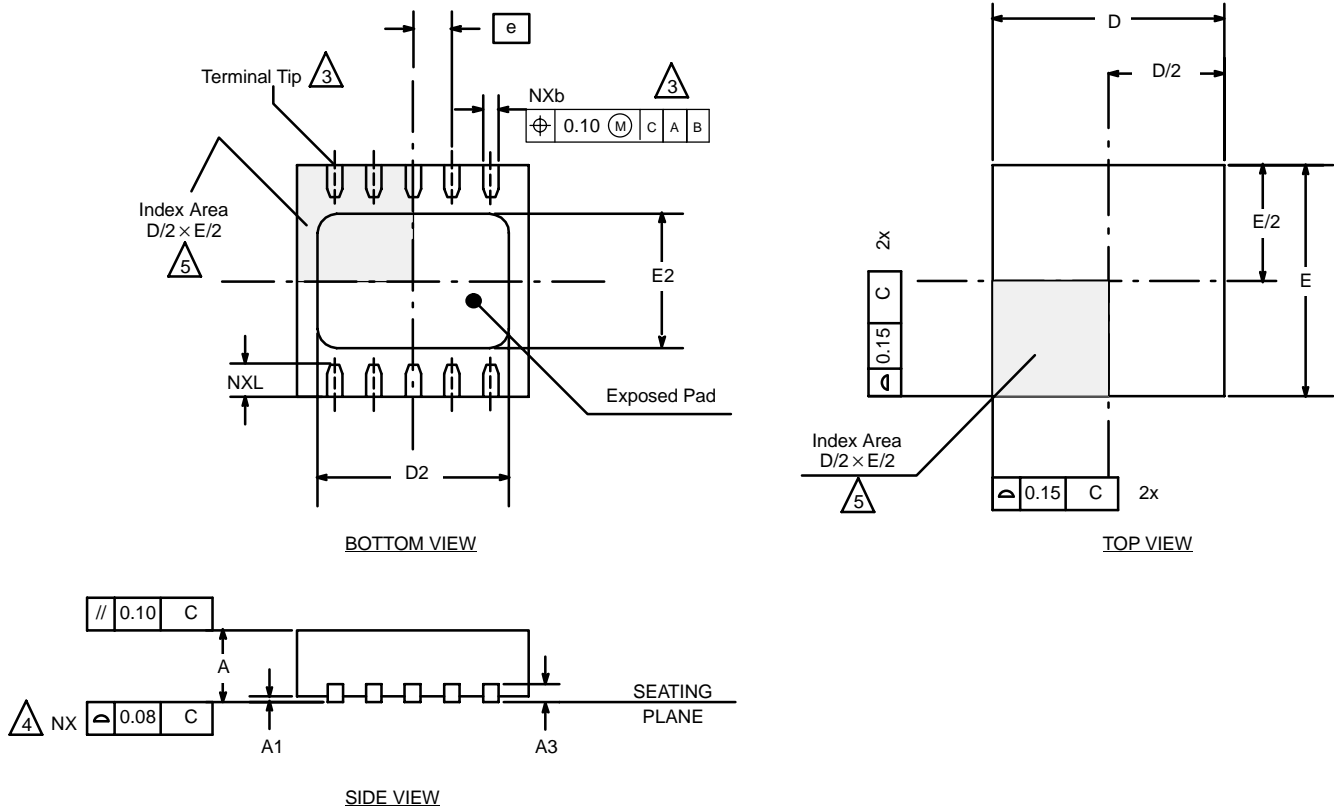
**Fig. 42**



<b>PRODUCT SUMMARY</b>		
Part number	SIP32433A	SIP32433B
Description	3.5 A, 78 mΩ, 2.8 V to 23 V, programmable OVP and current limit, active reverse blocking, latch-off on fault	3.5 A, 78 mΩ, 2.8 V to 23 V, programmable OVP and current limit, active reverse blocking, auto retry on fault
Configuration	Single	Single
Slew rate time (μs)	Adjustable	Adjustable
On delay time (μs)	190	190
Input voltage min. (V)	2.8	2.8
Input voltage max. (V)	28	28
On-resistance at input voltage min. (mΩ)	78	78
On-resistance at input voltage max. (mΩ)	78	78
Quiescent current at input voltage min. (μA)	180	180
Quiescent current at input voltage max. (μA)	250	250
Output discharge (yes / no)	N	N
Reverse blocking (yes / no)	Y	Y
Continuous current (A)	3.5	3.5
Package type	DFN33-10L	DFN33-10L
Package size (W, L, H) (mm)	3.0 x 3.0 x 0.9	3.0 x 3.0 x 0.9
Status code	2	2
Product type	Slew rate, current limit	Slew Rate Current Limit
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

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### DFN-10 LEAD (3 X 3)



**NOTES:**

- All dimensions are in millimeters and inches.
- N is the total number of terminals.
- (3) Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
- (4) Coplanarity applies to the exposed heat sink slug as well as the terminal.
- (5) The pin #1 identifier may be either a mold or marked feature, it must be located within the zone indicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.80	0.90	1.00	0.031	0.035	0.039
<b>A1</b>	0.00	0.02	0.05	0.000	0.001	0.002
<b>A3</b>	0.20 BSC			0.008 BSC		
<b>b</b>	0.18	0.23	0.30	0.007	0.009	0.012
<b>D</b>	3.00 BSC			0.118 BSC		
<b>D2</b>	2.20	2.38	2.48	0.087	0.094	0.098
<b>E</b>	3.00 BSC			0.118 BSC		
<b>E2</b>	1.49	1.64	1.74	0.059	0.065	0.069
<b>e</b>	0.50 BSC			0.020 BSC		
<b>L</b>	0.30	0.40	0.50	0.012	0.016	0.020

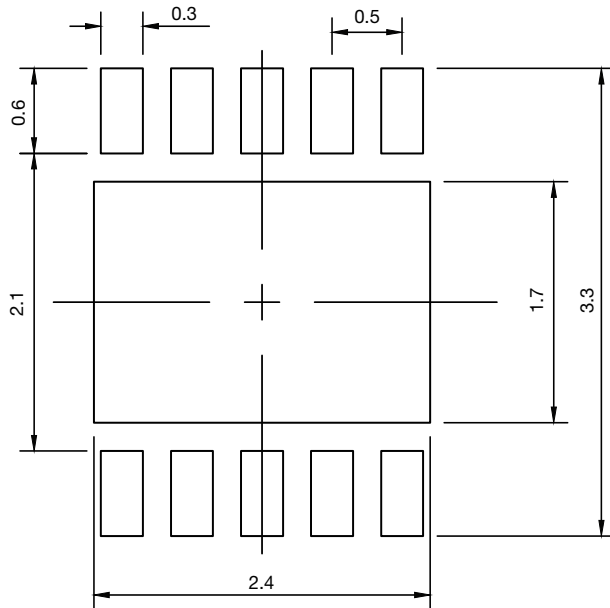
\*Use millimeters as the primary measurement.

ECN: S-42134—Rev. A, 29-Nov-04  
DWG: 5943

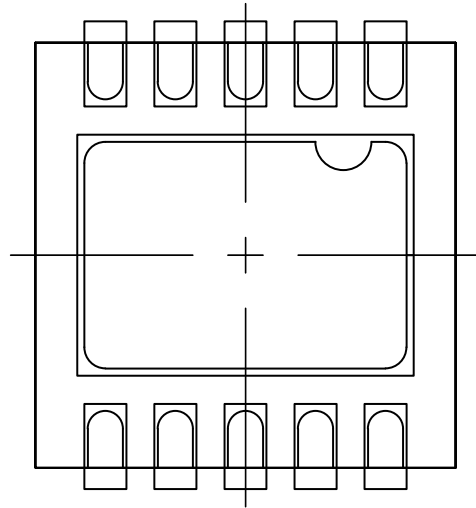


## Recommended Minimum PAD for DFN10 3 mm x 3 mm

Recommended Land Pattern



Recommended Land Pattern vs. Case Outline



Note: Dimension are in millimeters

ECN: S22-0379-Rev. A, 02-May-2022  
DWG: 3008



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