N- and P-Channel 20 V (D-S) MOSFET

DESCRIPTION

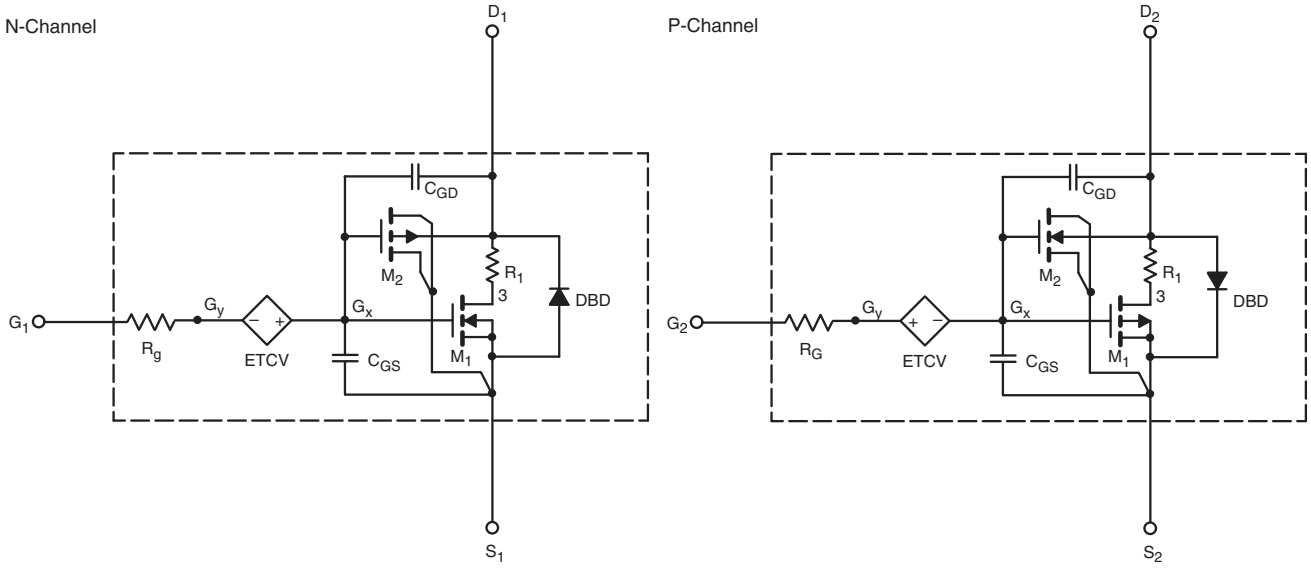
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

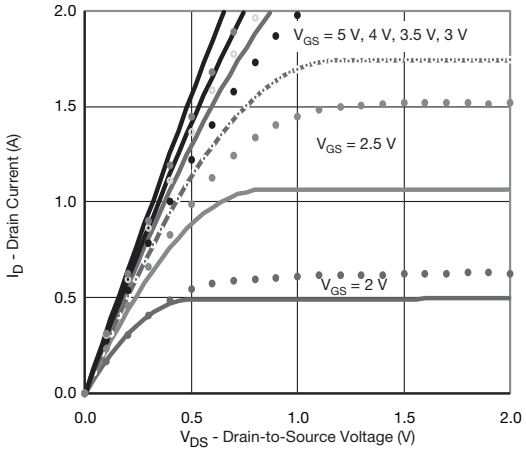
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.90	-	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	0.93	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.7 A	N-Ch	0.325	0.325	Ω
		V_{GS} = - 4.5 V, I_D = - 0.4 A	P-Ch	0.74	0.071	
		V_{GS} = 2.5 V, I_D = 0.4 A	N-Ch	0.458	0.462	
		V_{GS} = - 2.5 V, I_D = - 0.2 A	P-Ch	1.15	1.23	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 0.7 A	N-Ch	1.2	1.5	S
		V_{DS} = - 15 V, I_D = - 0.5 A	P-Ch	0.81	0.80	
Diode Forward Voltage[b]	V_{SD}	I_S = - 0.4 A, V_{GS} = 0 V	N-Ch	0.83	0.81	V
			P-Ch	0.86	0.83	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	37	38	pF
			P-Ch	43	43	
Output Capacitance	C_{oss}		N-Ch	14	14	
			P-Ch	16	16	
Reverse Transfer Capacitance	C_{rss}		N-Ch	5.5	6	
			P-Ch	9.6	10	
Total Gate Charge	Q_g	V_{GS} = 10 V, V_{DS} = 10 V, I_D = 0.7 A	N-Ch	0.7	1.2	nC
		V_{GS} = - 10 V, V_{DS} = - 10 V, I_D = - 0.5 A	P-Ch	0.9	1.9	
		N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.5 A P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 0.4 A	N-Ch	0.34	0.55	
			P-Ch	0.44	0.95	
Gate-Source Charge	Q_{gs}		N-Ch	0.15	0.15	
			P-Ch	0.25	0.25	
Gate-Drain Charge	Q_{gd}		N-Ch	0.15	0.15	
			P-Ch	0.25	0.25	

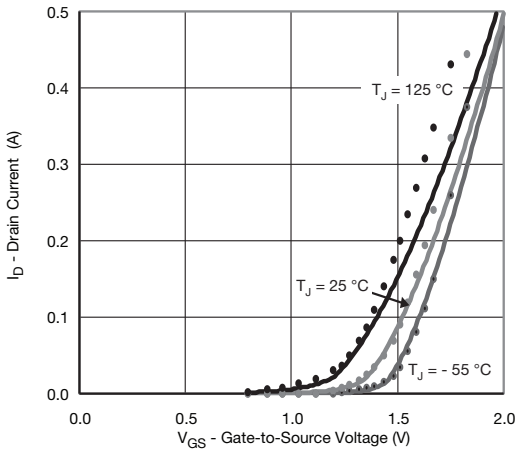
Notes

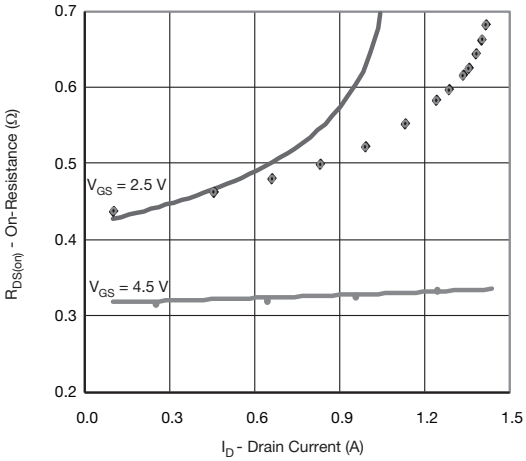
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

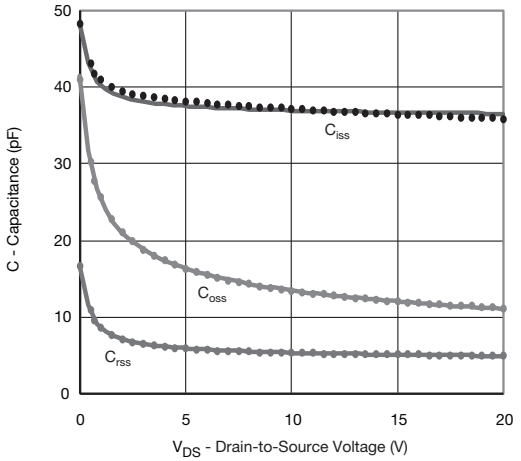
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

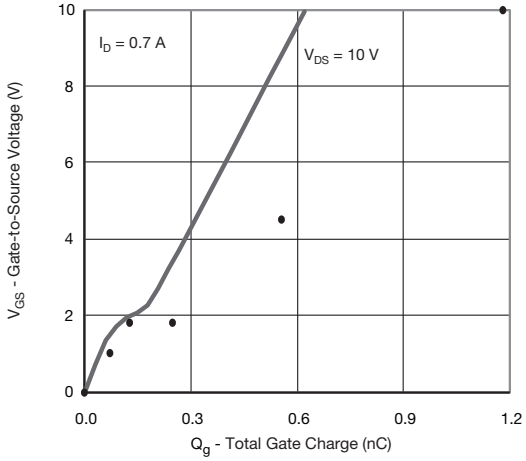
N-Channel MOSFET

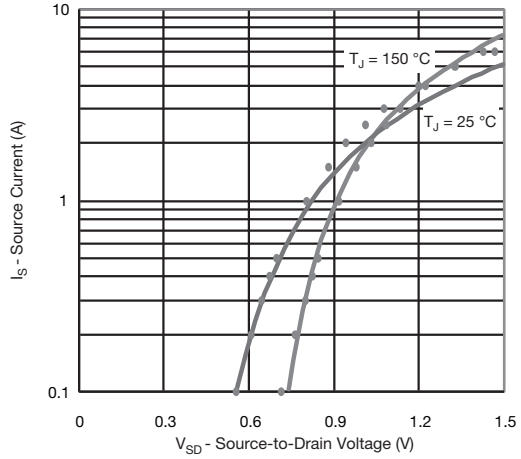










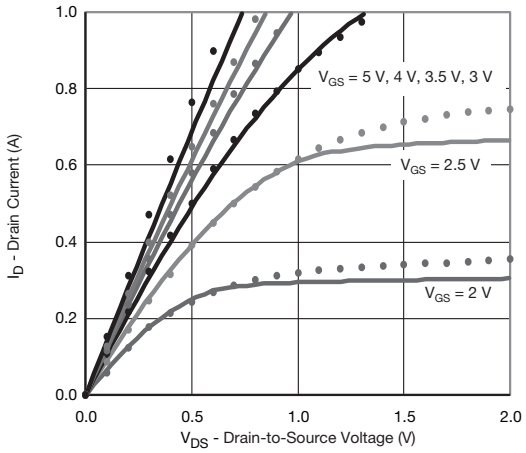


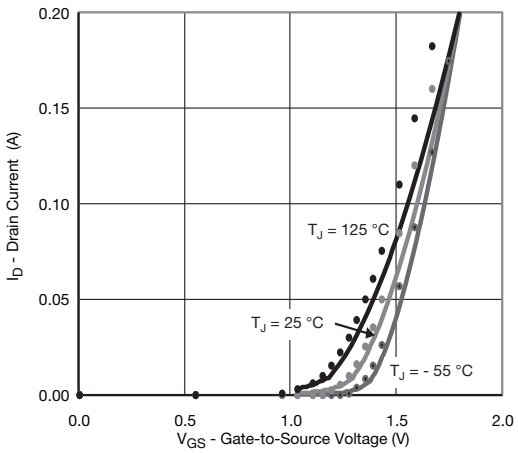
Note

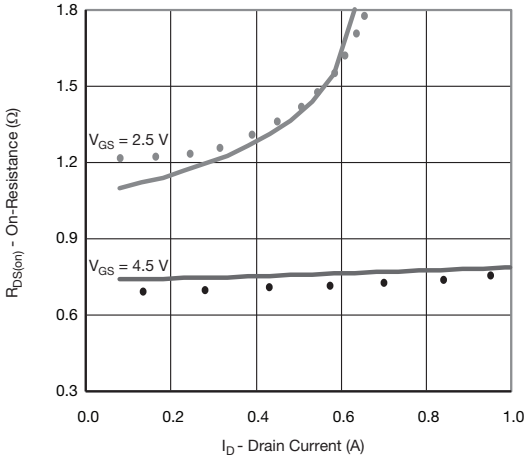
- Dots and squares represent measured data.

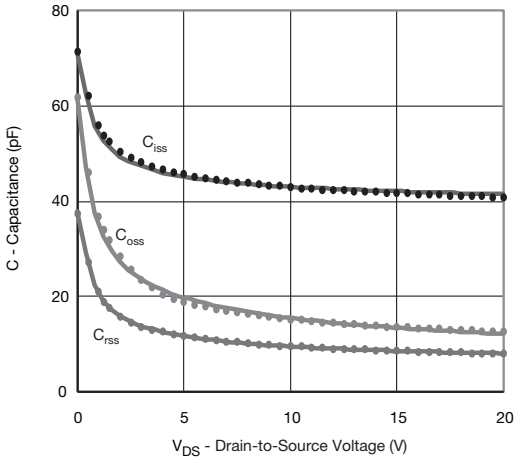
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

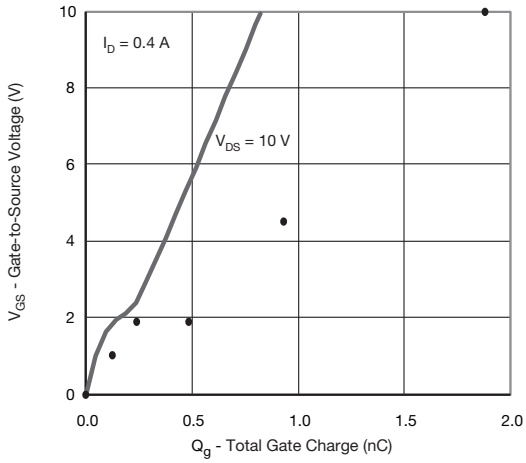
P-Channel MOSFET

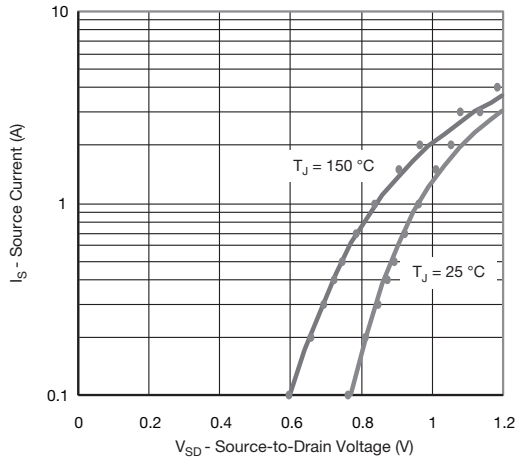












Note

- Dots and squares represent measured data.

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