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# Automotive N-Channel 20 V (D-S) 175 °C MOSFET

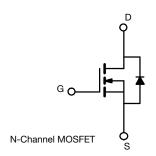
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	20				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0035				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0045				
I <sub>D</sub> (A)	100				
Configuration	Single				
Package	TO-252				

### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- AEC-Q101 qualified d
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912







<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		$V_{DS}$	20	V	
Gate-Source Voltage		$V_{GS}$	± 20	V	
Continuous Drain Current	$T_C = 25  ^{\circ}C^{a}$	L	100		
	T <sub>C</sub> = 125 °C	l <sub>D</sub>	65		
Continuous Source Current (Diode Conduction)		Is	75	Α	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	300			
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	45		
Single Pulse Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	101	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	83	W	
	T <sub>C</sub> = 125 °C		27	VV	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount c	$R_{thJA}$	50	°C/W		
Junction-to-Case (Drain)		$R_{thJC}$	1.8	C/VV		

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	_					I.	·	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		20	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2.0	2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, T <sub>J</sub> = 175 °C	=	-	250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.0020	0.0035	Ω	
Drain-Source On-State Resistance a	Ь	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	=	-	0.0050		
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	-	0.0058		
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	-	0.0030	0.0045		
Forward Transconductance b	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		=	186	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	4300	5500	pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 10 \text{ V}, f = 1 \text{ MHz}$	-	1350	1700		
Reverse Transfer Capacitance	C <sub>rss</sub>			1	585	800		
Total Gate Charge <sup>c</sup>	Qg			-	70	110		
Gate-Source Charge c	$Q_{gs}$	$V_{GS} = 10 \text{ V}$	$V_{DS} = 10 \text{ V}, I_{D} = 50 \text{ A}$	-	21	-	nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	11	=.		
Gate Resistance	$R_g$	f = 1 MHz		1.1	2.3	3.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 0.2 \Omega$ $I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		-	5	10	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	38	60		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	15	25		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	300	Α	
Forward Voltage	$V_{SD}$	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		-	0.86	1.2	V	

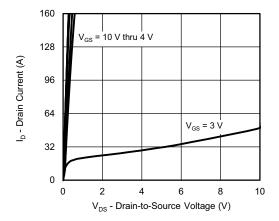
#### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

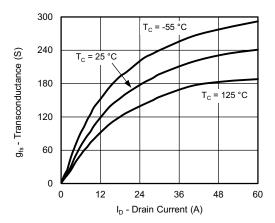
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



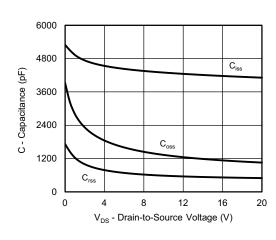
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



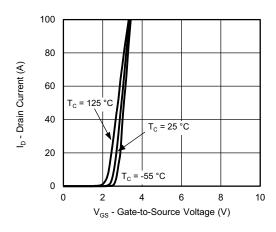
#### **Output Characteristics**



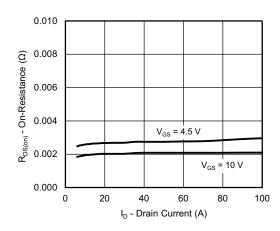
### Transconductance



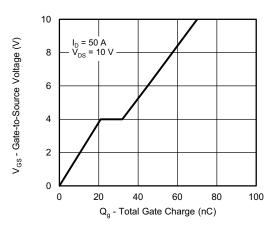
Capacitance



#### **Transfer Characteristics**



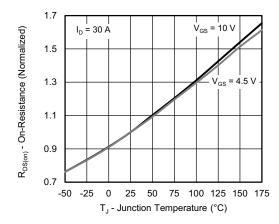
## On-Resistance vs. Drain Current



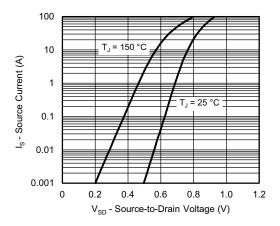
**Gate Charge** 



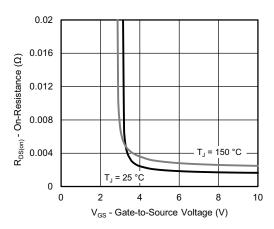
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



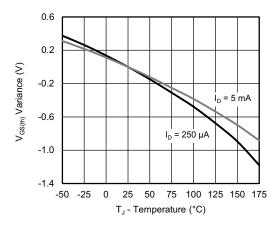
On-Resistance vs. Junction Temperature



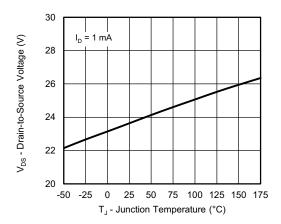
**Source Drain Diode Forward Voltage** 



On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

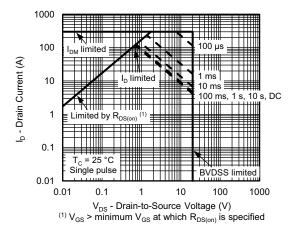


Breakdown Voltage vs. Junction Temperature

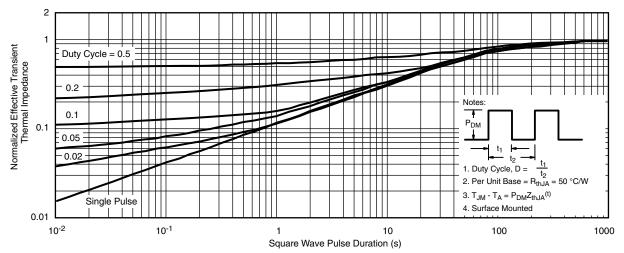
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## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



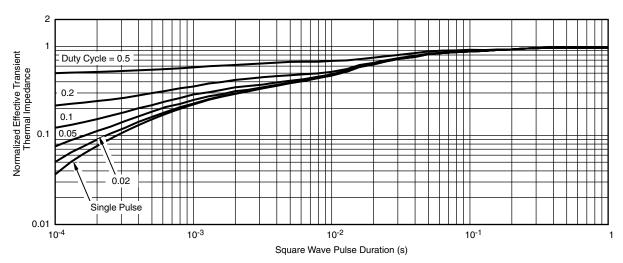
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

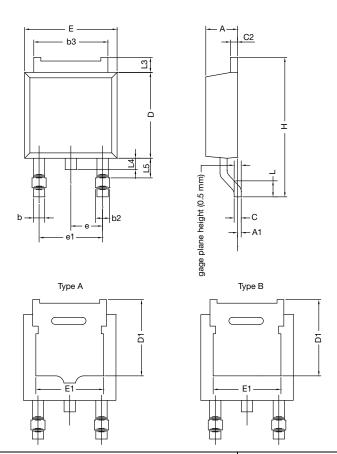
#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?63527">www.vishay.com/ppg?63527</a>.



## **TO-252AA Case Outline**



DIM.	MILLIM	IETERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	=	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	=	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	

# ECN: T24-0298-Rev. B, 29-Jul-2024 DWG: 6019

#### Notes

- Dimension L3 is for reference only
- Dimension D1 and E1 on type A and B is the same



## **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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