

## P-Channel 20 V (D-S) MOSFET

### DESCRIPTION

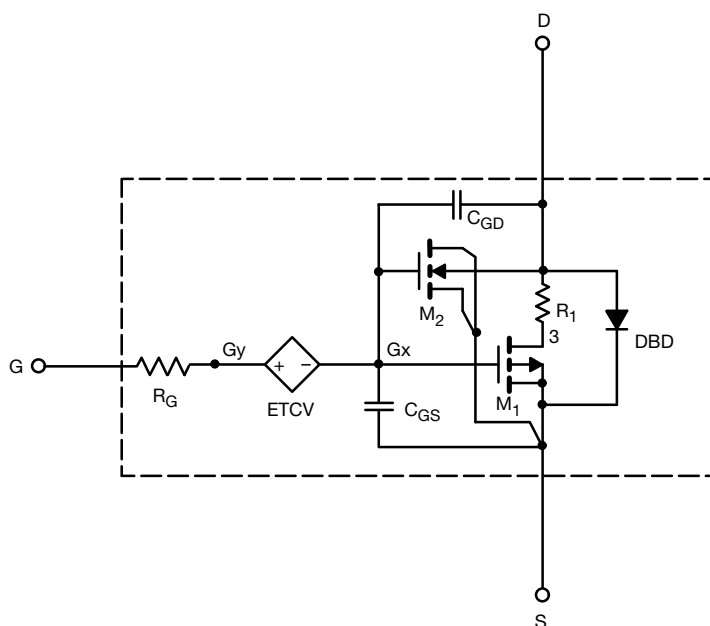
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



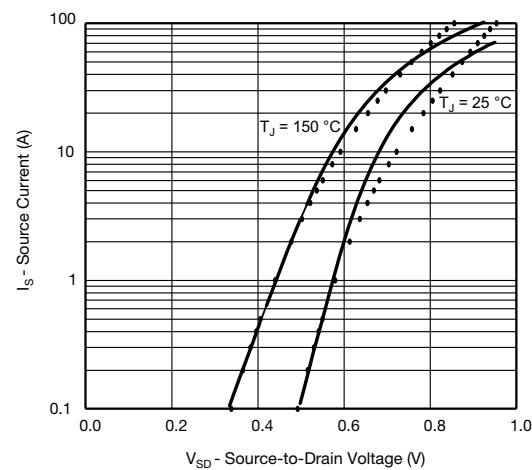
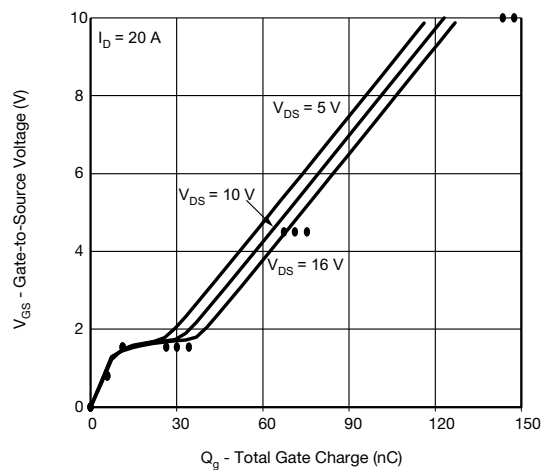
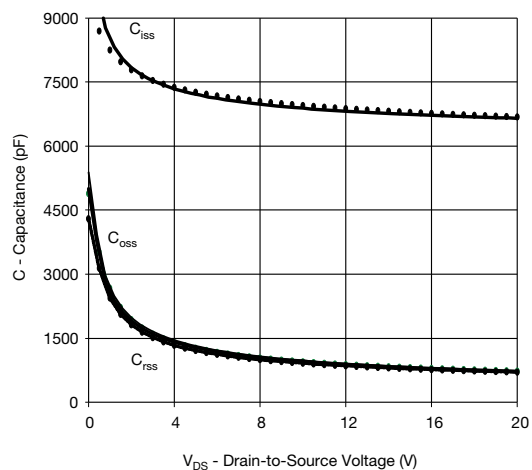
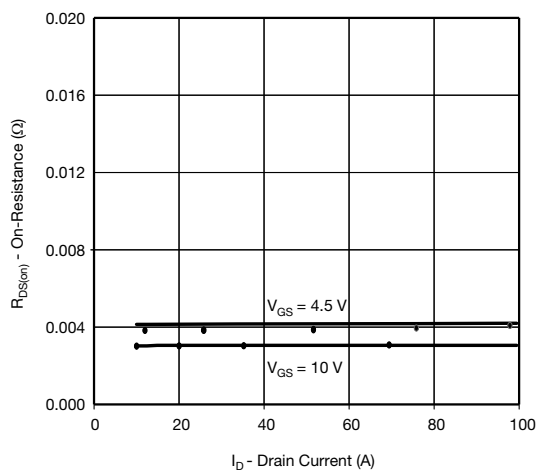
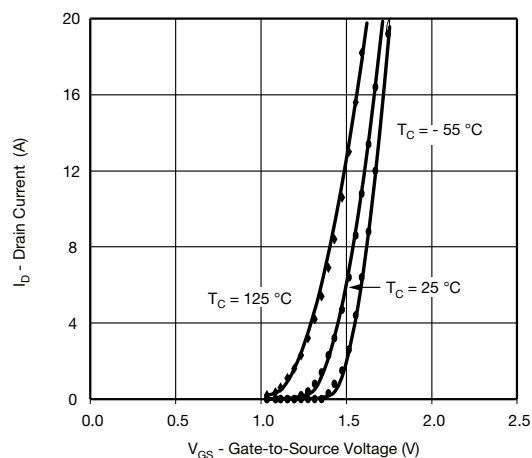
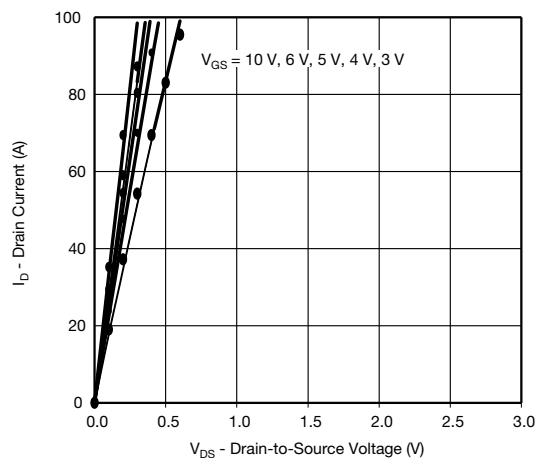
| SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) |              |  |                |               |          |
|---|--------------|--|----------------|---------------|----------|
| PARAMETER   | SYMBOL       | TEST CONDITIONS  | SIMULATED DATA | MEASURED DATA | UNIT     |
| <b>Static</b>   |              |  |                |               |          |
| Gate Threshold Voltage  | $V_{GS(th)}$ | $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{A}$                                | 0.8            | -             | V        |
| Drain-Source On-State Resistance <sup>a</sup>                       | $R_{DS(on)}$ | $V_{GS} = -10\ \text{V}$ , $I_D = -20\ \text{A}$                             | 0.0030         | 0.0030        | $\Omega$ |
|   |              | $V_{GS} = -4.5\ \text{V}$ , $I_D = -15\ \text{A}$                            | 0.0041         | 0.0039        |          |
| Forward Transconductance <sup>a</sup>                               | $g_{fs}$     | $V_{DS} = -15\ \text{V}$ , $I_D = -20\ \text{A}$                             | 85             | 90            | S        |
| Diode Forward Voltage   | $V_{SD}$     | $I_S = -10\ \text{A}$  | -0.71          | -0.75         | V        |
| <b>Dynamic<sup>b</sup></b>  |              |  |                |               |          |
| Input Capacitance   | $C_{iss}$    | $V_{DS} = -10\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$      | 6890           | 6950          | pF       |
| Output Capacitance  | $C_{oss}$    |  | 979            | 914           |          |
| Reverse Transfer Capacitance  | $C_{rss}$    |  | 955            | 947           |          |
| Total Gate Charge   | $Q_g$        | $V_{DS} = -10\ \text{V}$ , $V_{GS} = -10\ \text{V}$ , $I_D = -20\ \text{A}$  | 125            | 150           | nC       |
|   |              | $V_{DS} = -10\ \text{V}$ , $V_{GS} = -4.5\ \text{V}$ , $I_D = -20\ \text{A}$ | 63             | 72            |          |
| Gate-Source Charge  | $Q_{gs}$     |  | 12             | 12            |          |
| Gate-Drain Charge   | $Q_{gd}$     |  | 19             | 19            |          |

**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$ .  
b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.