

## N- and P-Channel 30 V (D-S) MOSFET

### DESCRIPTION

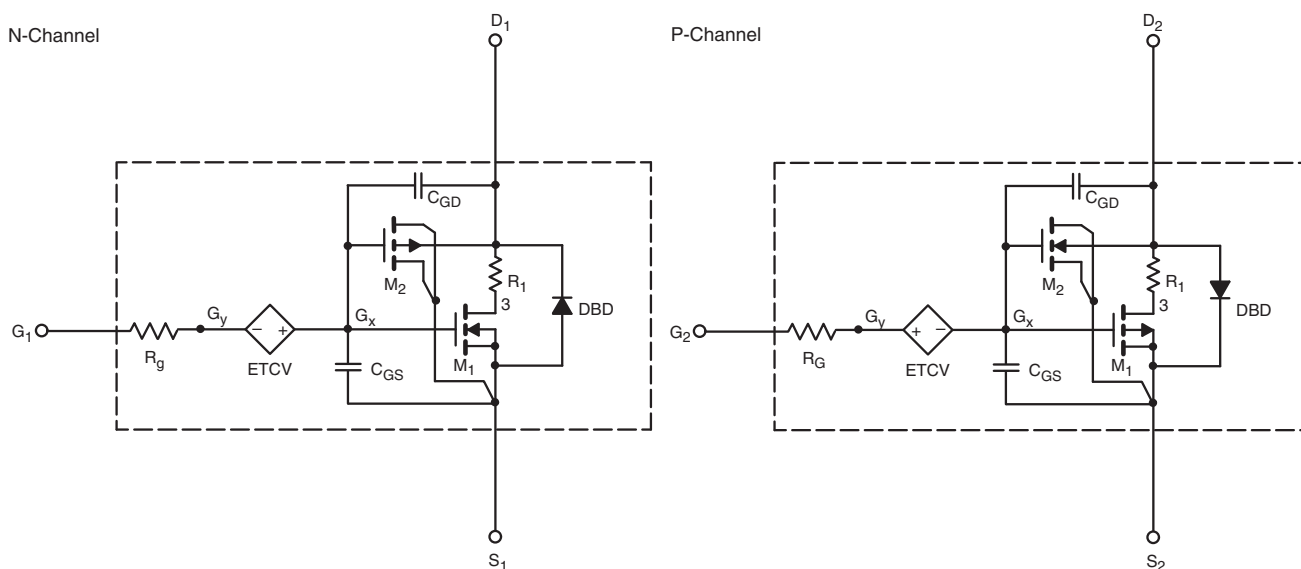
The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	2	-	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	P-Ch	2.4	-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.6 A	N-Ch	0.322	0.323	Ω
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 0.4 A	P-Ch	0.740	0.740	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.1 A	N-Ch	0.458	0.437	
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 0.1 A	P-Ch	1.4	1.4	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.6 A	N-Ch	1.4	1.2	S
		V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 0.4 A	P-Ch	0.71	0.60	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 0.5 A, V <sub>GS</sub> = 0 V	N-Ch	0.86	0.80	V
		I <sub>S</sub> = - 0.4 A, V <sub>GS</sub> = 0 V	P-Ch	- 0.89	- 0.80	
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz  P-Channel V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch	28	28	pF
Output Capacitance	C <sub>oss</sub>		P-Ch	34	34	
			N-Ch	10	10	
			P-Ch	12	12	
			Reverse Transfer Capacitance	C <sub>rss</sub>	N-Ch	
P-Ch	7				7	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.6 A	N-Ch	0.53	1	nC
		V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 0.4 A	P-Ch	0.72	1.5	
		N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.6 A	N-Ch	0.29	0.55	
			P-Ch	0.40	0.80	
Gate-Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 0.4 A	N-Ch	0.20	0.20	
			P-Ch	0.40	0.40	
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch	0.20	0.20	
			P-Ch	0.35	0.35	

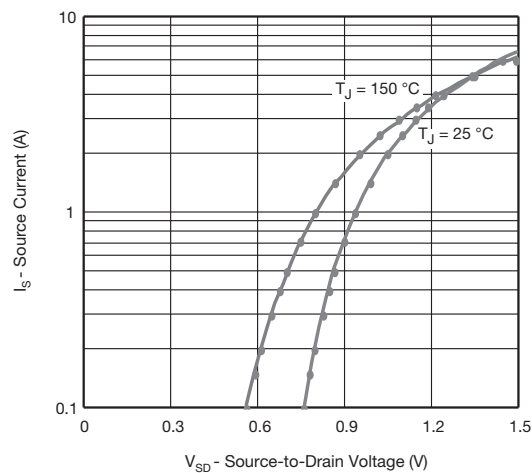
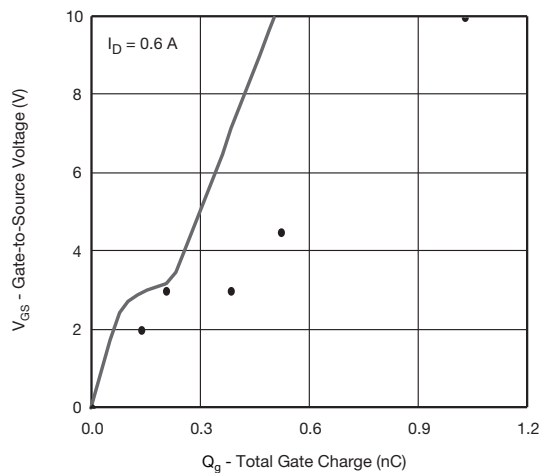
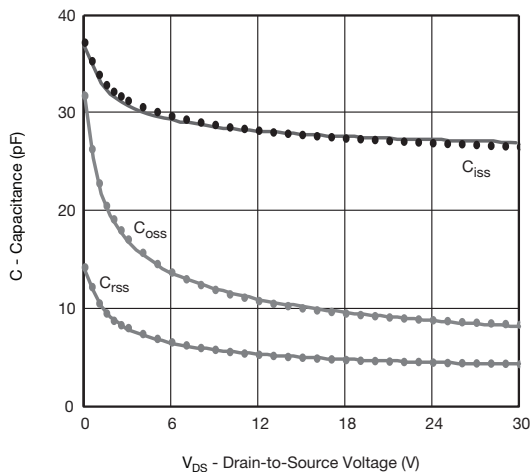
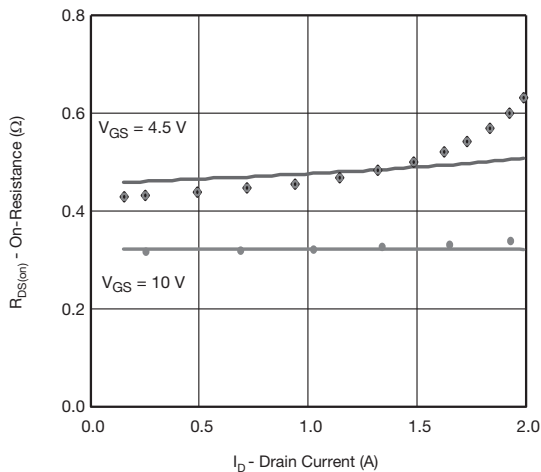
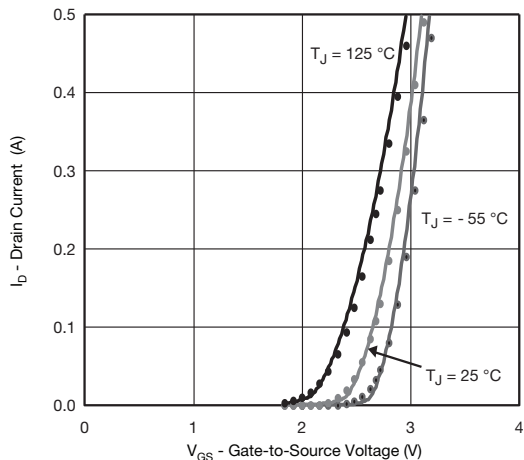
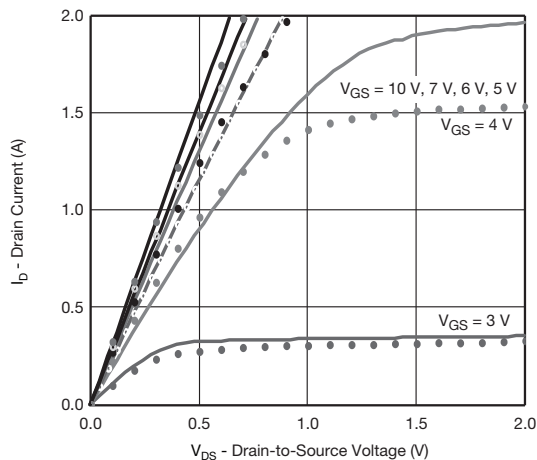
**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$ .  
b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

### N-Channel MOSFET



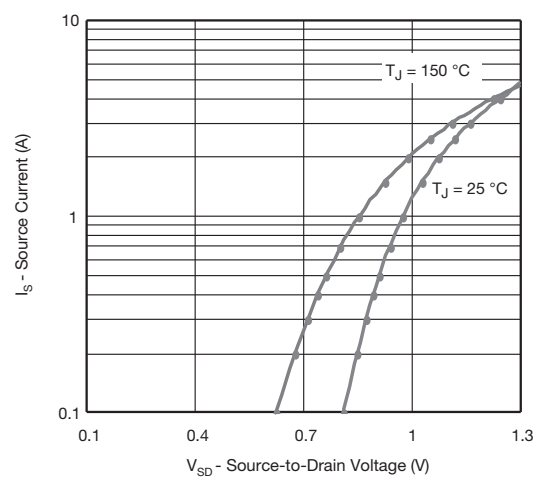
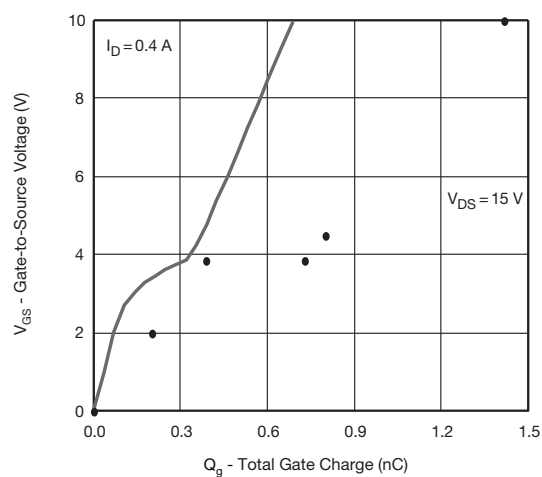
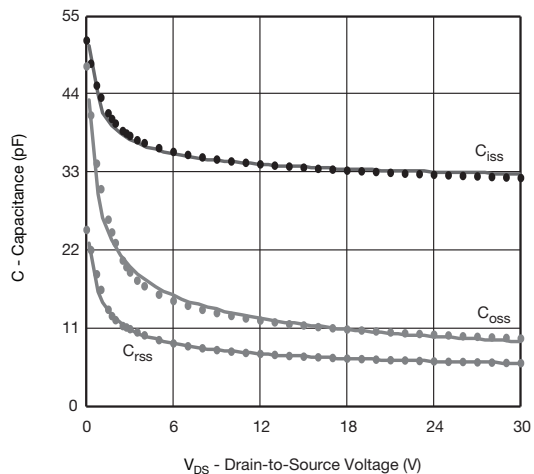
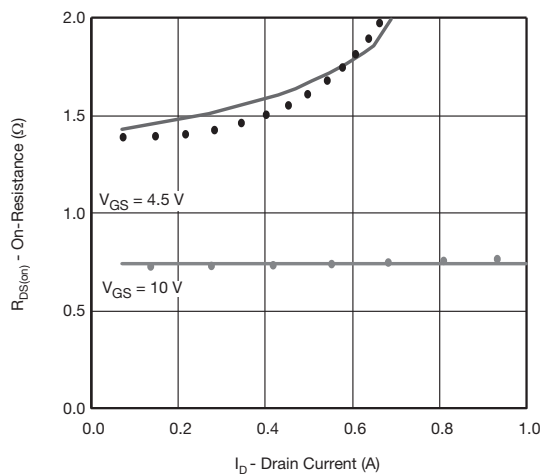
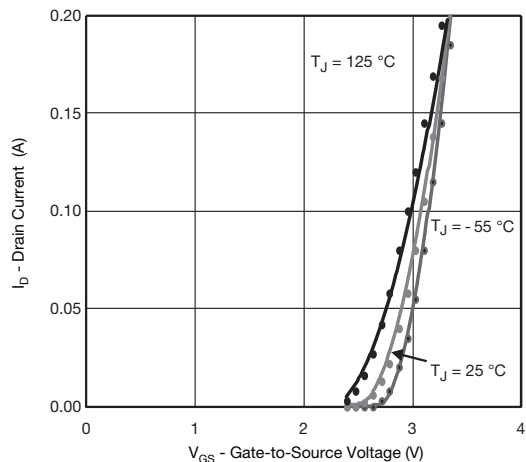
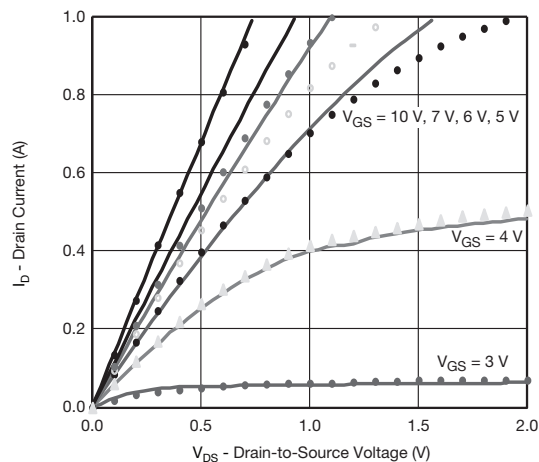
#### Note

- Dots and squares represent measured data.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

### P-Channel MOSFET



#### Note

- Dots and squares represent measured data.