

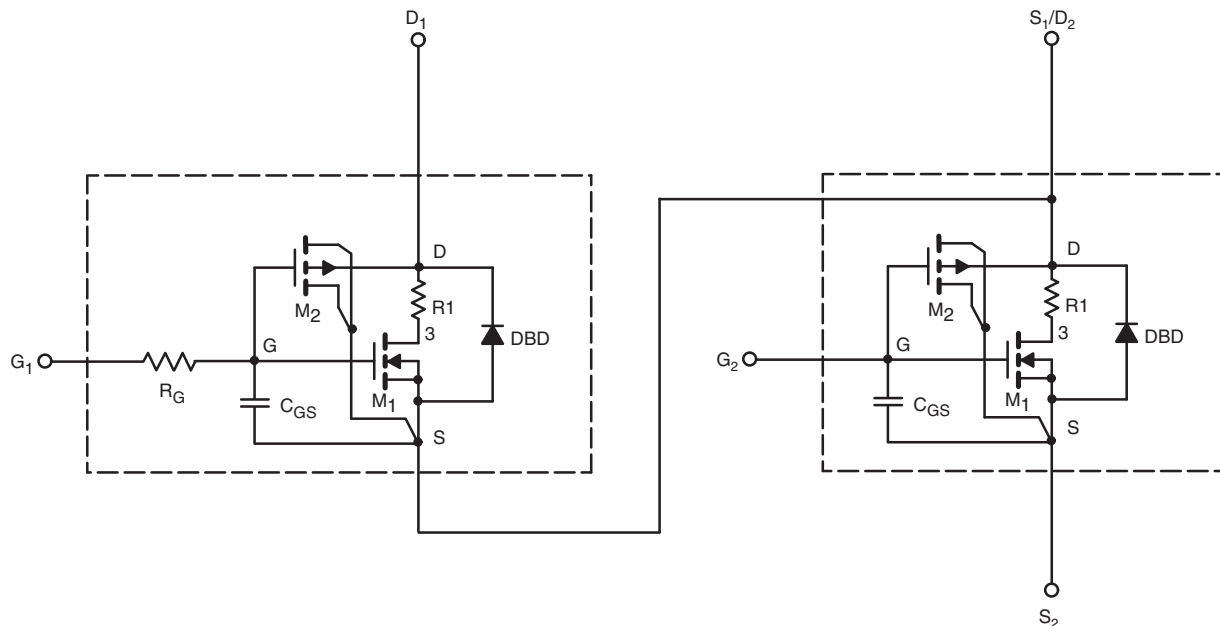
## Dual N-Channel 30 V (D-S) MOSFET

### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	Ch-1	1.5	-	V	
			Ch-2	1.5	-		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	Ch-1	0.0078	0.0075	Ω	
			Ch-2	0.0038	0.0038		
			V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 13 A	Ch-1	0.0100		0.0105
				Ch-2	0.0048		0.0048
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	Ch-1	42	48	S	
			Ch-2	69	85		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	Ch-1	0.79	0.80	V	
			Ch-2	0.38	0.38		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	C <sub>iss</sub>	Channel-1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Ch-1	827	830	pF	
			Ch-2	1950	1980		
Output Capacitance	C <sub>oss</sub>	Channel-2 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Ch-1	190	185		
			Ch-2	466	455		
Reverse Transfer Capacitance	C <sub>rss</sub>	Channel-1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Ch-1	81	80		
			Ch-2	156	165		
Total Gate Charge	Q <sub>g</sub>	Channel-1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	Ch-1	15	15.6	nC	
			Ch-2	33	36		
		Channel-2 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	Ch-1	7.4	7.7		
			Ch-2	17	17		
Gate-Source Charge	Q <sub>gs</sub>	Channel-1 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A	Ch-1	2.6	2.6		
			Ch-2	5.7	5.7		
Gate-Drain Charge	Q <sub>gd</sub>	Channel-2 V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	Ch-1	3	3		
			Ch-2	5	5		

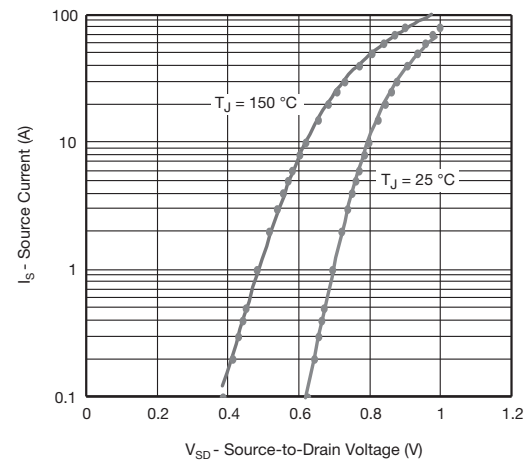
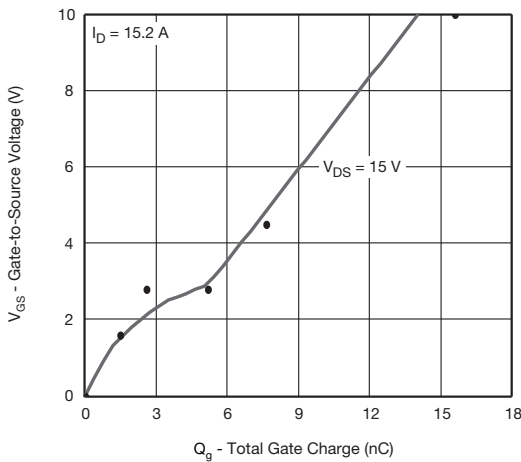
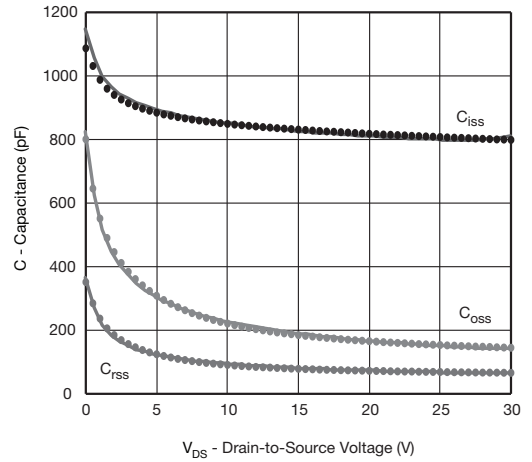
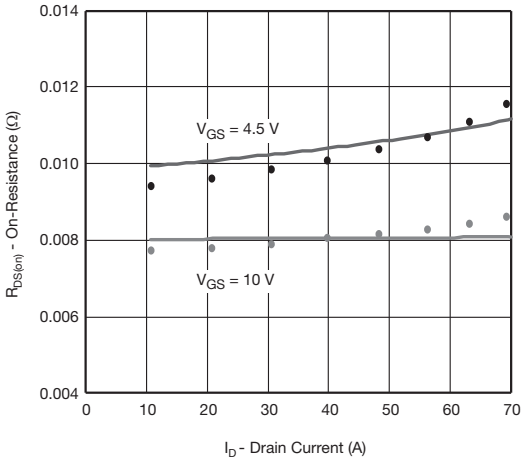
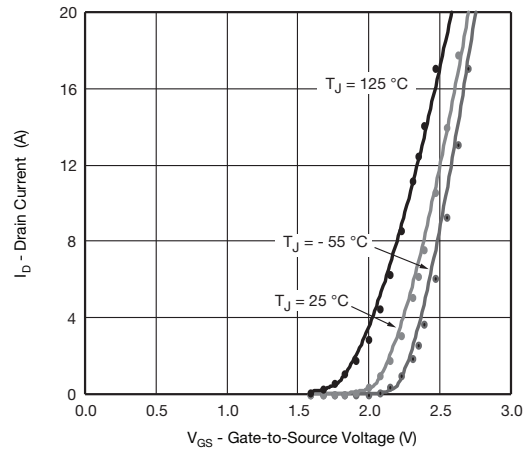
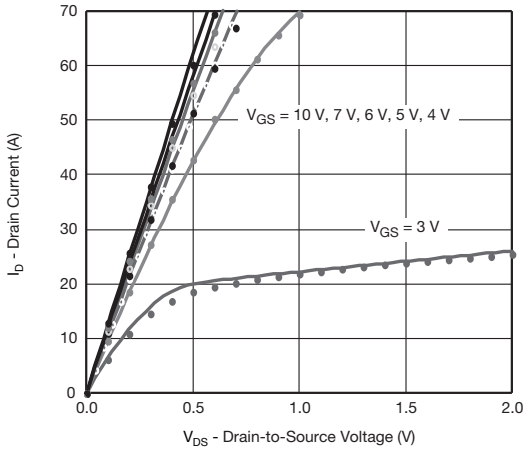
**Notes**

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

### Channel-1 MOSFET



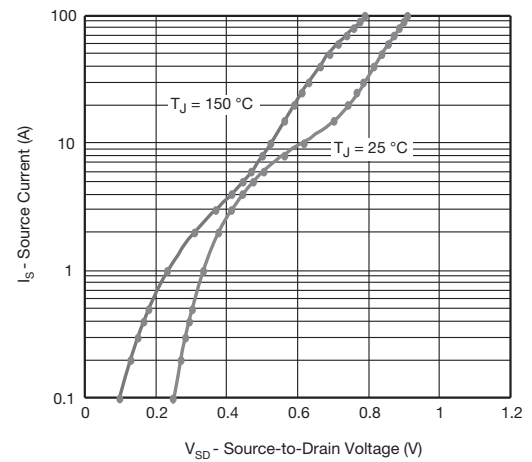
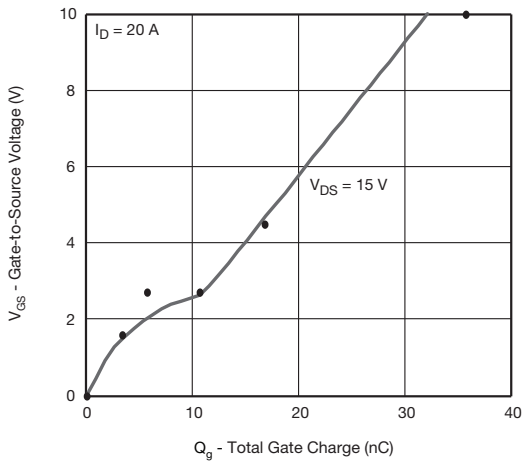
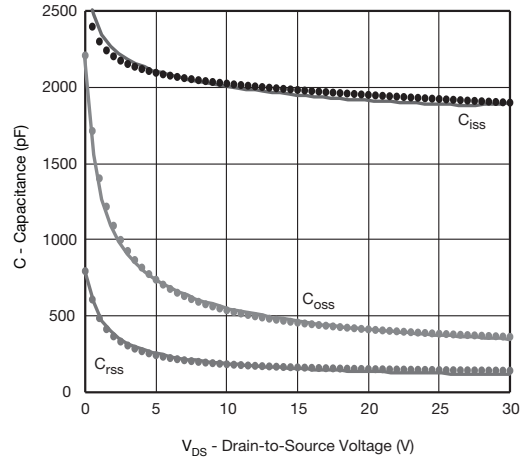
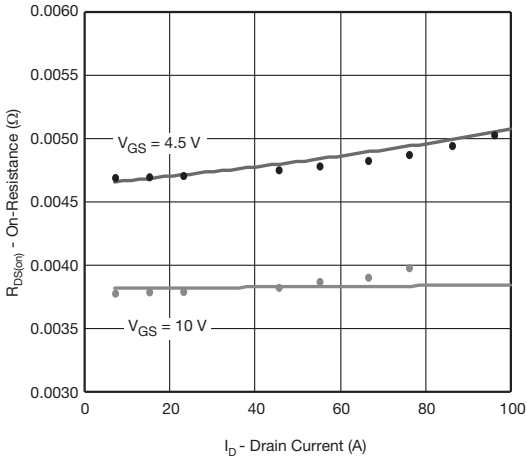
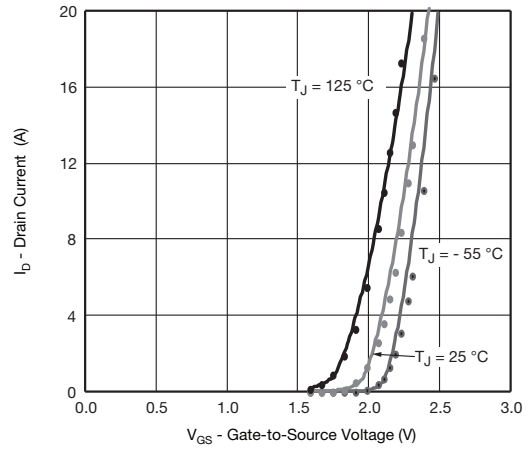
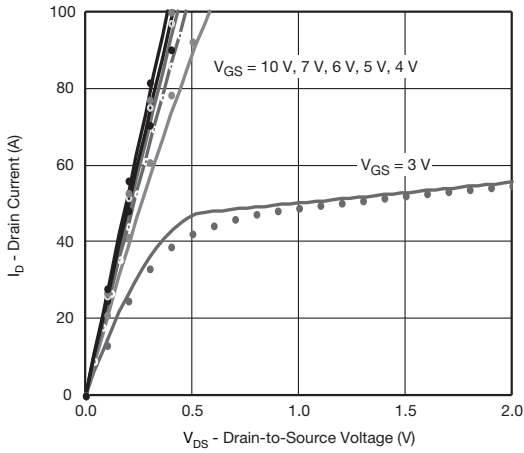
### Note

- Dots and squares represent measured data.



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

### Channel-2 MOSFET



#### Note

- Dots and squares represent measured data.



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