Dual N-Channel 30 V (D-S) MOSFET

DESCRIPTION

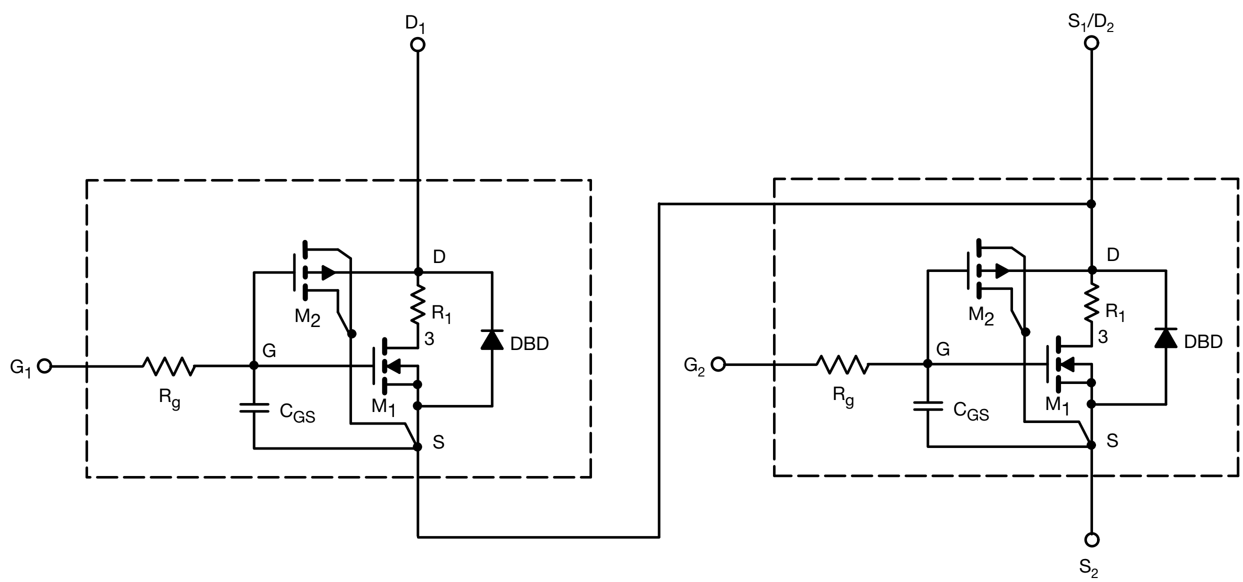
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	Ch-1	1.6	-	V
			Ch-2	1.5	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 9.8 A	Ch-1	0.020	0.020	Ω
		V_{GS} = 10 V, I_D = 15 A	Ch-2	0.009	0.009	
		V_{GS} = 4.5 V, I_D = 8.5 A	Ch-1	0.0265	0.0265	
		V_{GS} = 4.5 V, I_D = 12 A	Ch-2	0.0150	0.0135	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 9.8 A	Ch-1	26	30	S
		V_{DS} = 10 V, I_D = 15 A	Ch-2	25	30	
Diode Forward Voltage[a]	V_{SD}	I_S = 8 A, V_{GS} = 0 V	Ch-1	0.84	0.84	V
		I_S = 10 A, V_{GS} = 0 V	Ch-2	0.82	0.82	
Dynamic[b]						
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz; Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	397	400	pF
			Ch-2	716	730	
Output Capacitance	C_{oss}		Ch-1	127	125	
			Ch-2	157	155	
Reverse Transfer Capacitance	C_{rss}		Ch-1	24	25	
			Ch-2	66	65	
Total Gate Charge	Q_g	Channel-1 V_{DS} = 15 V, V_{GS} = 10 V, I_D = 9.8 A	Ch-1	6.2	7.4	nC
		Channel-2 V_{DS} = 15 V, V_{GS} = 10 V, I_D = 15 A	Ch-2	12	14.2	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 9.8 A; Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 15 A	Ch-1	3	3.5	
			Ch-2	6	6.8	
Gate-Source Charge	Q_{gs}		Ch-1	1.5	1.5	
			Ch-2	2.2	2.2	
Gate-Drain Charge	Q_{gd}		Ch-1	1.1	1.1	
			Ch-2	2.3	2.3	

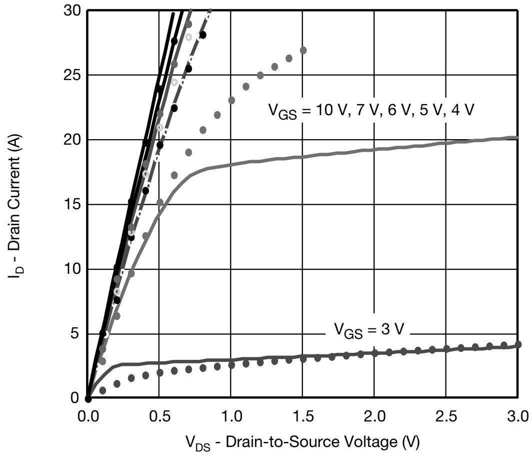
Notes

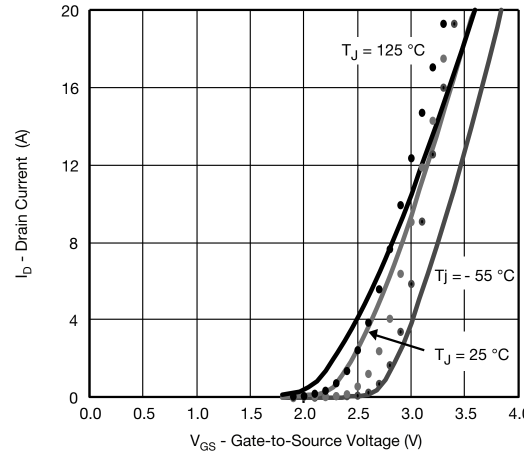
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

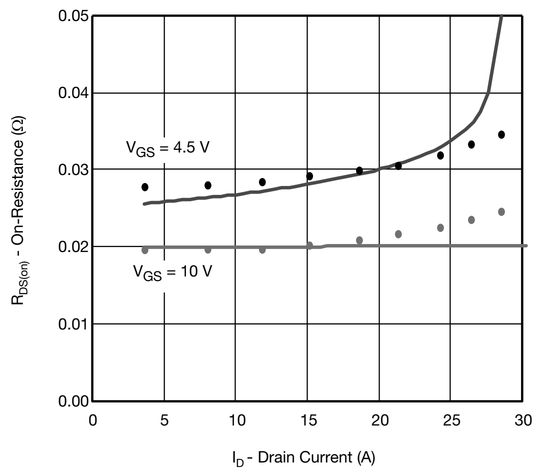
b. Guaranteed by design, not subject to production testing.

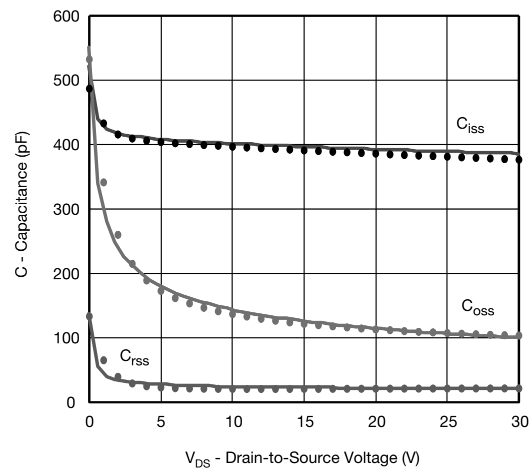
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

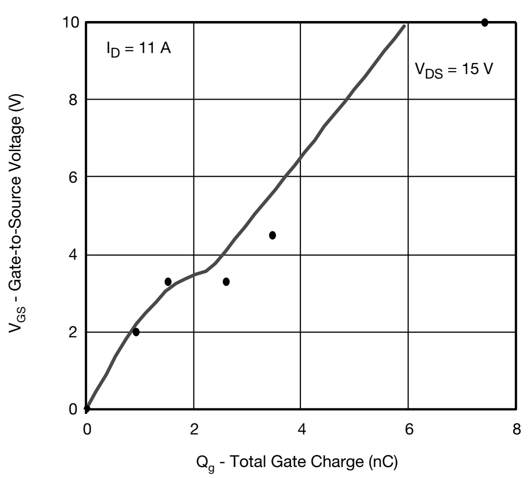
Channel-1 MOSFET

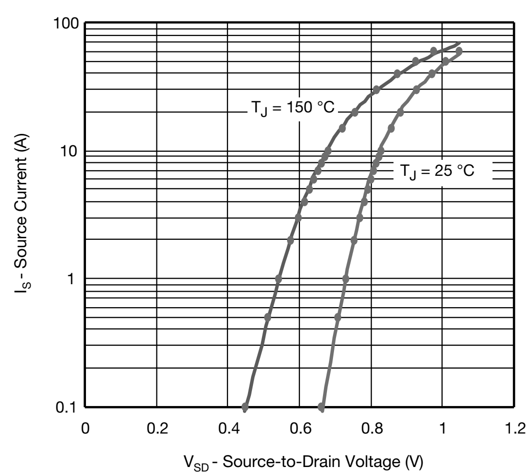










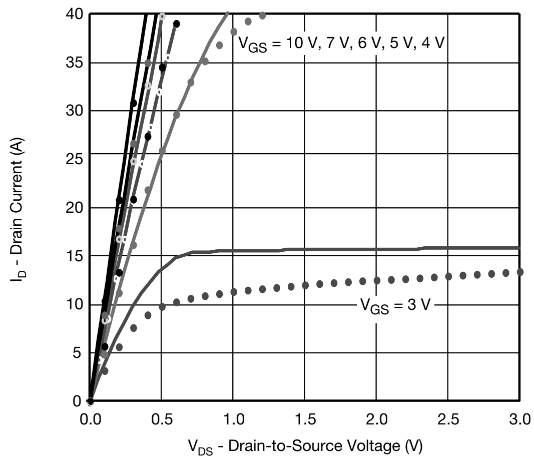


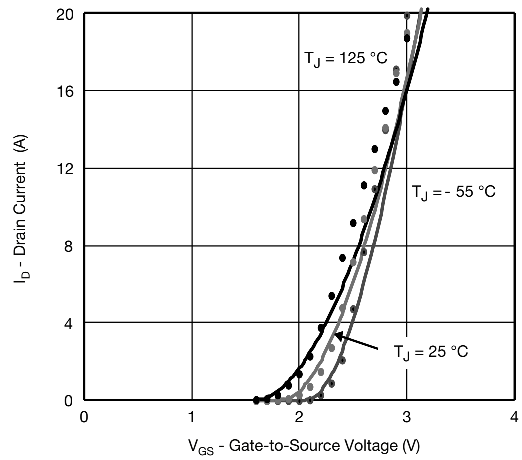
Note

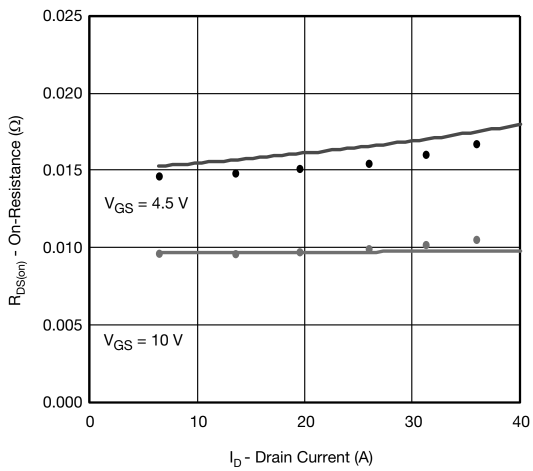
- Dots and squares represent measured data.

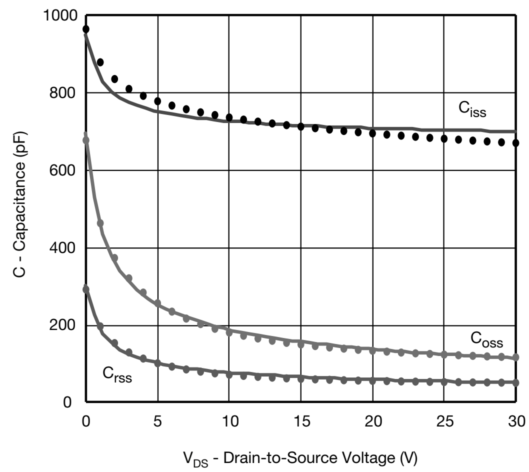
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

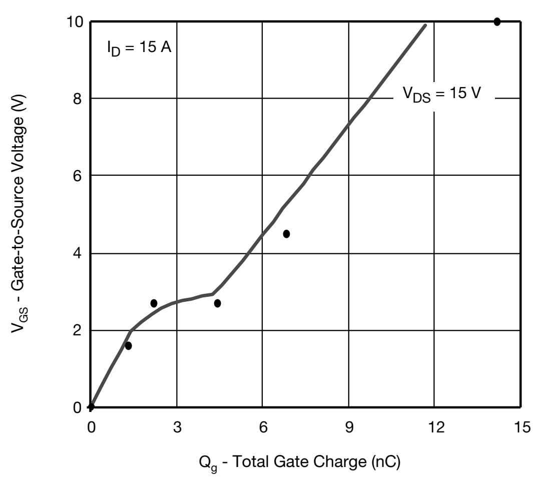
Channel-2 MOSFET

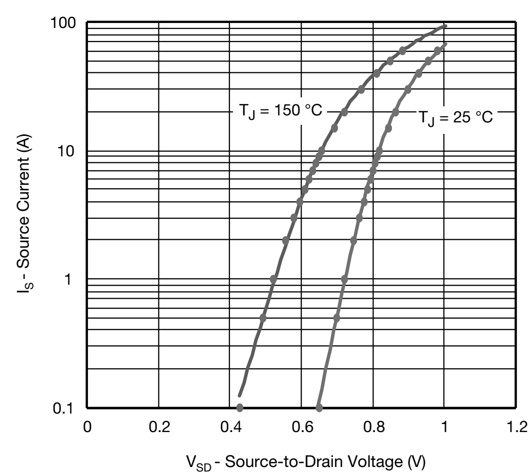












Note

- Dots and squares represent measured data.

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