

N-Channel Dual Asymmetric 40 V (D-S) 175 °C MOSFET

DESCRIPTION

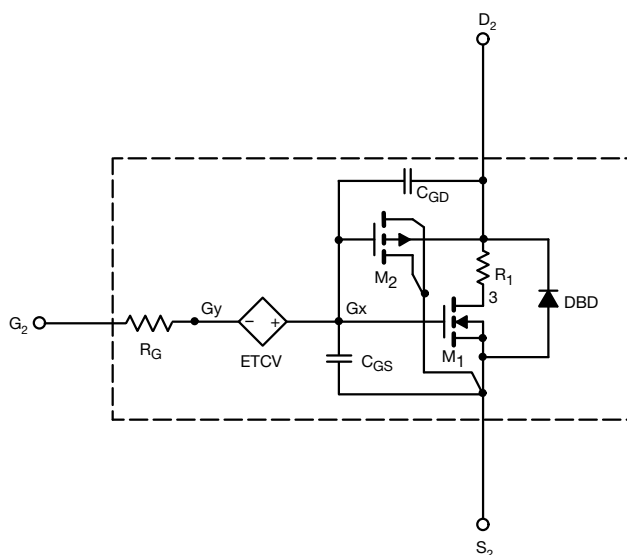
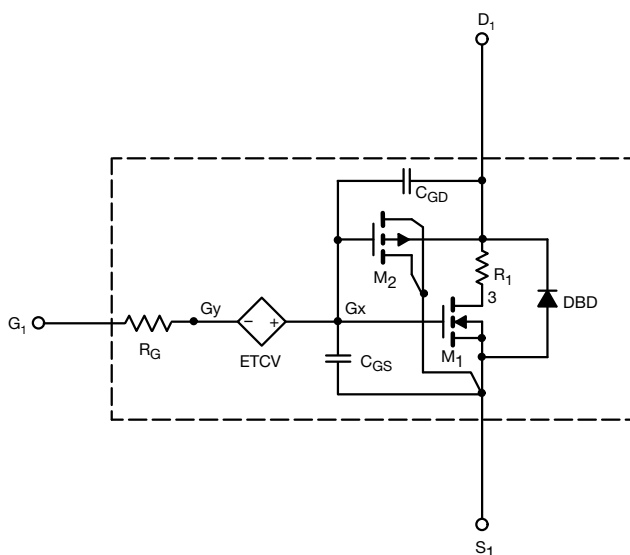
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.9	1.8	V
			Ch-2	2	1.8	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.8 A	Ch-1	0.017	0.018	Ω
		V _{GS} = 10 V, I _D = 10.1 A	Ch-2	0.008	0.009	
		V _{GS} = 4.5 V, I _D = 7.1 A	Ch-1	0.021	0.022	
		V _{GS} = 4.5 V, I _D = 9.3 A	Ch-2	0.010	0.011	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A	Ch-1	38	46	S
		V _{DS} = 15 V, I _D = 10.1 A	Ch-2	62	73	
Diode Forward Voltage ^a	V _{SD}	I _S = 5.2 A	Ch-1	0.8	0.8	V
		I _S = 6.8 A	Ch-2	0.8	0.8	
Dynamic ^b						
Input Capacitance	C _{iss}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	647	647	pF
Output Capacitance	C _{oss}		Ch-2	1170	1161	
		Ch-1	107	105		
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	Ch-2	181	178	
		Ch-1	42	42		
			Ch-2	68	68	
Total Gate Charge	Q _g	Channel 1 V _{DS} = 20 V, V _{GS} = 10 V, I _D = 16 A	Ch-1	11	13.1	nC
Gate-Source Charge	Q _{gs}		Ch-2	19	22.5	
		Ch-1	2.12	2.12		
Gate-Drain Charge	Q _{gd}	Channel 2 V _{DS} = 20 V, V _{GS} = 10 V, I _D = 6 A	Ch-2	3.35	3.35	
		Ch-1	1.84	1.84		
			Ch-2	3.14	3.14	

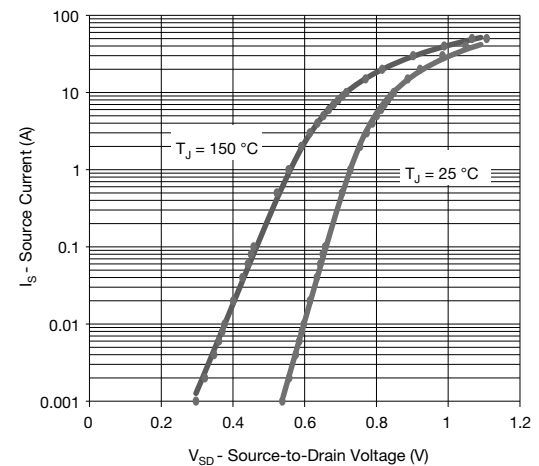
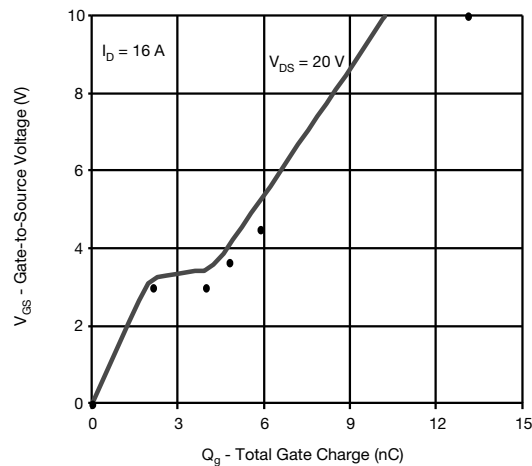
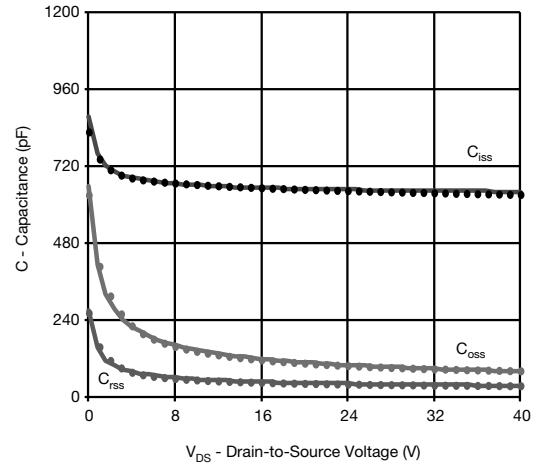
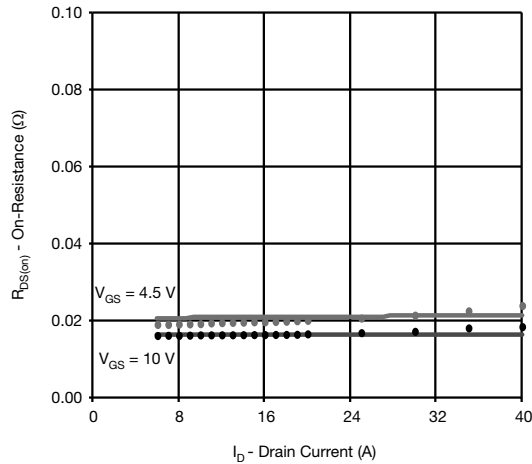
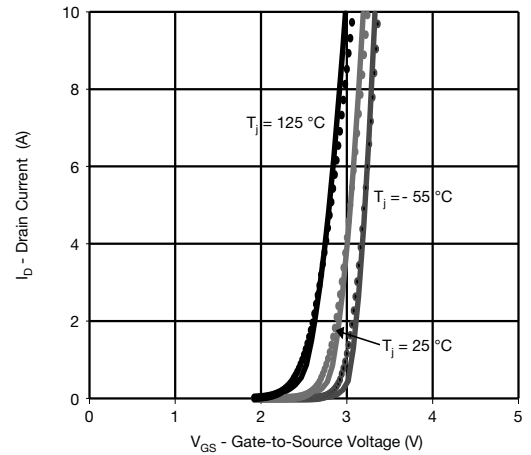
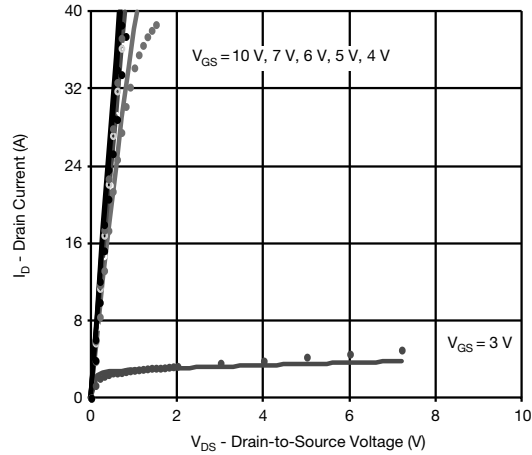
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\ \%$.
b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)

N-Channel 1 MOSFET



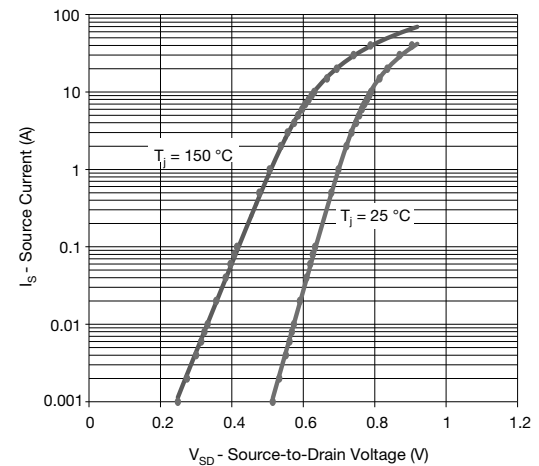
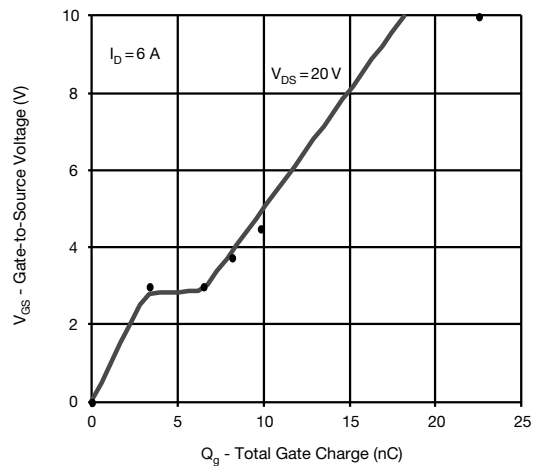
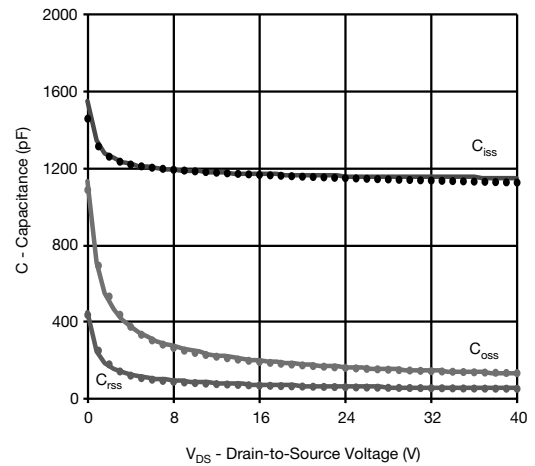
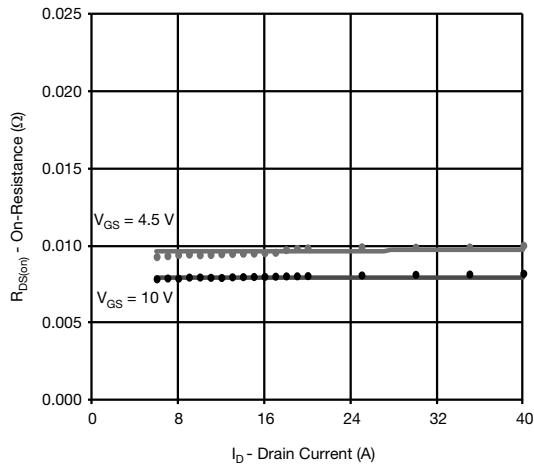
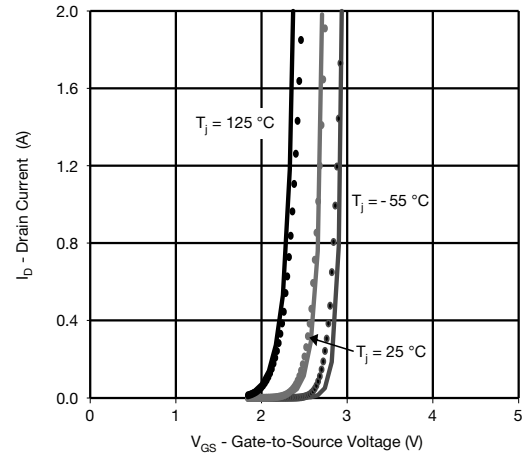
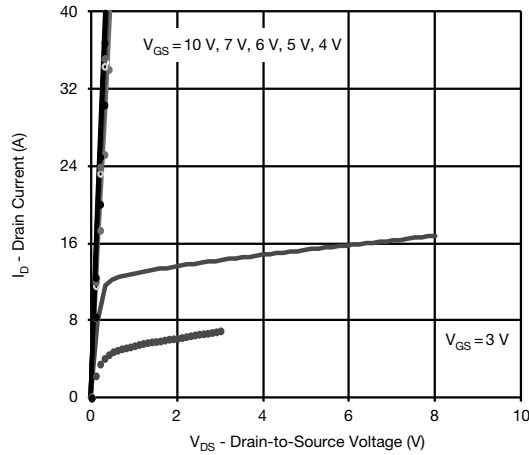
Note

- Dots and squares represent measured data.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)

N-Channel 2 MOSFET



Note

- Dots and squares represent measured data.