

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^{a, d}	Q _g (Typ.)
-20	0.0080 at V _{GS} = -4.5 V	-16.7	70 nC
	0.0086 at V _{GS} = -3.7 V	-16.1	
	0.0110 at V _{GS} = -2.5 V	-14.2	
	0.0185 at V _{GS} = -1.8 V	-11	

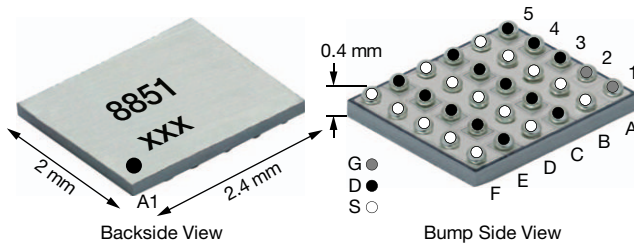
FEATURES

- TrenchFET[®] power MOSFET
- Small 2.4 mm x 2 mm outline area
- Low 0.4 mm max. profile
- Typical ESD protection 6000 V HBM
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



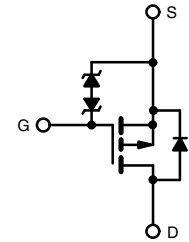
RoHS
COMPLIANT
HALOGEN
FREE

Power MICRO FOOT[®] 2.4 x 2



APPLICATIONS

- Battery switch / load switch
- Power management
- For smart phones, tablet PCs, and mobile computing



P-Channel MOSFET

Ordering Information:

Si8851EDB-T2-E1 (Lead (Pb)-free and halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _A = 25 °C	-16.7 ^a
		T _A = 70 °C	-13.4 ^a
		T _A = 25 °C	-7.7 ^b
		T _A = 70 °C	-6.2 ^b
Pulsed Drain Current (t = 100 μs)	I _{DM}	-80	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	-0.55 ^b
Maximum Power Dissipation	P _D	T _A = 25 °C	3.1 ^a
		T _A = 70 °C	2 ^a
		T _A = 25 °C	0.66 ^b
		T _A = 70 °C	0.43 ^b
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Package Reflow Conditions ^c	VPR	260	
	IR/Convection	260	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
- Refer to IPC/JEDEC[®] (J-STD-020), no manual or hand soldering.
- Based on T_A = 25 °C.

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t = 5 s	R _{thJA}	30	40	°C/W
Maximum Junction-to-Ambient ^{c, d}	t = 5 s		145	188	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper.
- Maximum under steady state conditions is 85 °C/W.
- Surface mounted on 1" x 1" FR4 board with minimum copper.
- Maximum under steady state conditions is 330 °C/W.



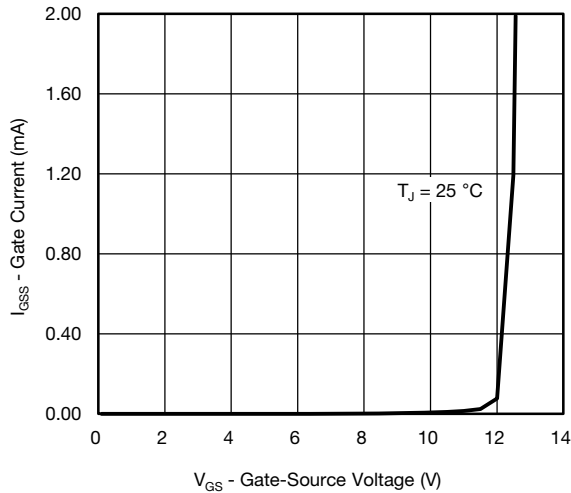
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-11	-	mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	3	-		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45	-	-1	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 0.5	μA	
		V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 10		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-5	-	-	A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -7 A	-	0.0060	0.0080	Ω	
		V _{GS} = -3.7 V, I _D = -7 A	-	0.0065	0.0086		
		V _{GS} = -2.5 V, I _D = -5 A	-	0.0081	0.0110		
		V _{GS} = -1.8 V, I _D = -3 A	-	0.0130	0.0185		
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -7 A	-	50	-	S	
Dynamic^b							
Input Capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	6900	-	pF	
Output Capacitance	C _{oss}		-	640	-		
Reverse Transfer Capacitance	C _{rss}		-	715	-		
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -8 V, I _D = -5 A	-	120	180	nC	
			-	70	105		
Gate-Source Charge	Q _{gs}	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5 A	-	8	-		
Gate-Drain Charge	Q _{gd}		-	14	-		
Gate Resistance	R _g		V _{GS} = -0.1 V, f = 1 MHz	-	2.3		-
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 2 Ω I _D ≅ -5 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	35	70		ns
Rise Time	t _r		-	40	80		
Turn-Off Delay Time	t _{d(off)}		-	115	230		
Fall Time	t _f		-	35	70		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 2 Ω I _D ≅ -5 A, V _{GEN} = -8 V, R _g = 1 Ω	-	15	30		
Rise Time	t _r		-	10	20		
Turn-Off Delay Time	t _{d(off)}		-	110	220		
Fall Time	t _f		-	25	50		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _A = 25 °C	-	-	-2.6	A	
Pulse Diode Forward Current (t = 100 μs)	I _{SM}		-	-	-80		
Body Diode Voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.8	-1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = -5 A, di/dt = 100 A/μs, T _J = 25 °C	-	40	80	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	30	60	nC	
Reverse Recovery Fall Time	t _a		-	16	-	ns	
Reverse Recovery Rise Time	t _b		-	24	-		

Notes

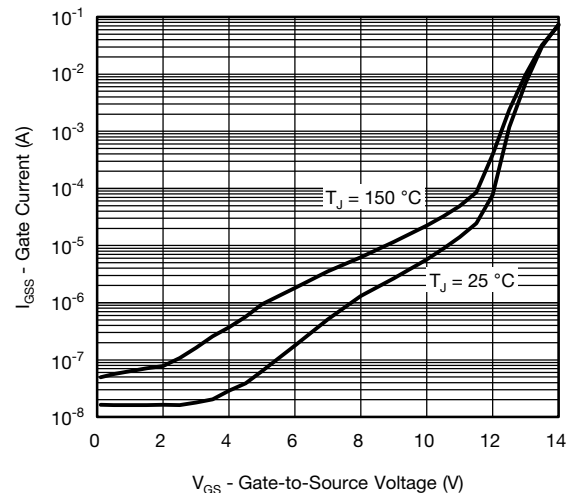
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

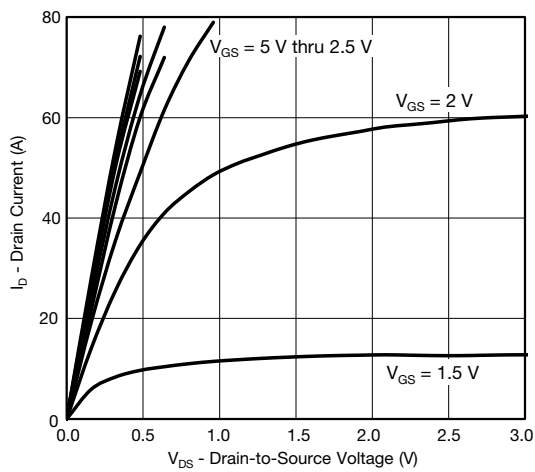
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



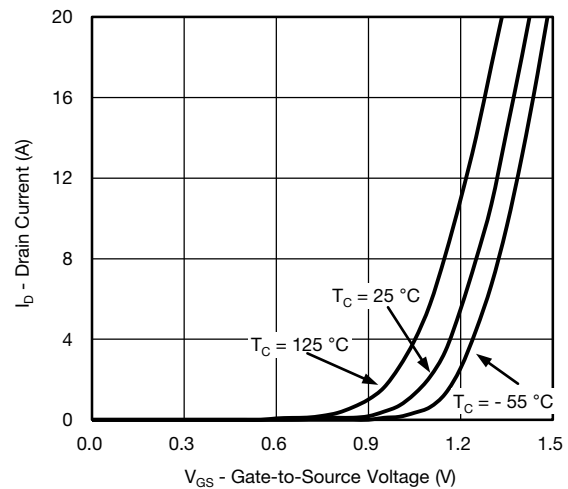
Gate Current vs. Gate-Source Voltage



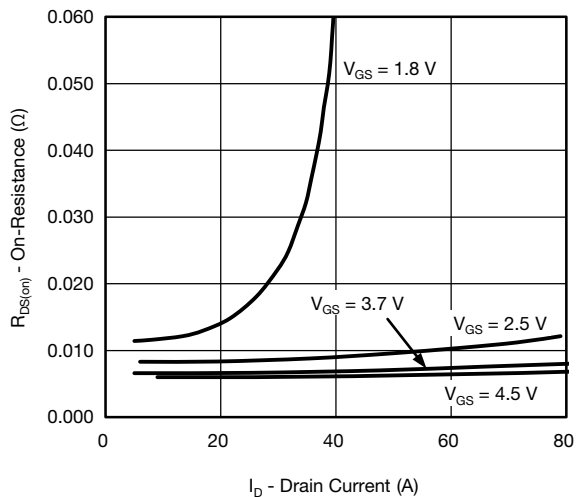
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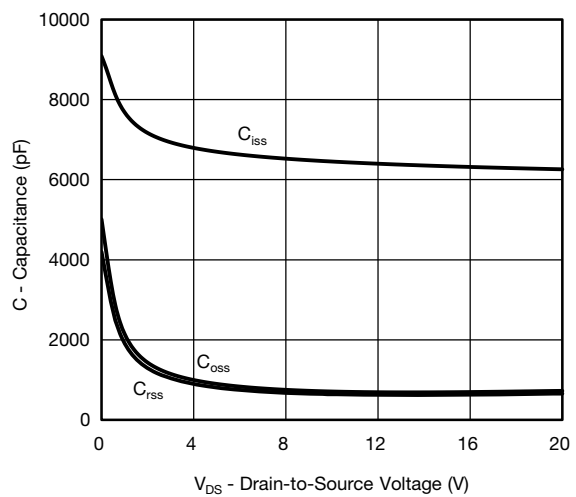
Output Characteristics



Transfer Characteristics



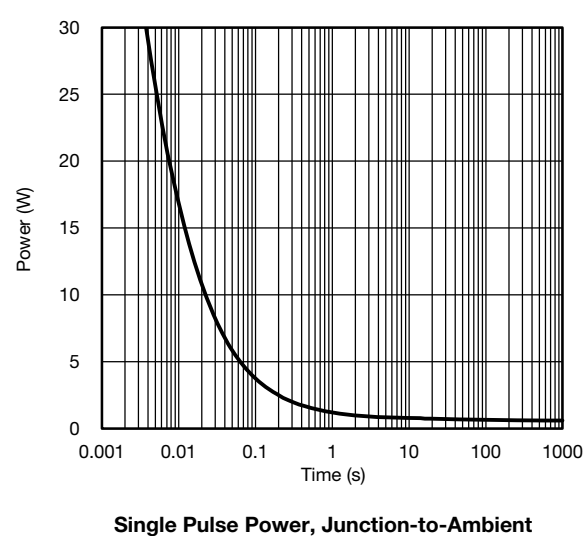
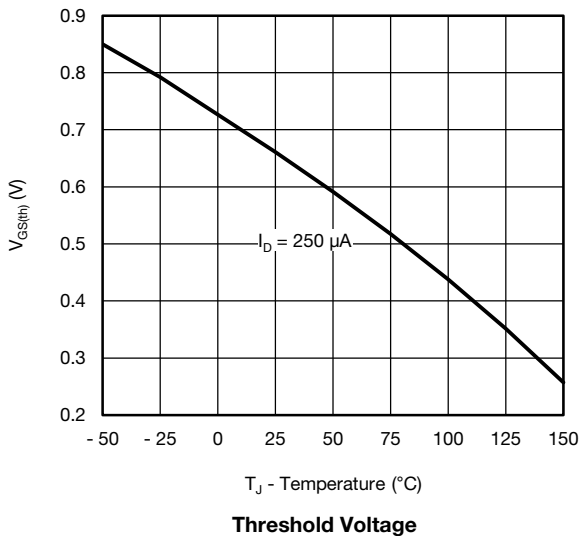
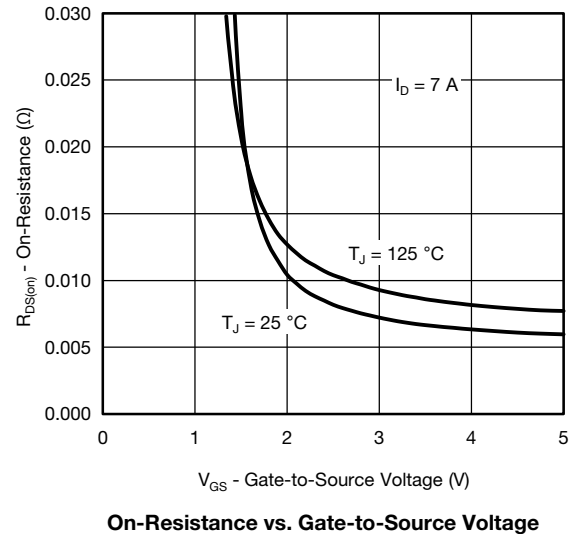
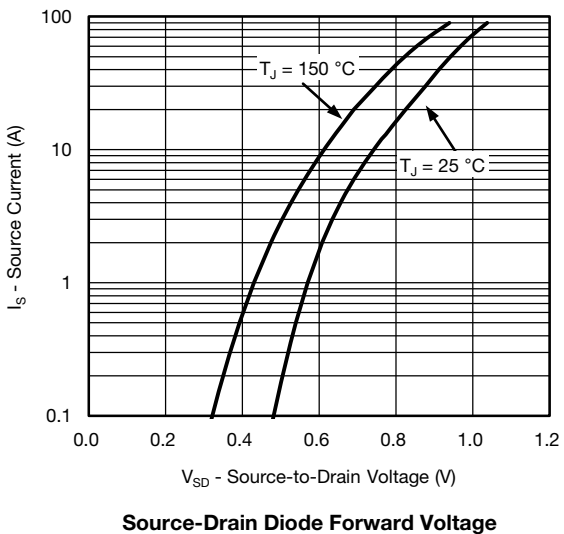
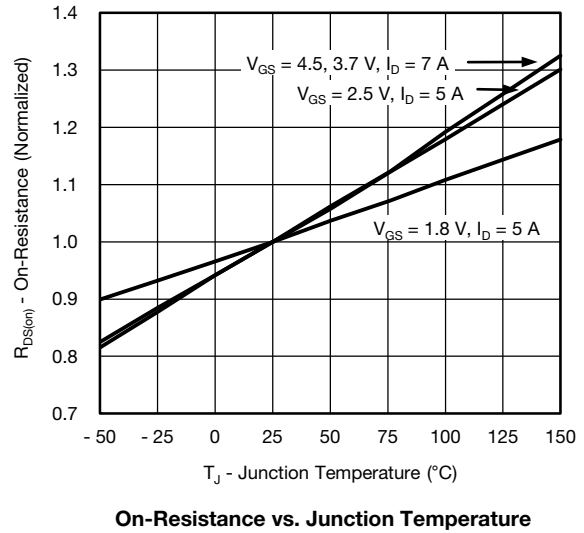
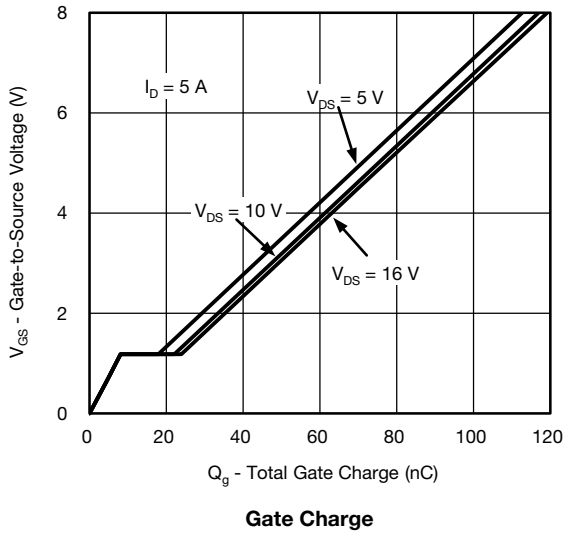
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

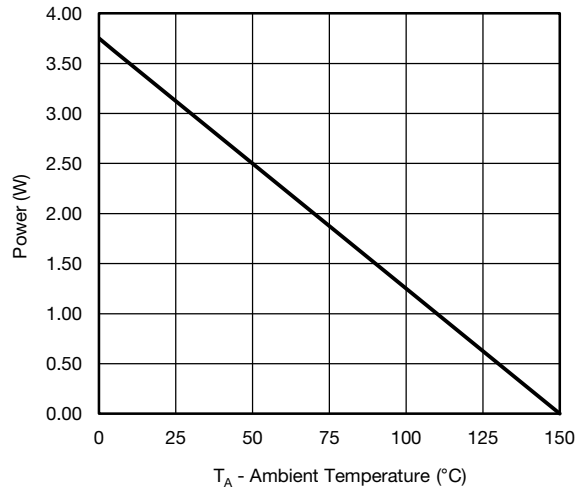
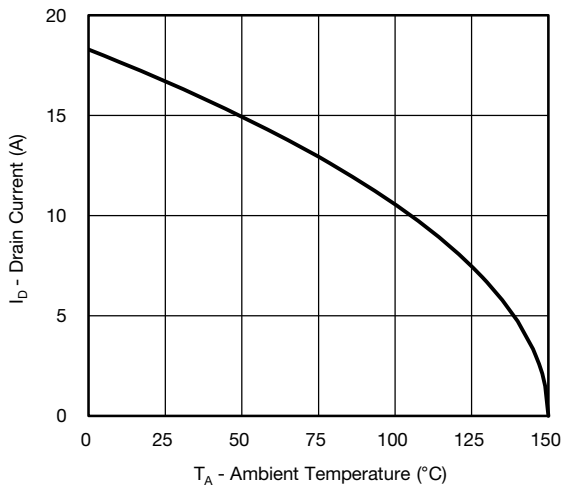
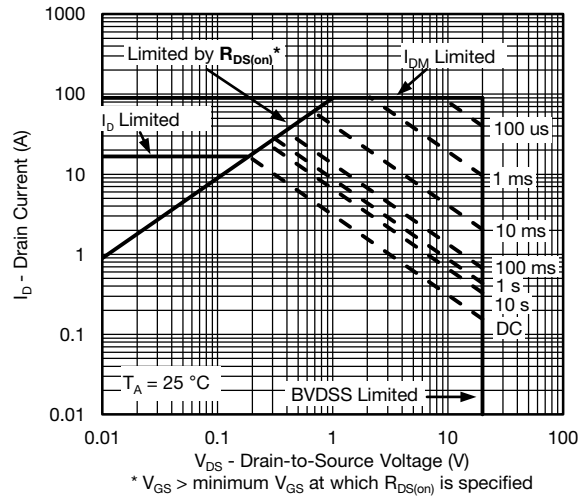


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





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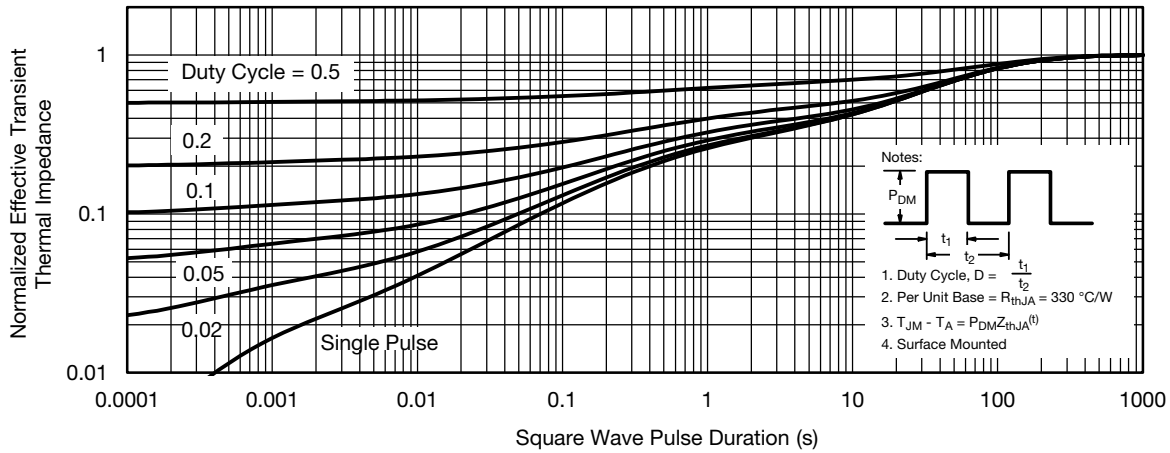


Note

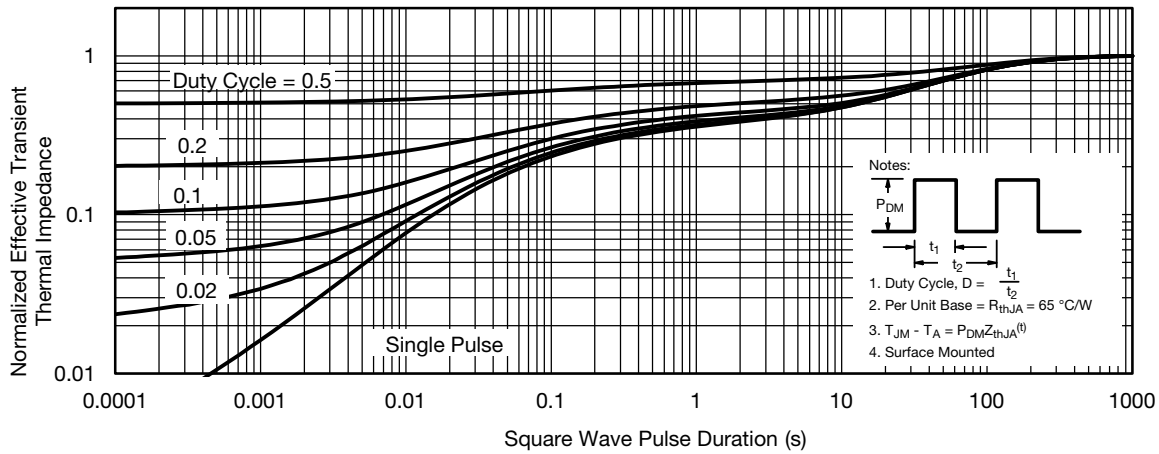
a. When mounted on 1" x 1" FR4 with full copper and $t = 5$ s



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



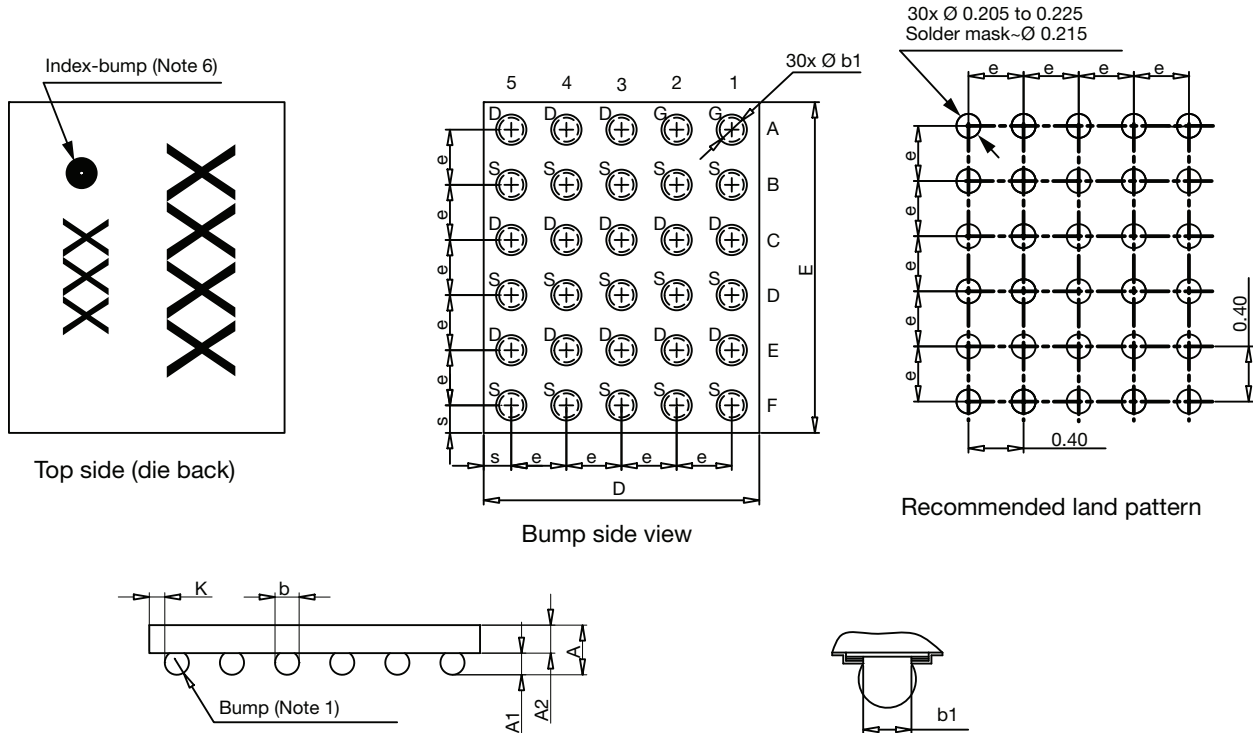
Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with minimum Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with maximum Copper)

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MICRO FOOT[®]: 30-Bumps (2.4 mm x 2 mm, 0.4 mm Pitch, 0.184 mm Bump Height)


Notes

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.328	0.365	0.402	0.0129	0.0144	0.0158
A1	0.136	0.160	0.184	0.0054	0.0063	0.0072
A2	0.192	0.205	0.218	0.0076	0.0081	0.0086
b	0.200	0.220	0.240	0.0079	0.0087	0.0094
b1		0.175			0.0069	
e		0.400			0.0157	
s	0.160	0.180	0.200	0.0063	0.0071	0.0079
D	1.920	1.960	2.000	0.0756	0.0772	0.0787
E	2.320	2.360	2.400	0.0913	0.0929	0.0945
K	0.040	0.070	0.100	0.0016	0.0028	0.0039

Note

- Use millimeters as the primary measurement.

ECN: T15-0177-Rev. A, 27-Apr-15
DWG: 6040



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