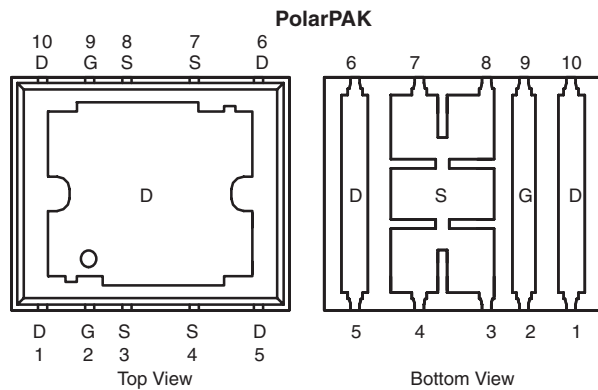




## N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)		Q <sub>g</sub> (Typ.)
		Silicon Limit	Package Limit	
60	0.0061 at V <sub>GS</sub> = 10 V	110	60	51 nC

Package Drawing:  
[www.vishay.com/doc?72945](http://www.vishay.com/doc?72945)



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE876DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

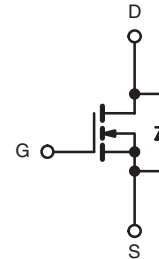
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK<sup>®</sup> Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
  - Die Not Exposed
  - Same Layout Regardless of Die Size < 150 μm
- Low Q<sub>gd</sub>/Q<sub>gs</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS directive 2002/95/EC



RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

- Primary Side Switch
- Half-Bridge



N-Channel MOSFET

For Related Documents:  
[www.vishay.com/ppg?64823](http://www.vishay.com/ppg?64823)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	110 (Silicon Limit)	A
		T <sub>C</sub> = 70 °C	60 <sup>a</sup> (Package Limit)	
		T <sub>A</sub> = 25 °C	60 <sup>a</sup>	
		T <sub>A</sub> = 70 °C	22 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	60		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	60 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	50		
Single Pulse Avalanche Energy	E <sub>AS</sub>	125	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	125	W
		T <sub>C</sub> = 70 °C	80	
		T <sub>A</sub> = 25 °C	5.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	$R_{thJC}$ (Drain)	0.8	1	
Maximum Junction-to-Case (Source) <sup>a, c</sup>		$R_{thJC}$ (Source)	2.2	2.7	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.  
b. Maximum under Steady State conditions is 68 °C/W.  
c. Measured at source pin (on the side of the package).

**SPECIFICATIONS  $T_J = 25$  °C, unless otherwise noted**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	60			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A		70		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	2.5		4.4	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60$ V, $V_{GS} = 0$ V			1	$\mu$ A
		$V_{DS} = 60$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 20$ A		0.0050	0.0061	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 20$ A		30		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 30$ V, $V_{GS} = 0$ V, $f = 1$ MHz		3100		pF
Output Capacitance	$C_{oss}$			480		
Reverse Transfer Capacitance	$C_{rss}$			180		
Total Gate Charge	$Q_g$	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_D = 19.8$ A		51	77	nC
Gate-Source Charge	$Q_{gs}$			19		
Gate-Drain Charge	$Q_{gd}$			15		
Gate Resistance	$R_g$	$f = 1$ MHz		1.1	2.2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30$ V, $R_L = 3$ $\Omega$ $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		22	30	ns
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			60	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				60	
Body Diode Voltage	$V_{SD}$	$I_S = 10$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C		60	90	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			135	205	nC
Reverse Recovery Fall Time	$t_a$			42		ns
Reverse Recovery Rise Time	$t_b$			18		

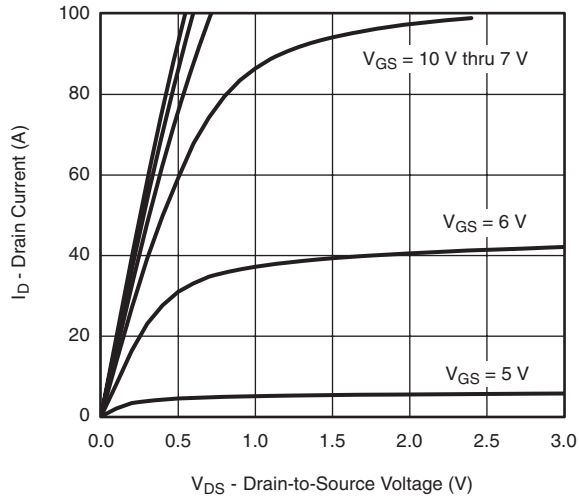
Notes:

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
b. Guaranteed by design, not subject to production testing.

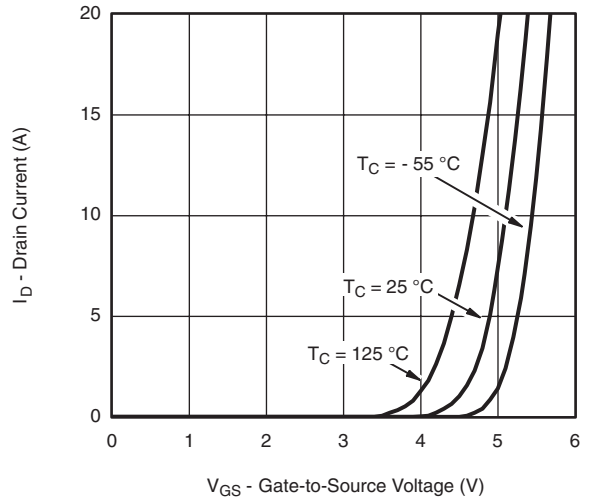
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



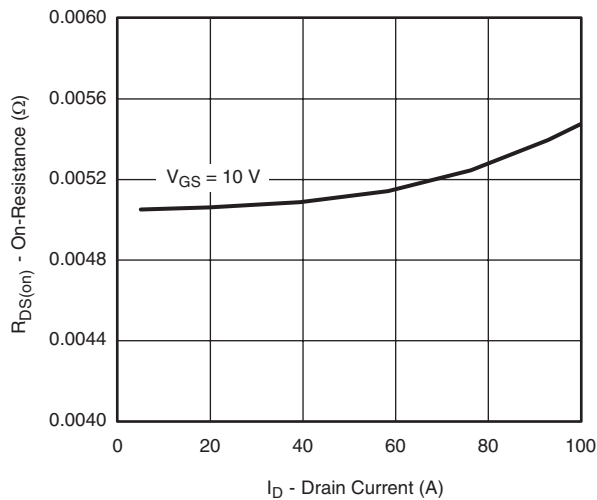
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



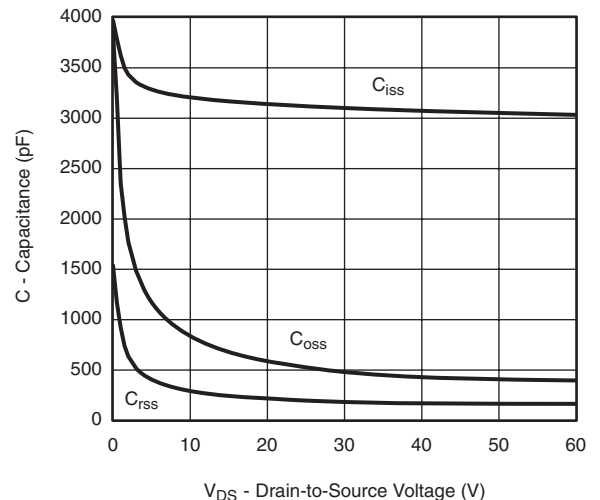
**Output Characteristics**



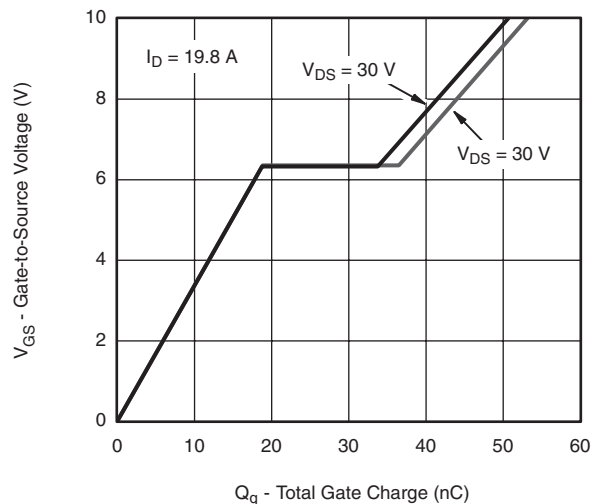
**Transfer Characteristics**



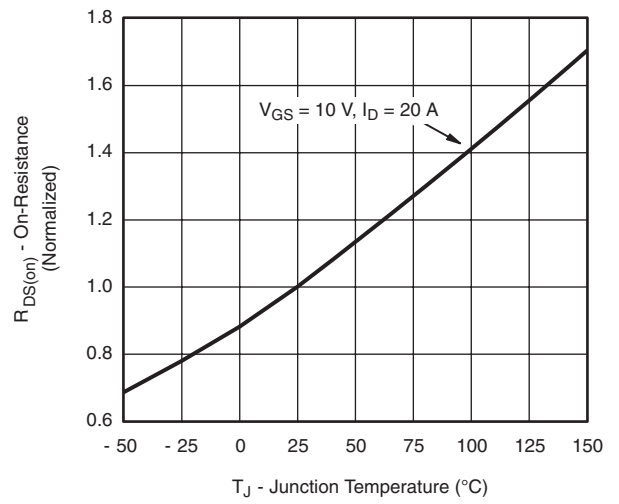
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

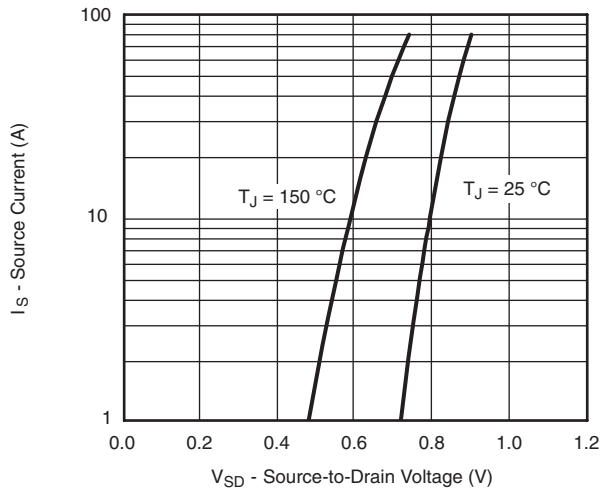


**Gate Charge**

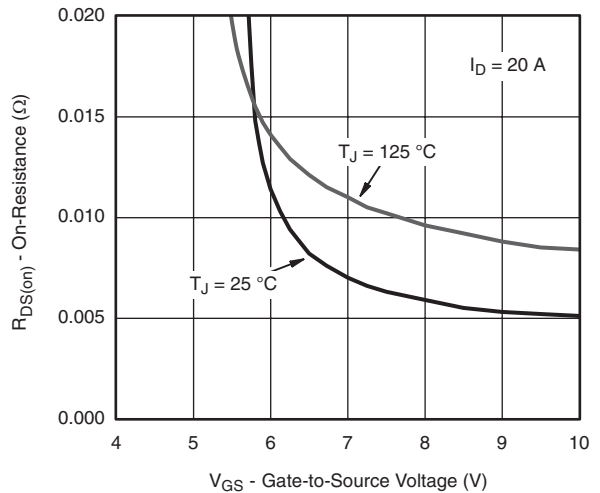


**On-Resistance vs. Junction Temperature**

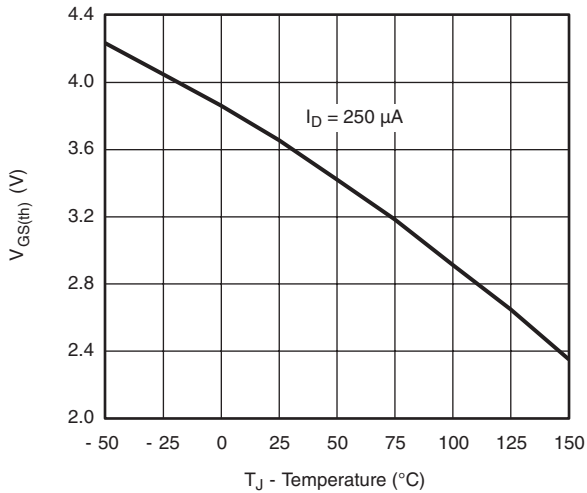
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



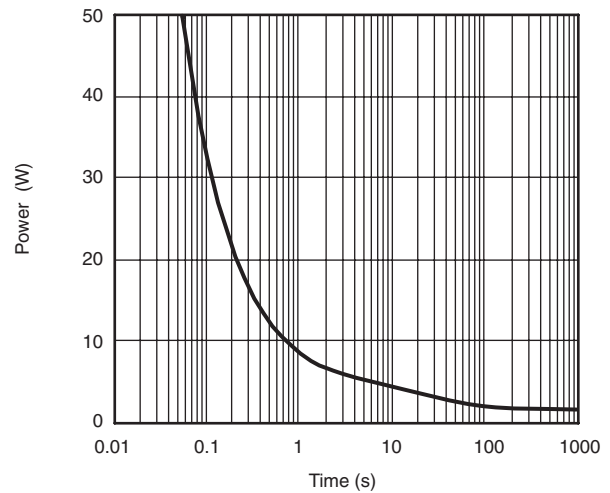
**Source-Drain Diode Forward Voltage**



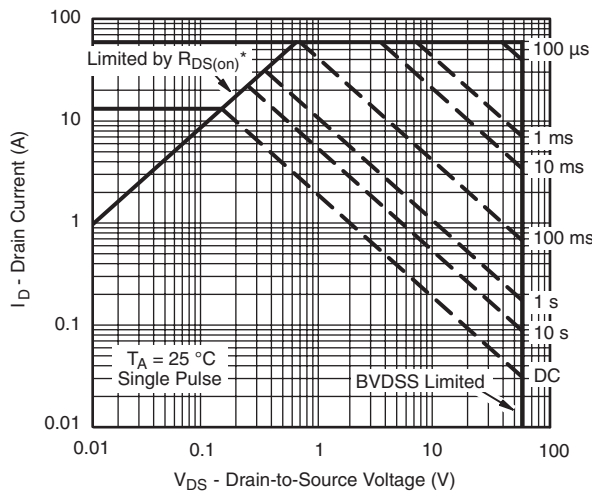
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**

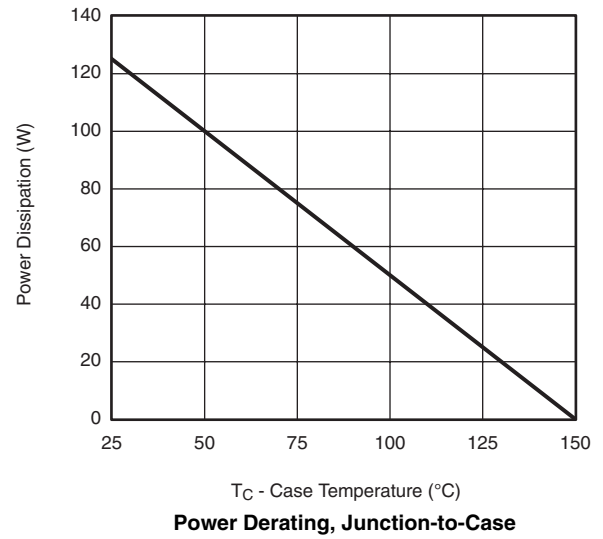
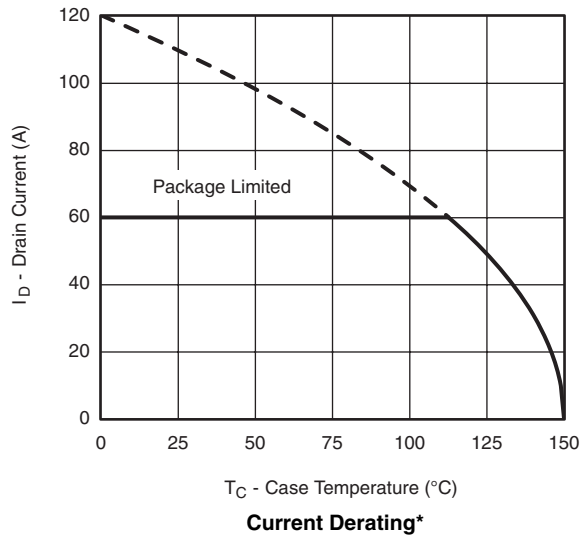


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



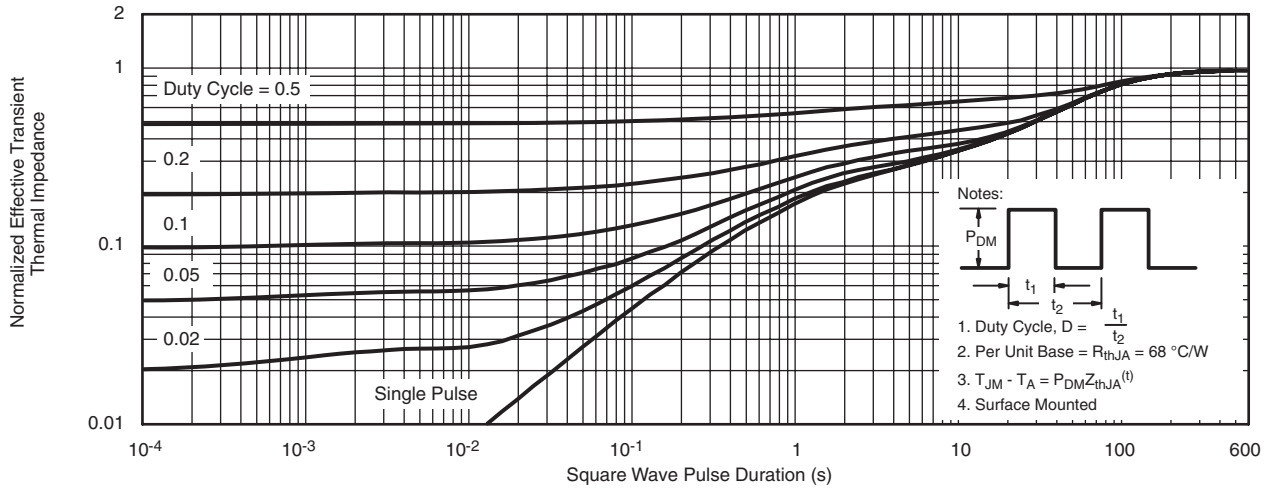
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# SiE876DF

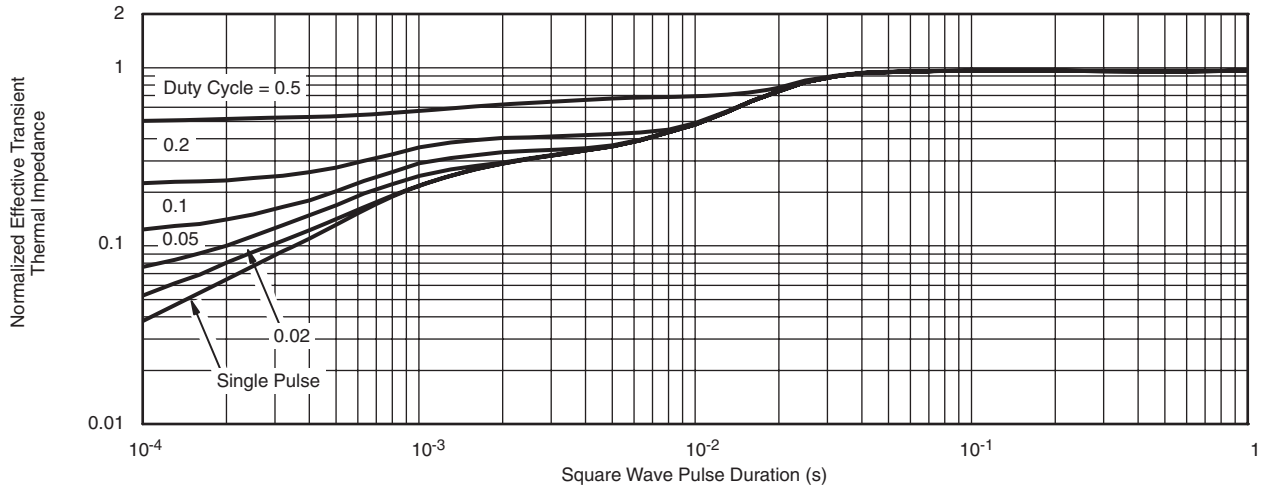
Vishay Siliconix



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)

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