

## P-Channel 20 V (D-S) MOSFET

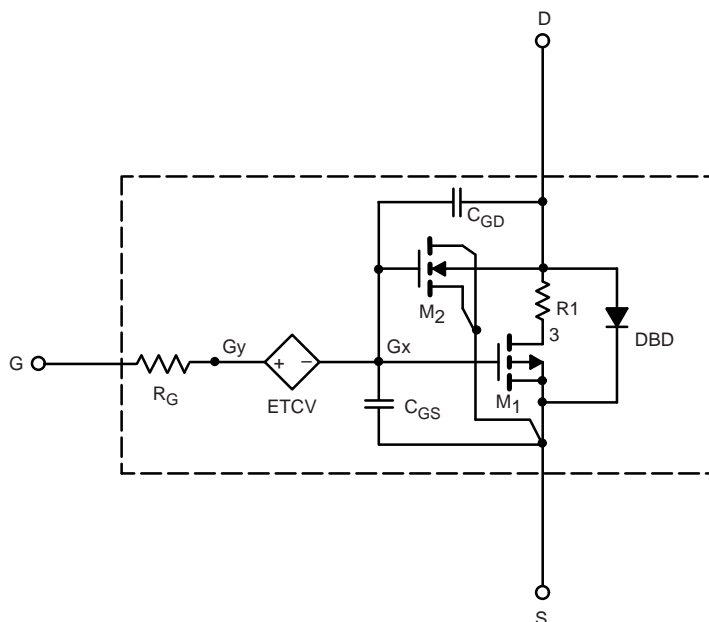
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

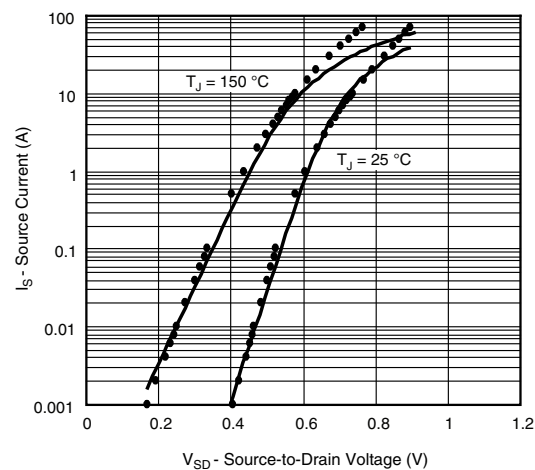
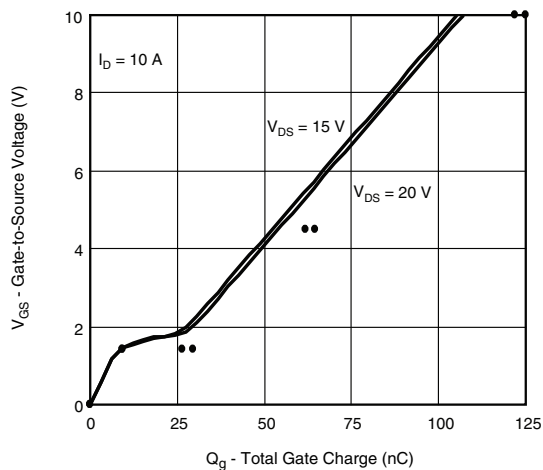
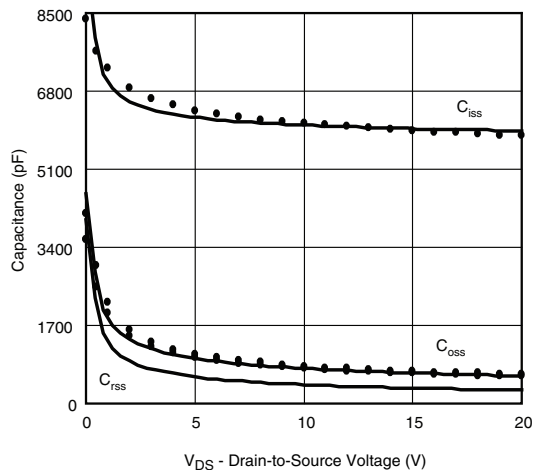
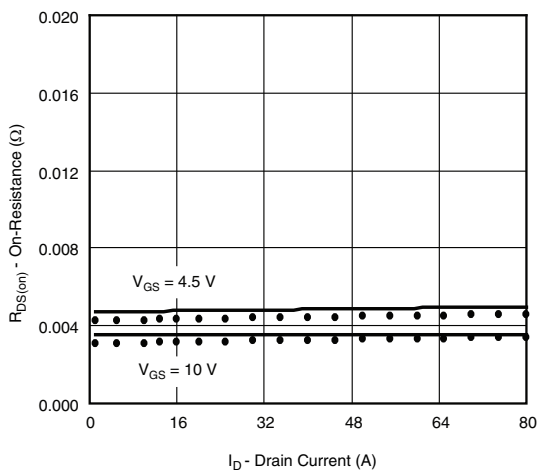
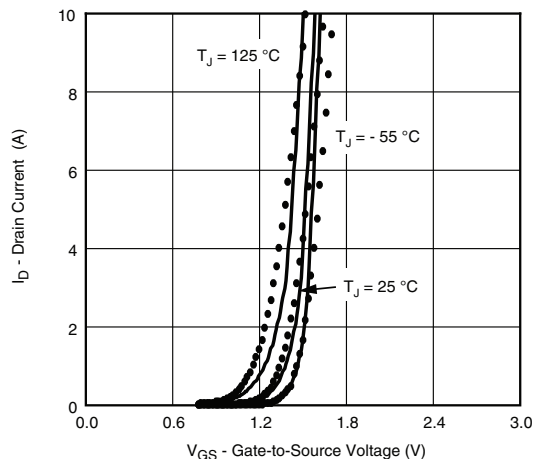
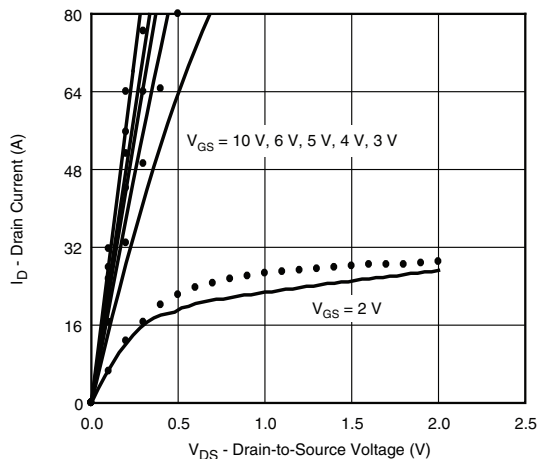
| PARAMETER                                     | SYMBOL       | TEST CONDITIONS   | SIMULATED DATA | MEASURED DATA | UNIT     |
|---|--------------|---|----------------|---------------|----------|
| <b>Static</b>                                 |              |   |                |               |          |
| Gate-Source Threshold Voltage                 | $V_{GS(th)}$ | $V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$                       | 0.80           | -             | V        |
| Drain-Source On-State Resistance <sup>a</sup> | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}$ , $I_D = -20\text{ A}$                            | 0.0034         | 0.0031        | $\Omega$ |
|   |              | $V_{GS} = -4.5\text{ V}$ , $I_D = -15\text{ A}$                           | 0.0047         | 0.0043        |          |
| Forward Transconductance <sup>a</sup>         | $g_{fs}$     | $V_{DS} = -10\text{ V}$ , $I_D = -20\text{ A}$                            | 57             | 70            | S        |
| Diode Forward Voltage <sup>a</sup>            | $V_{SD}$     | $I_S = -4\text{ A}$   | -0.69          | -0.68         | V        |
| <b>Dynamic<sup>b</sup></b>                    |              |   |                |               |          |
| Input Capacitance                             | $C_{iss}$    | $V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$      | 6060           | 6000          | pF       |
| Output Capacitance                            | $C_{oss}$    |   | 766            | 780           |          |
| Reverse Transfer Capacitance                  | $C_{rss}$    |   | 412            | 820           |          |
| Total Gate Charge                             | $Q_g$        | $V_{DS} = -10\text{ V}$ , $V_{GS} = -10\text{ V}$ , $I_D = -10\text{ A}$  | 107            | 122           | nC       |
|   |              |   | 54             | 62            |          |
| Gate-Source Charge                            | $Q_{gs}$     | $V_{DS} = -10\text{ V}$ , $V_{GS} = -4.5\text{ V}$ , $I_D = -10\text{ A}$ | 9.4            | 9.4           |          |
| Gate-Drain Charge                             | $Q_{gd}$     |   | 17.2           | 17.2          |          |

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.