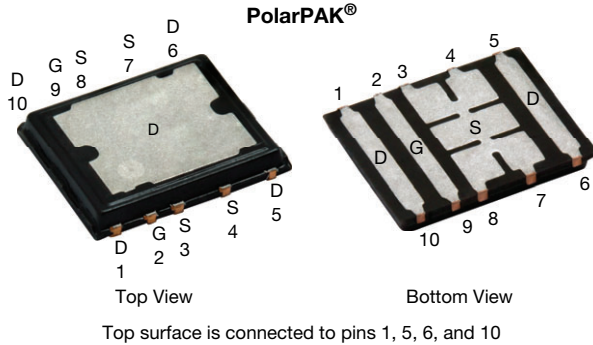


N-Channel 25 V (D-S) MOSFET



FEATURES

- TrenchFET® Gen III power MOSFET
- Ultra low thermal resistance using top-exposed PolarPAK® package for double-sided cooling
- Leadframe-based encapsulated package
 - Die not exposed
 - Same layout regardless of die size, ≤ 100 V
- Low Q_{gd}/Q_{gs} ratio helps prevent shoot-through
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

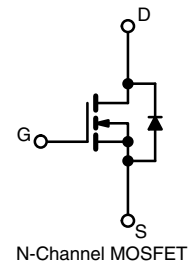


RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	25
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.0014
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.0018
Q_g typ. (nC)	46
I_D (A) ^a (package limit)	60
I_D (A) ^a (silicon limit)	229
Configuration	Single

APPLICATIONS

- VRM
- DC/DC conversion: low side
- Server V_{CORE}



ORDERING INFORMATION	
Package	PolarPAK
Lead (Pb)-free and halogen-free	SiE882DF-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	25	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	60 ^a (package limit)	A
		229 (silicon limit)	
		60 ^a	
		47 ^{b, c}	
Pulsed drain current	I_{DM}	100	A
		41 ^{b, c}	
Continuous source-drain diode current	I_S	60 ^a	A
		4.3 ^{b, c}	
Single pulse avalanche current	I_{AS}	50	mJ
Avalanche energy	E_{AS}	125	
Maximum power dissipation	P_D	125	W
		80	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

Notes

- Package limited is 60 A
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum junction-to-case (drain top)	Steady state	R_{thJC} (drain)	0.8	1	
Maximum junction-to-case (source) ^{a, c}		R_{thJC} (source)	2.2	2.7	

Notes

- a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 68 °C/W
c. Measured at source pin (on the side of the package)

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	25	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A	-	25	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-6	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1	1.7	2.2	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 25$ V, $V_{GS} = 0$ V	-	-	1	μ A
		$V_{DS} = 25$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 20$ A	-	0.0011	0.0014	Ω
		$V_{GS} = 4.5$ V, $I_D = 20$ A	-	0.0015	0.0018	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15$ V, $I_D = 20$ A	-	125	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 12.5$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	6400	-	pF
Output capacitance	C_{oss}		-	1400	-	
Reverse transfer capacitance	C_{rss}		-	550	-	
Total gate charge	Q_g	$V_{DS} = 12.5$ V, $V_{GS} = 10$ V, $I_D = 20$ A	-	96	145	nC
		$V_{DS} = 12.5$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A	-	46	70	
Gate-source charge	Q_{gs}		-	18	-	
Gate-drain charge	Q_{gd}		-	12	-	
Gate resistance	R_g	$f = 1$ MHz	0.2	1.1	2.2	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 12.5$ V, $R_L = 1.25$ Ω , $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	-	45	70	ns
Rise time	t_r		-	170	255	
Turn-off delay time	$t_{d(off)}$		-	65	100	
Fall time	t_f		-	85	130	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 12.5$ V, $R_L = 1.25$ Ω , $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	20	30	
Rise time	t_r		-	15	25	
Turn-off delay time	$t_{d(off)}$		-	45	70	
Fall time	t_f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25$ °C	-	-	60	A
Pulse diode forward current ^a	I_{SM}		-	-	100	
Body diode voltage	V_{SD}	$I_S = 10$ A	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C	-	55	85	ns
Body diode reverse recovery charge	Q_{rr}		-	70	105	nC
Reverse recovery fall time	t_a		-	25	-	ns
Reverse recovery rise time	t_b		-	30	-	

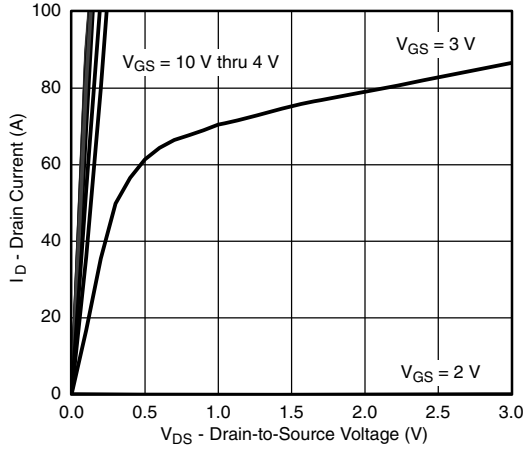
Notes

- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

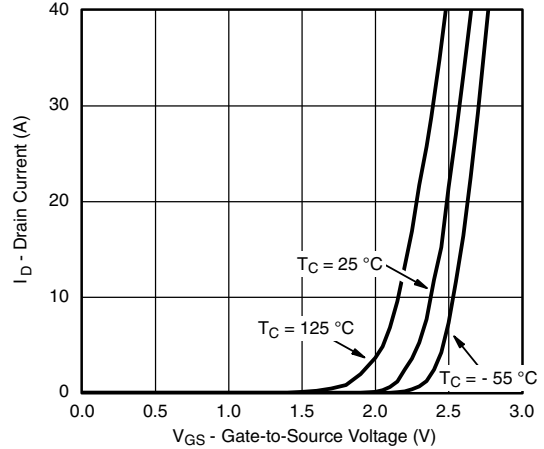
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



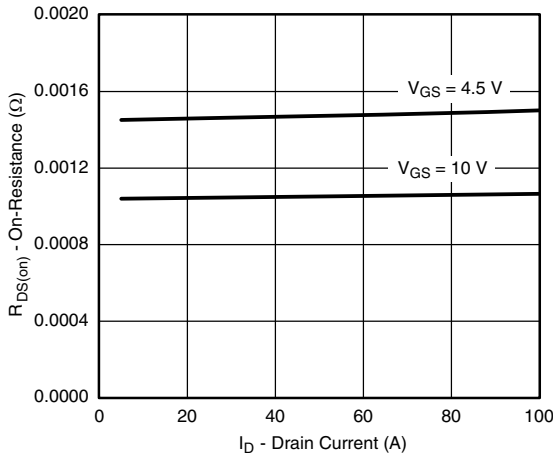
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



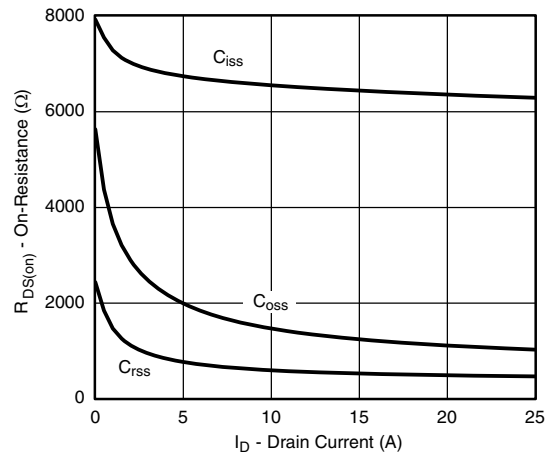
Output Characteristics



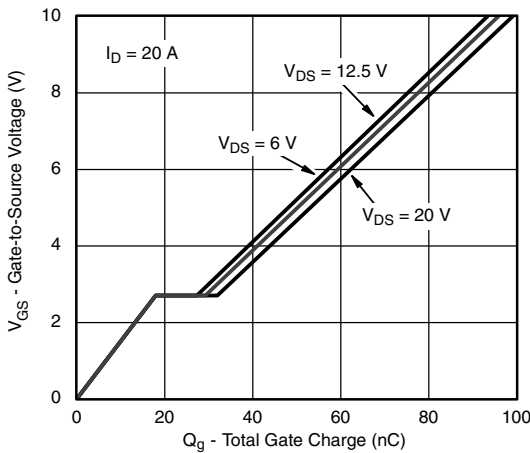
Transfer Characteristics



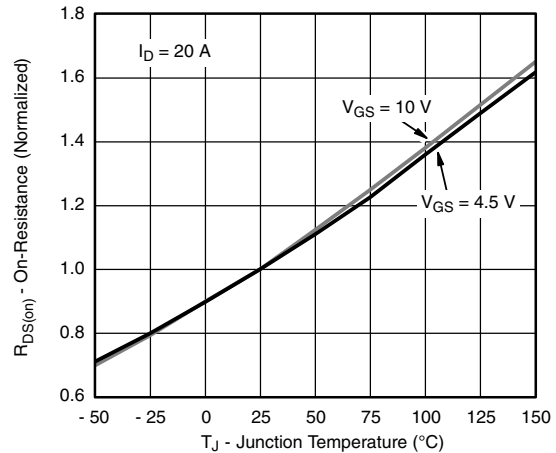
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



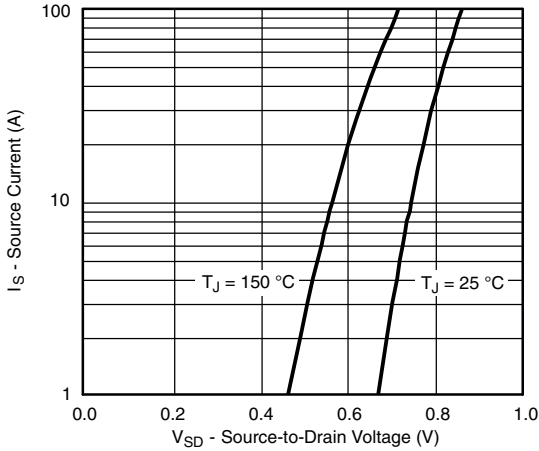
Gate Charge



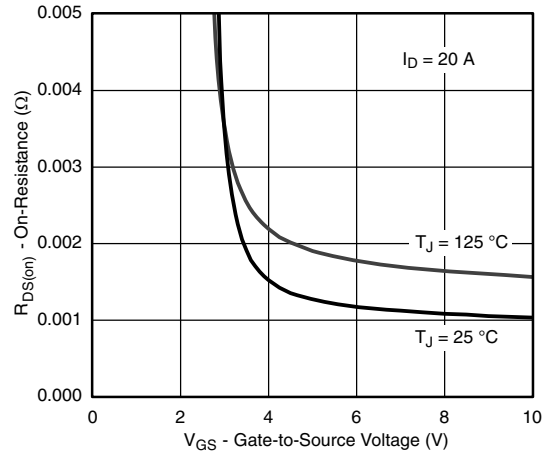
On-Resistance vs. Junction Temperature



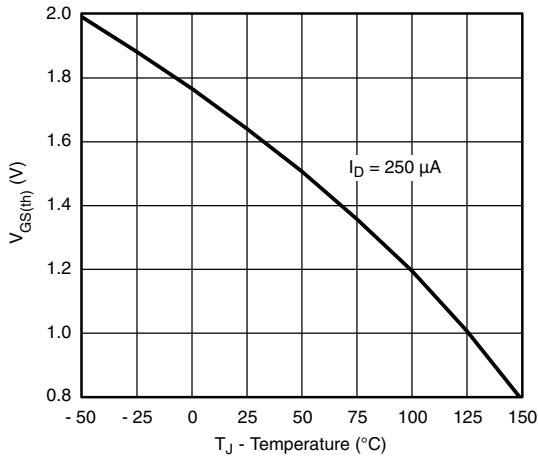
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



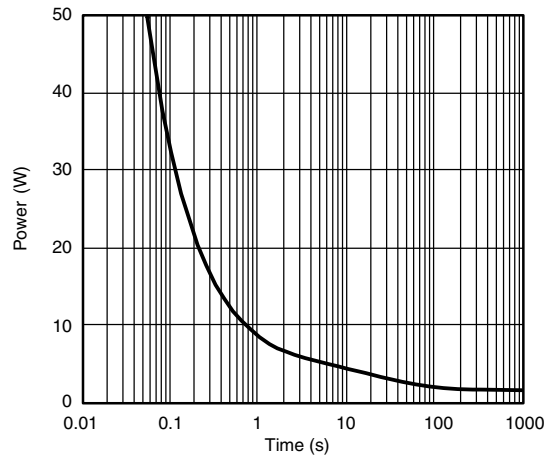
Source-Drain Diode Forward Voltage



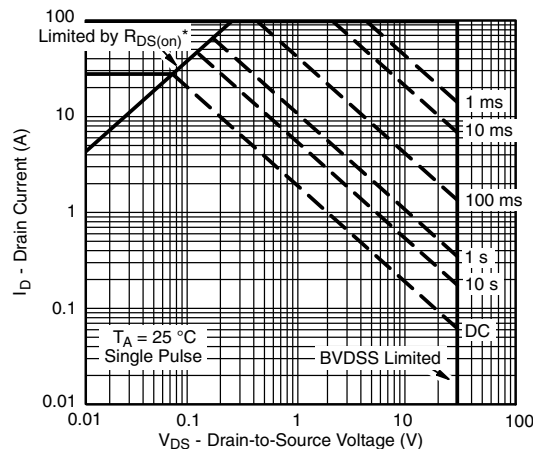
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



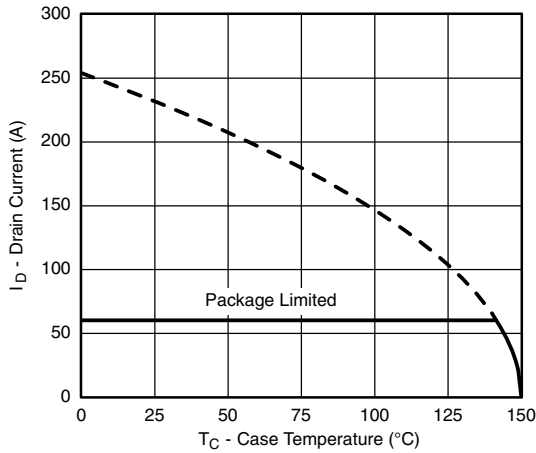
Single Pulse Power, Junction-to-Ambient



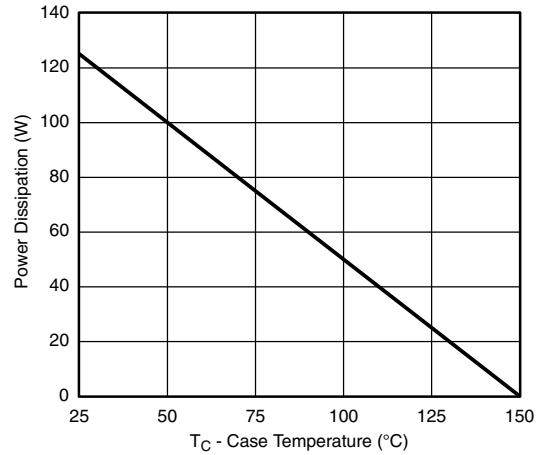
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



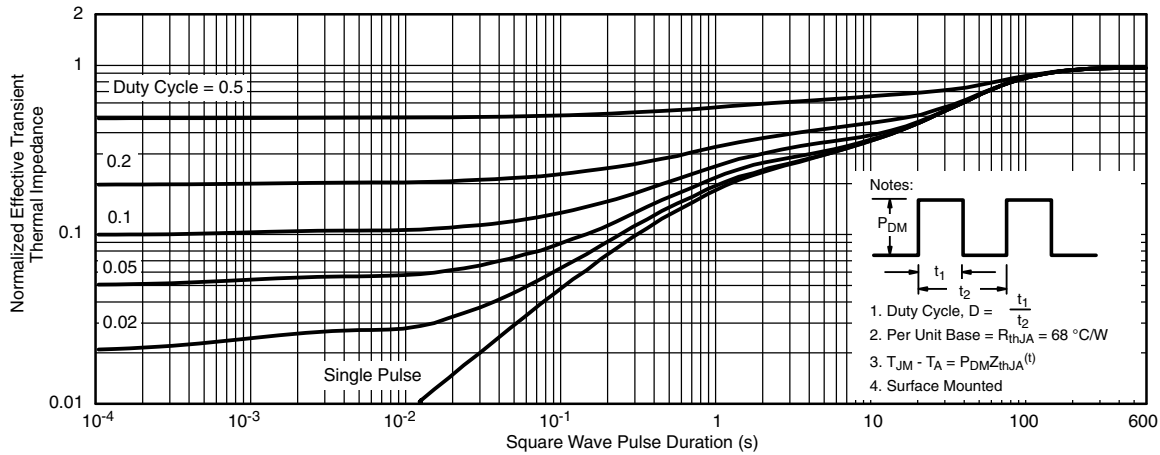
Power Derating, Junction-to-Case

Note

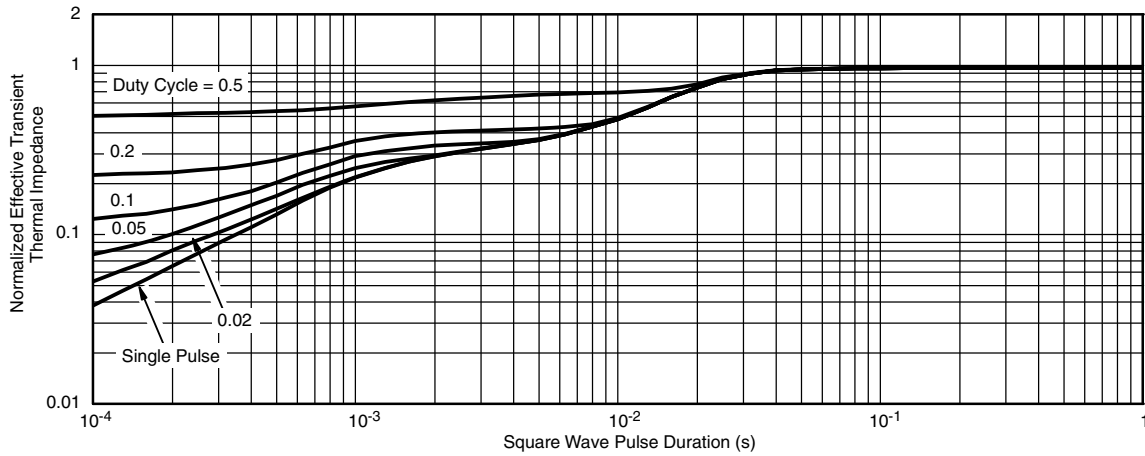
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



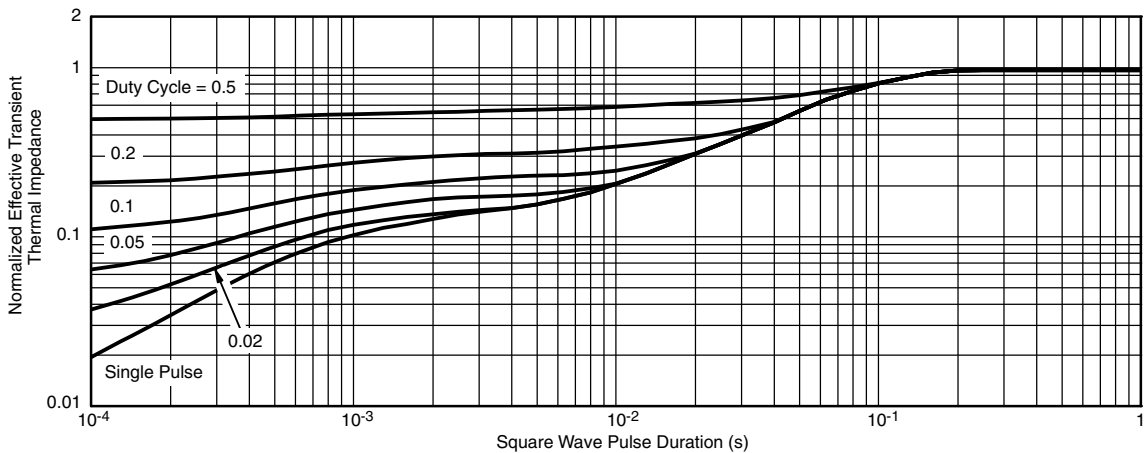
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65002.

POLARPAK™ OPTION L



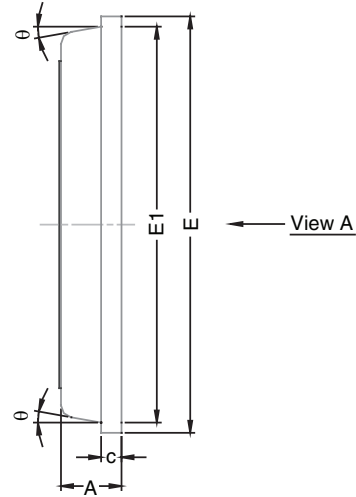
(Top View)



DETAIL Z



Product datasheet/information page contain links to applicable package drawing.



View A



View A
(Bottom View)

Package Information

Vishay Siliconix



DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	-	0.05	0.000	-	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	-	-	0.009	-	-
H2	0.45	-	0.56	0.018	-	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	-	0.56	0.018	-	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37	-	-	0.054	-	-
K4	0.24	-	-	0.009	-	-
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	-	-	0.009	-	-
M4	0.05	-	-	0.002	-	-
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	-	-	0.047	-	-
T4	3.90	-	-	0.153	-	-
T5	0	0.18	0.36	0.000	0.007	0.014
θ	0°	10°	12°	0°	10°	12°

ECN: T-08441-Rev. C, 11-Aug-08
DWG: 5946

Notes

Millimeters govern over inches.

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
 Dimensions in mm/(Inches)
 No External Traces within Broken Lines
 Dot indicates Gate Pin (Part Marking)



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