



P-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^c	Q_g (Typ.)
- 100	0.043 at $V_{GS} = - 10$ V	- 36	54 nC
	0.048 at $V_{GS} = - 4.5$ V	- 34.4	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

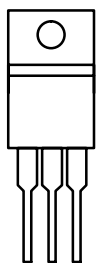


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- LCD Inverter
- Backlighting

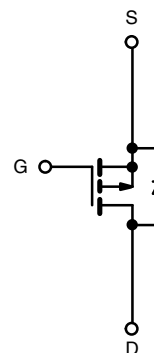
TO-220AB



G D S

Top View

Drain connected to Tab



P-Channel MOSFET

Ordering Information: SUP40P10-43-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^c	I_D	$T_C = 25$ °C	- 36
		$T_C = 125$ °C	- 16
Pulsed Drain Current	I_{DM}	- 40	A
Avalanche Current	I_{AS}	- 35	
Single Pulse Avalanche Energy ^a	E_{AS}	61	mJ
Power Dissipation	P_D	$T_C = 25$ °C	
		$T_A = 25$ °C	2.0
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air	R_{thJA}	62	°C/W
Junction-to-Case	R_{thJC}	1.0	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-109		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = -250\text{ }\mu\text{A}$		5.9		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
		$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			-200	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		0.036	0.043	Ω
		$V_{GS} = -10\text{ V}, I_D = -10\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.078	
		$V_{GS} = -10\text{ V}, I_D = -10\text{ A}, T_J = 150\text{ }^\circ\text{C}$			0.088	
		$V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$		0.040	0.048	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -10\text{ A}$		38		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -50\text{ V}, f = 1\text{ MHz}$		4600		μF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge ^c	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		106	160	nC
		$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		54	81	
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		14		
Gate-Drain Charge ^c	Q_{gd}			26		
Gate Resistance	R_g	$f = 1.0\text{ MHz}$	0.8	4	8	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.3\text{ }\Omega$ $I_D \cong -8\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1.0\text{ }\Omega$		15	25	ns
Rise Time ^c	t_r			20	30	
Turn-Off Delay Time ^c	$t_{d(off)}$			110	165	
Fall Time ^c	t_f			100	150	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.3\text{ }\Omega$ $I_D \cong 8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1.0\text{ }\Omega$		42	65	
Rise Time ^c	t_r			160	240	
Turn-Off Delay Time ^c	$t_{d(off)}$			100	150	
Fall Time ^c	t_f			100	150	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$^b						
Continuous Current	I_S				-40	A
Pulsed Current	I_{SM}				-40	
Forward Voltage ^a	V_{SD}	$I_F = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.5	V
Reverse Recovery Time	t_{rr}	$I_F = -8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		60	90	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			-5	-7.5	A
Reverse Recovery Charge	Q_{rr}				150	225

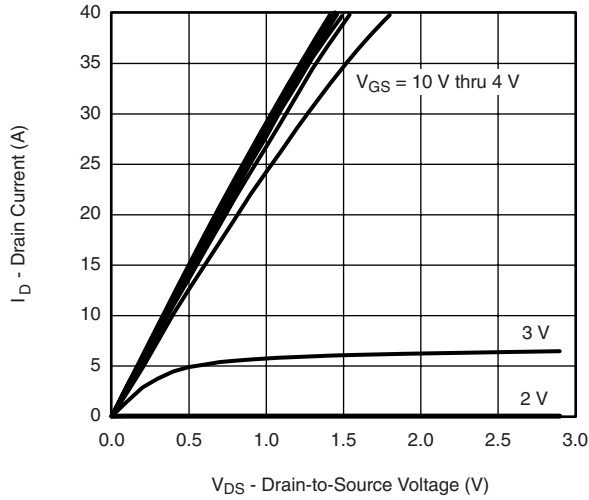
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

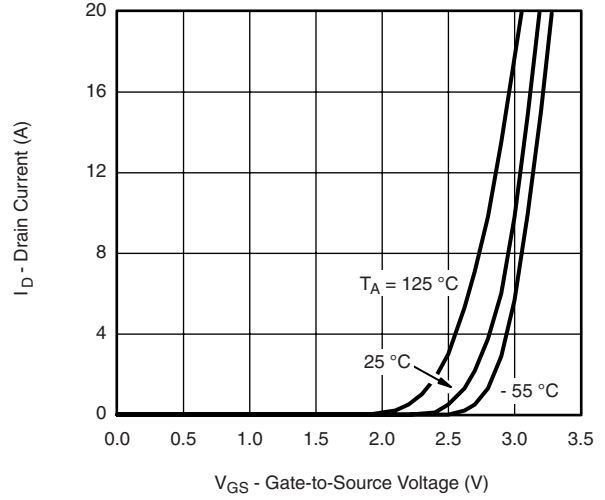
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



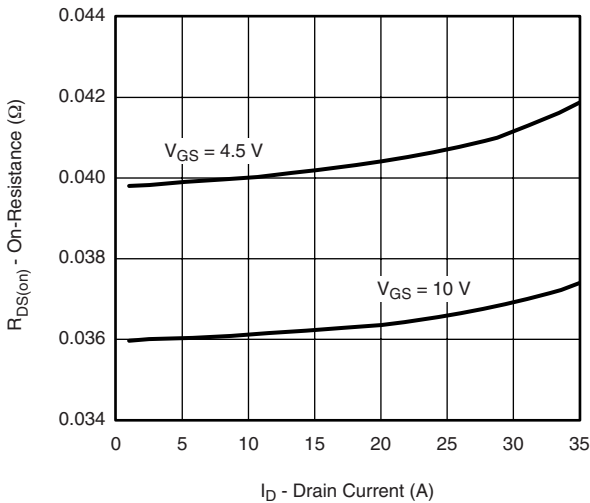
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



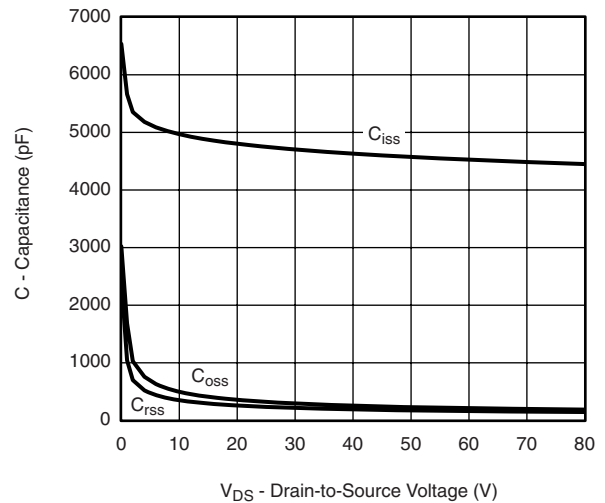
Output Characteristics



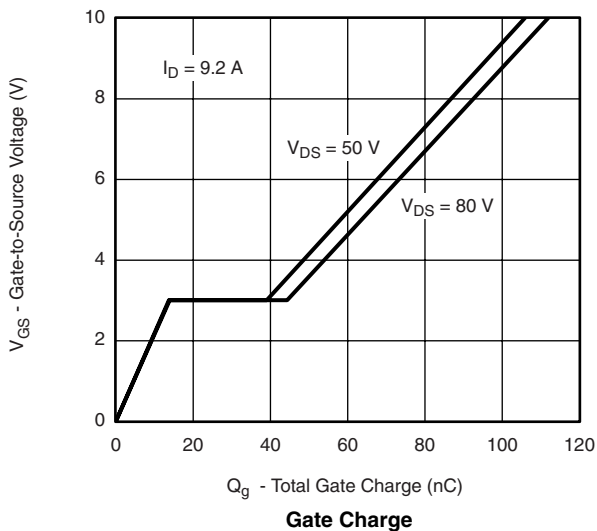
Transfer Characteristics



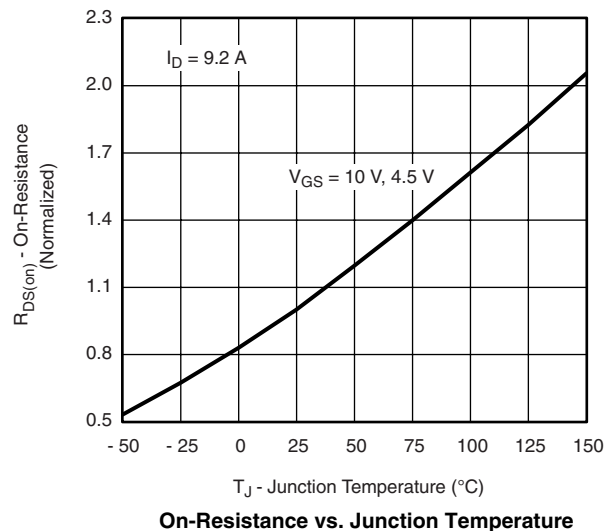
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



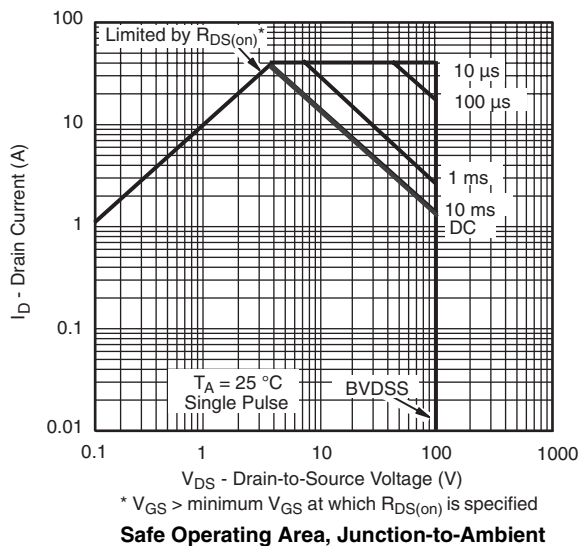
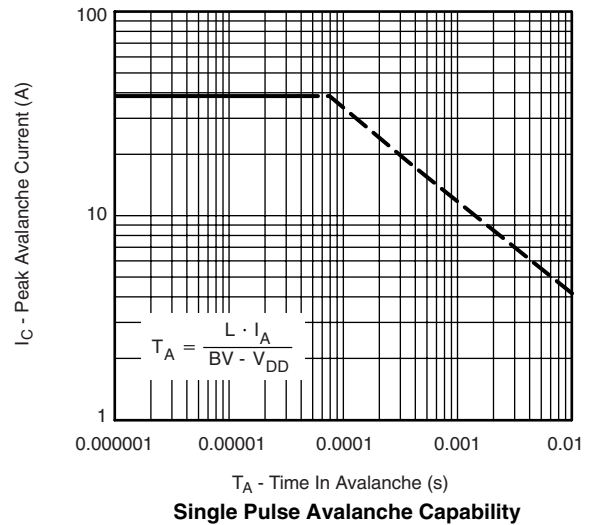
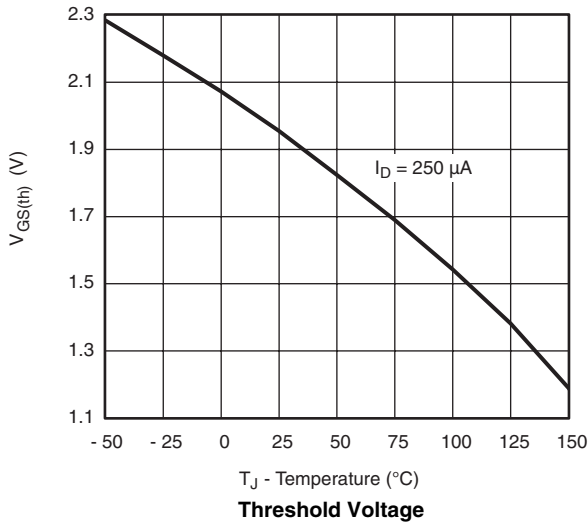
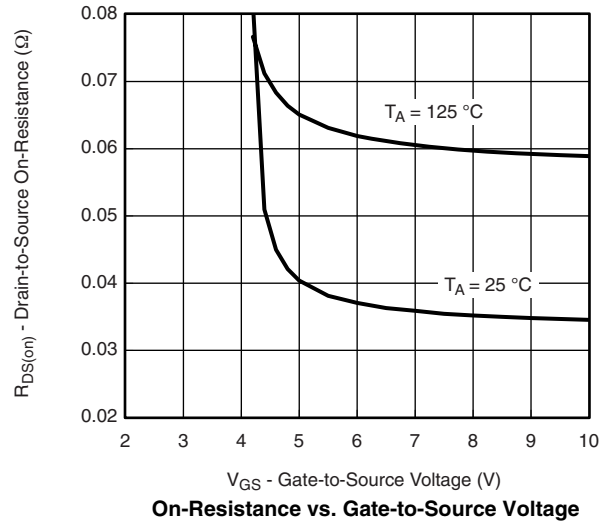
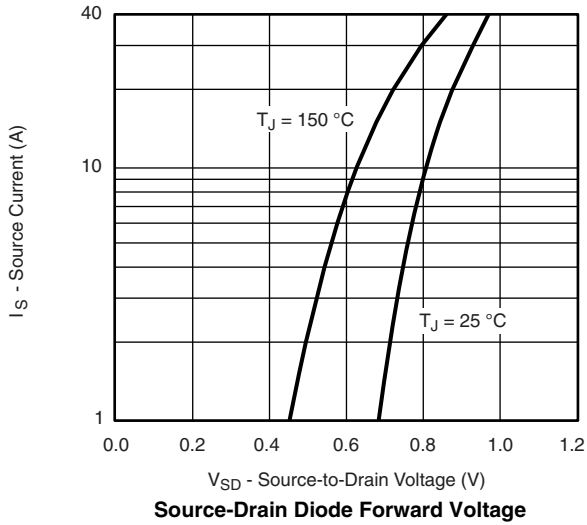
On-Resistance vs. Junction Temperature

SUP40P10-43



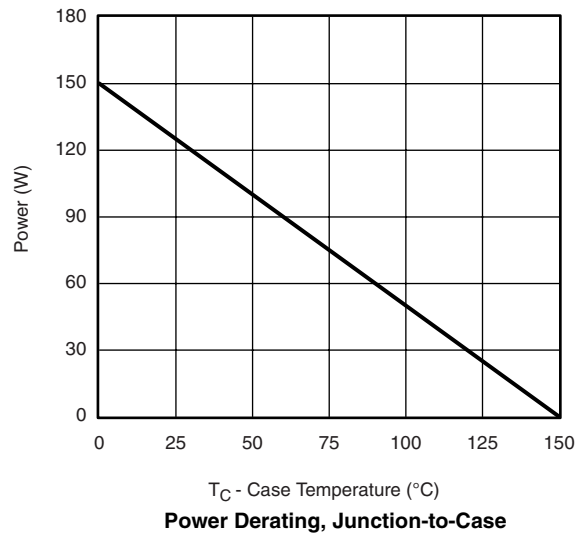
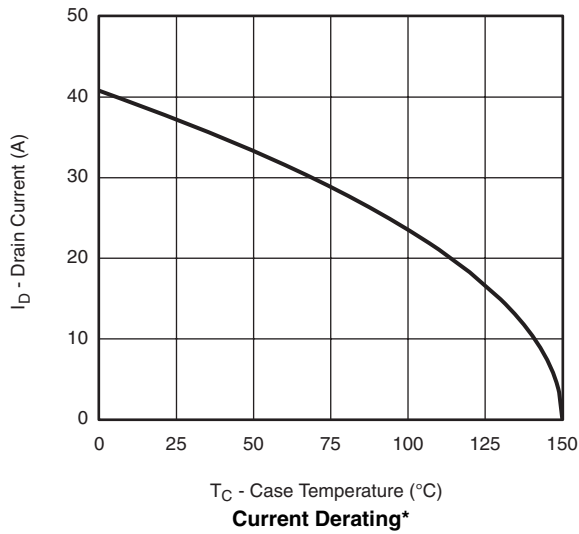
Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

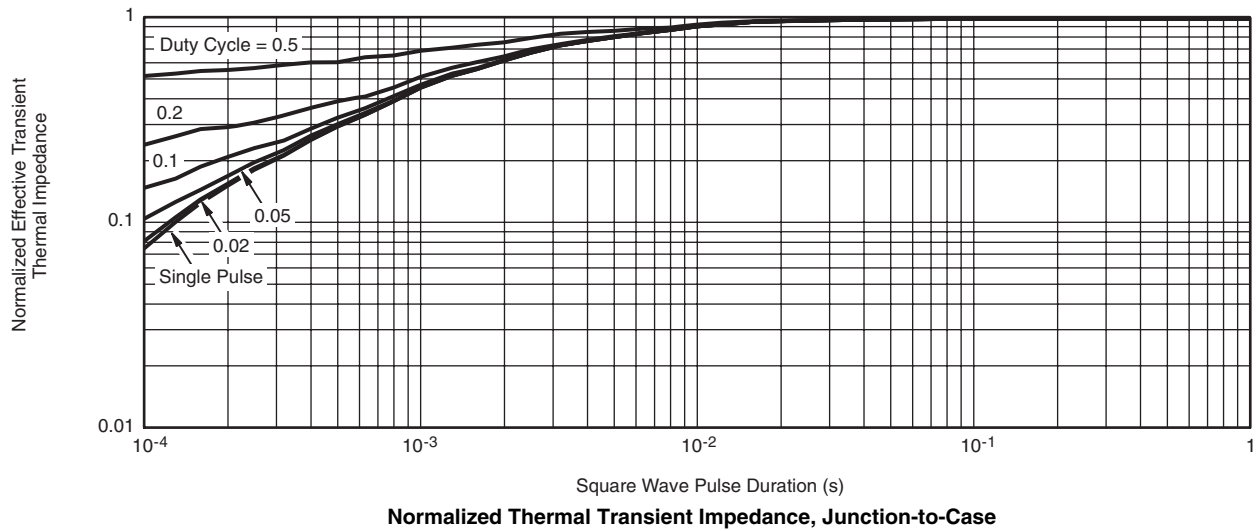




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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