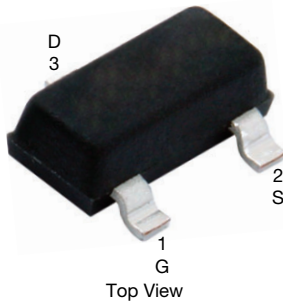


N-Channel 30 V (D-S) MOSFET

SOT-23 (TO-236)



Marking code: P2

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.068
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.085
Q_g typ. (nC)	3
I_D (A) ^a	3.6
Configuration	Single

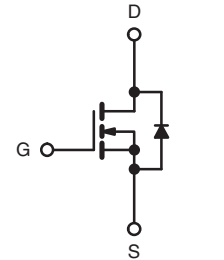
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- DC/DC converter for portable devices
- Load switch



N-Channel MOSFET

ORDERING INFORMATION	
Package	SOT-23
Lead (Pb)-free and halogen-free	Si2300DS-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	3.6 ^a	A
	$T_C = 70$ °C		3	
	$T_A = 25$ °C		3.1 ^{b, c}	
	$T_A = 70$ °C		2.5 ^{b, c}	
Pulsed drain current		I_{DM}	15	
Continuous source-drain diode current	$T_C = 25$ °C	I_S	1.4	A
	$T_A = 25$ °C		0.9 ^{b, c}	
Maximum power dissipation	$T_C = 25$ °C	P_D	1.7	W
	$T_C = 70$ °C		1.1	
	$T_A = 25$ °C		1.1 ^{b, c}	
	$T_A = 70$ °C		0.7 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	$t \leq 5$ s	R_{thJA}	90	115	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	60	75	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 130 °C/W



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	21	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-3.2	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6	-	1.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$	-	0.055	0.068	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 2.6\text{ A}$	-	0.070	0.085	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 2.9\text{ A}$	-	13	-	S
Dynamic ^b						
Input capacitance	C_{ISS}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	320	-	pF
Output capacitance	C_{OSS}		-	45	-	
Reverse transfer capacitance	C_{RSS}		-	19	-	
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 3.1\text{ A}$	-	6.5	10	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 3.1\text{ A}$	-	3	4.5	
Gate-source charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 3.1\text{ A}$	-	0.8	-	
Gate-drain charge	Q_{gd}		-	0.5	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.6	3.2	6.4	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong 2.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	10	15	ns
Rise time	t_r		-	15	25	
Turn-off delay time	$t_{d(off)}$		-	20	30	
Fall time	t_f		-	11	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 6\text{ }\Omega$ $I_D \cong 2.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	5	10	
Rise time	t_r		-	12	20	
Turn-off delay time	$t_{d(off)}$		-	15	25	
Fall time	t_f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	1.4	A
Pulse diode forward current	I_{SM}		-	-	15	
Body diode voltage	V_{SD}	$I_S = 2.5\text{ A}, V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = 2.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	11	20	ns
Body diode reverse recovery charge	Q_{rr}		-	5	10	nC
Reverse recovery fall time	t_a		-	7	-	ns
Reverse recovery rise time	t_b		-	4	-	

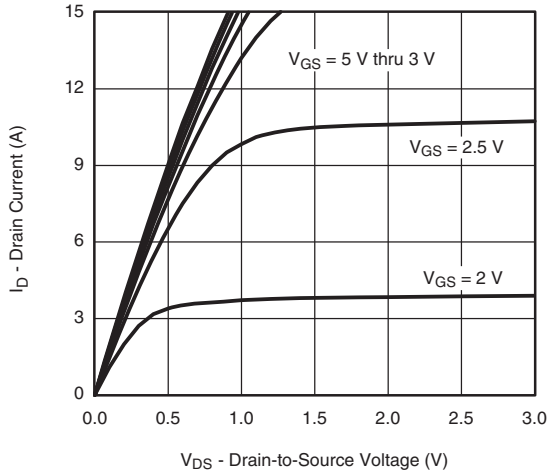
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

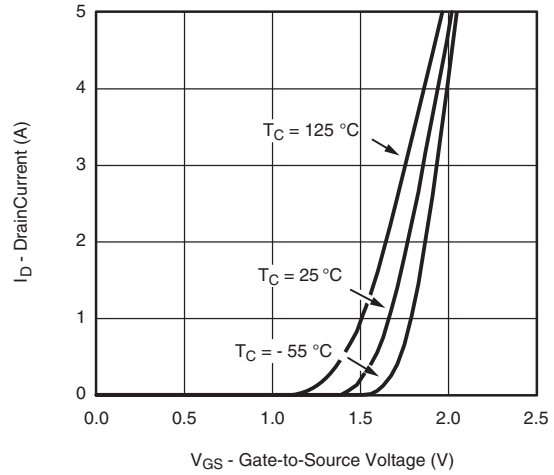
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



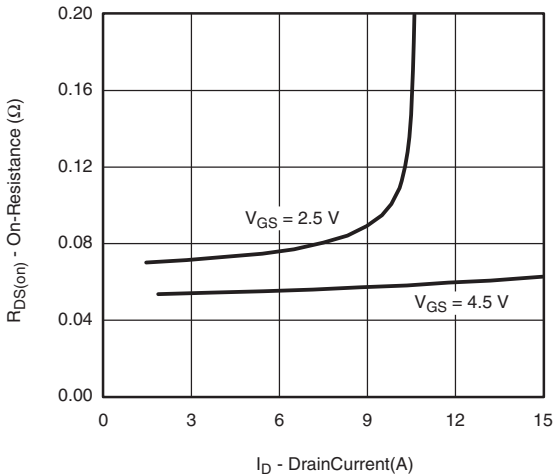
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



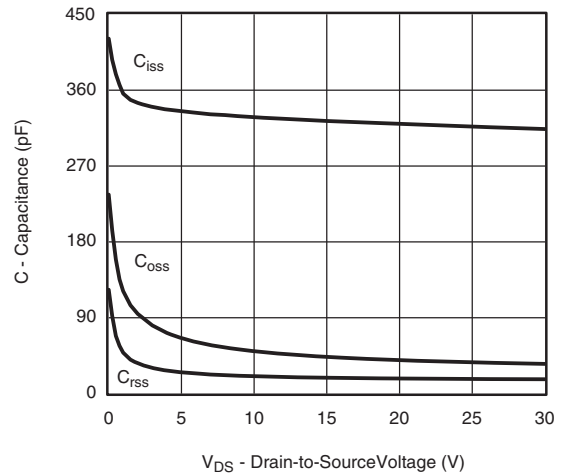
Output Characteristics



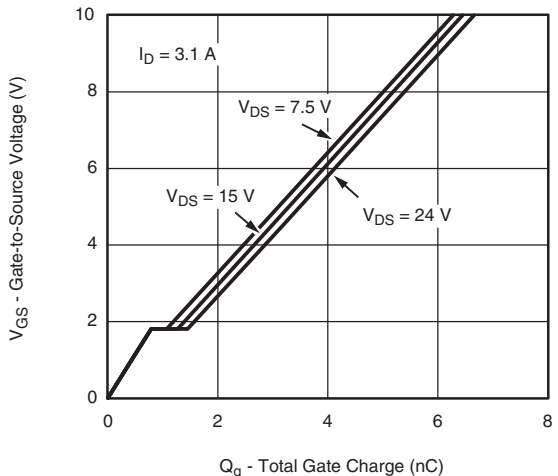
Transfer Characteristics



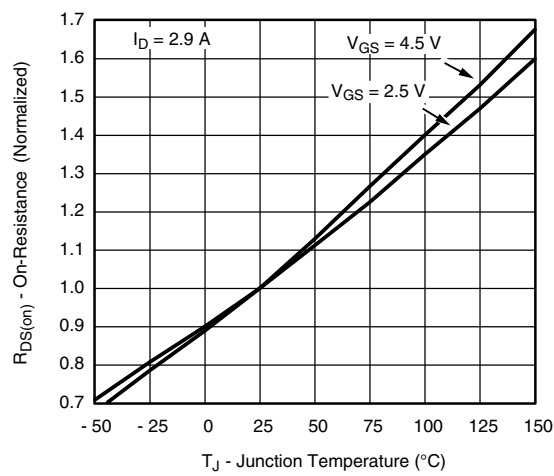
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



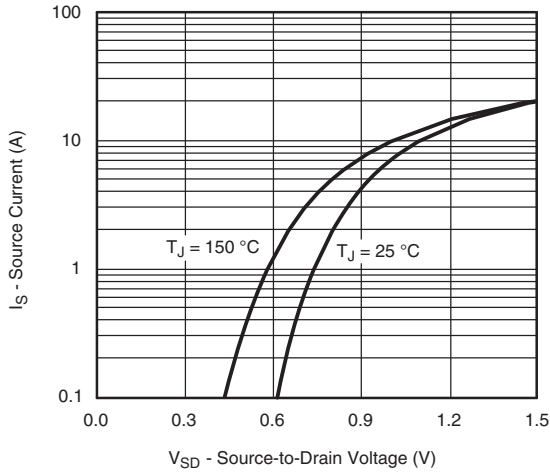
Gate Charge



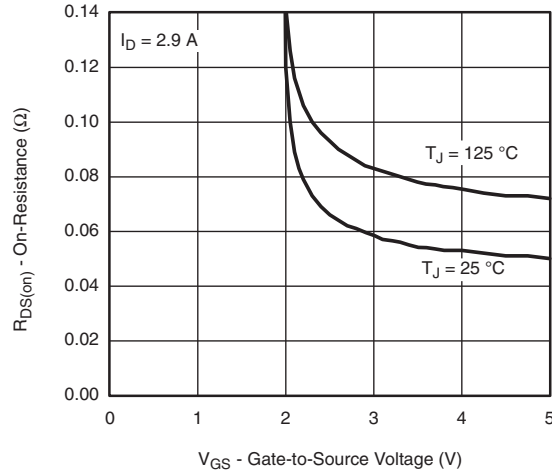
On-Resistance vs. Junction Temperature



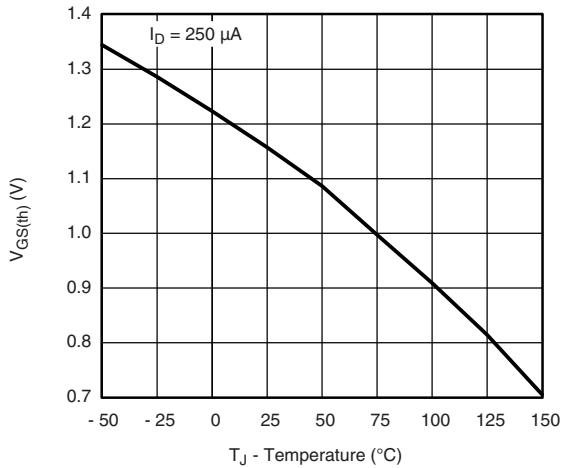
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



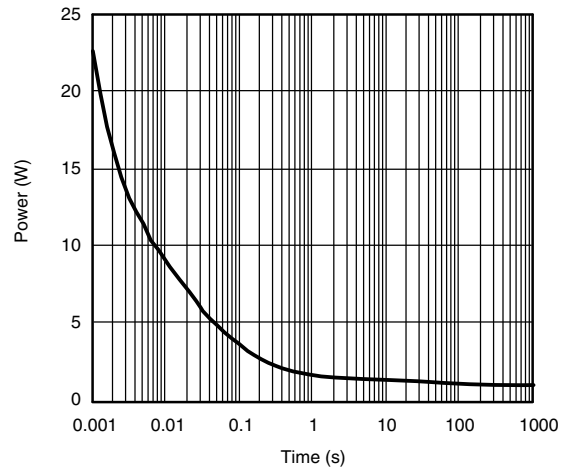
Source-Drain Diode Forward Voltage



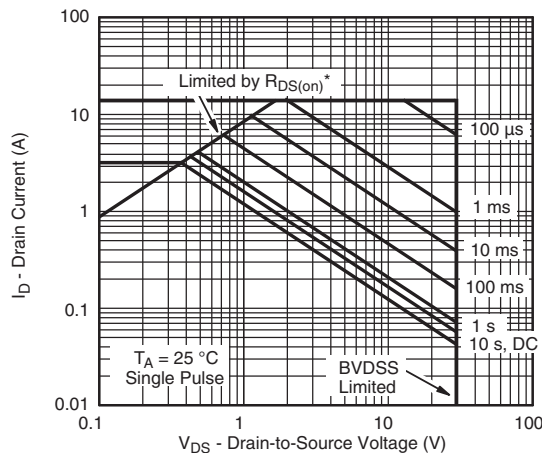
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



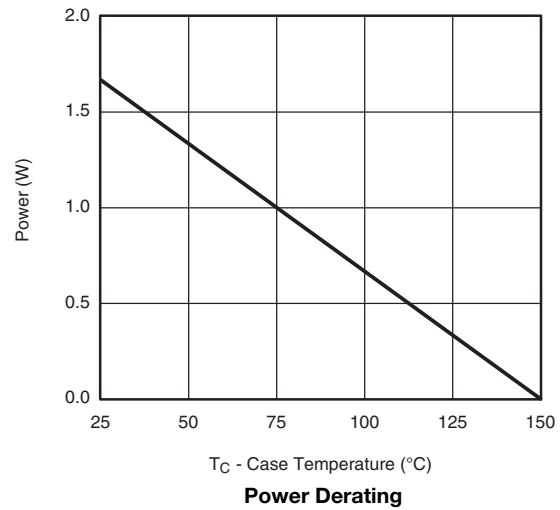
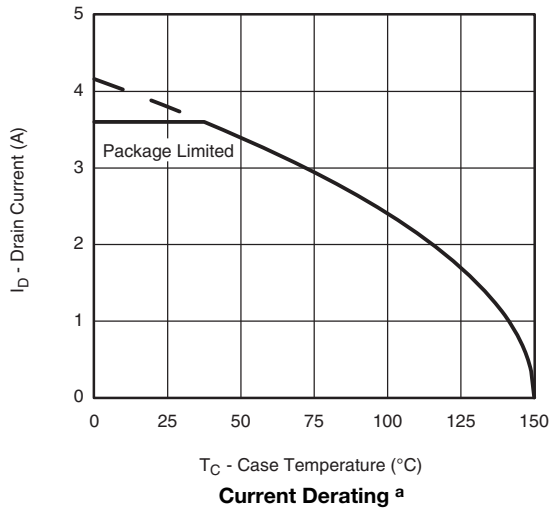
Single Pulse Power



Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

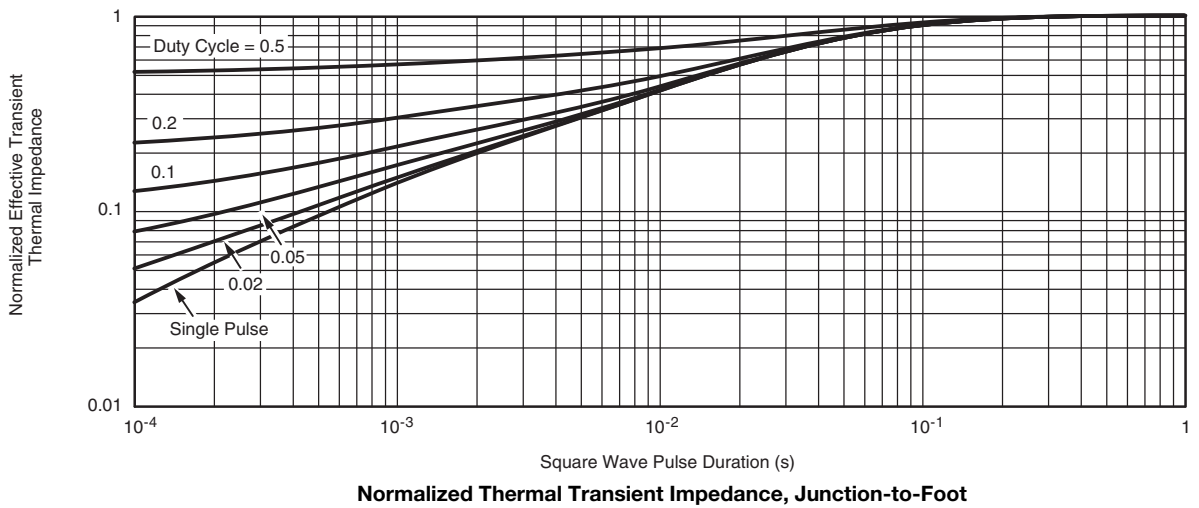
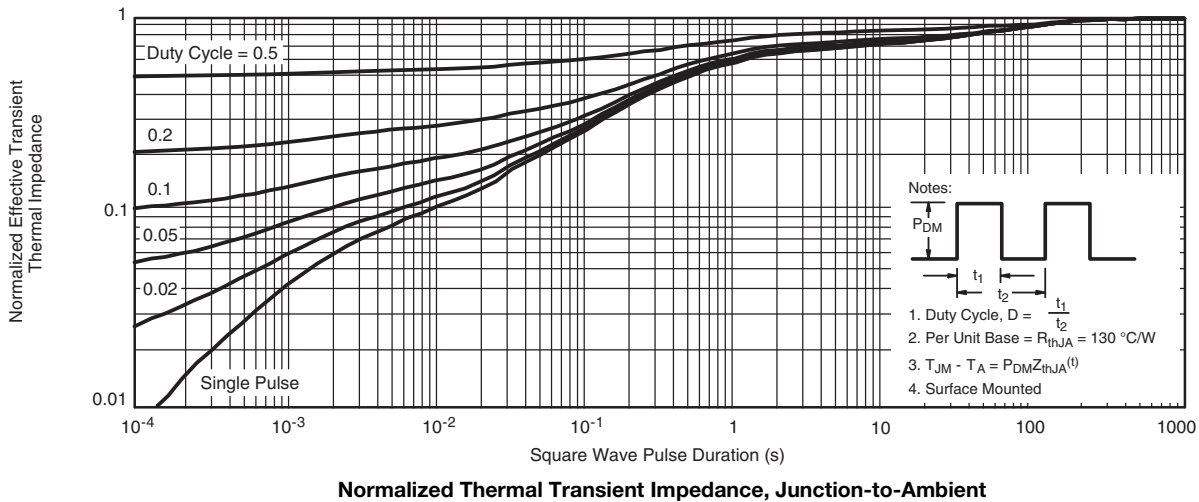


Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65701.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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