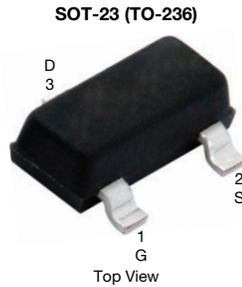


P-Channel 20 V (D-S) MOSFET



Marking Code: P6

PRODUCT SUMMARY	
V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.061
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.080
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8$ V	0.110
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.5$ V	0.165
Q_g typ. (nC)	7.6
I_D (A) ^a	-4.4
Configuration	Single

ORDERING INFORMATION	
Package	SOT-23
Lead (Pb)-free and halogen-free	Si2377EDS-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-20	V
Gate-source voltage	V_{GS}	± 8	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-4.4
		$T_C = 70$ °C	3.5
		$T_A = 25$ °C	-3.7 ^{b, c}
		$T_A = 70$ °C	-2.9 ^{b, c}
Pulsed drain current	I_{DM}	-20	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	-1 ^{b, c}
Maximum power dissipation	P_D	$T_C = 25$ °C	1.8
		$T_C = 70$ °C	1.1
		$T_A = 25$ °C	1.25 ^{b, c}
		$T_A = 70$ °C	0.8 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	$t \leq 5$ s	R_{thJA}	80	100	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	55	70	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 130 °C/W

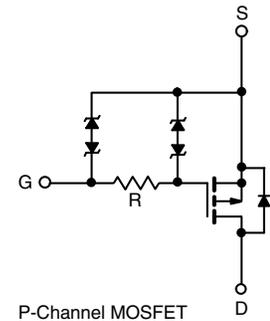
FEATURES

- TrenchFET® power MOSFET
- 100% R_g tested
- Typical ESD performance 2000 V
- Built in ESD protection with Zener Diode
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- Load switch for portable devices





SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-13	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	2.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.4	-	-1	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 6	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 0.5	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-15	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.2 A	-	0.050	0.061	Ω
		V _{GS} = -2.5 V, I _D = -2.8 A	-	0.065	0.080	
		V _{GS} = -1.8 V, I _D = -1.5 A	-	0.090	0.110	
		V _{GS} = -1.5 V, I _D = -0.5 A	-	0.110	0.165	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -3.2 A	-	12	-	S
Dynamic ^b						
Total gate charge	Q _g	V _{DS} = -10 V, V _{GS} = -8 V, I _D = -5.3 A	-	14	21	nC
		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5.3 A	-	7.6	12	
			-	0.8	-	
Gate-source charge	Q _{gs}	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5.3 A	-	3.1	-	nC
Gate-drain charge	Q _{gd}		-	-	-	
Gate resistance	R _g	f = 1 MHz	0.4	2	4	kΩ
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.3 Ω I _D ≅ -4.3 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	0.2	0.3	μs
Rise time	t _r		-	1	1.5	
Turn-off delay time	t _{d(off)}		-	4	6	
Fall time	t _f		-	2	3	
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.3 Ω I _D ≅ -4.3 A, V _{GEN} = -8 V, R _g = 1 Ω	-	0.09	0.14	
Rise time	t _r		-	0.4	0.6	
Turn-off delay time	t _{d(off)}		-	5.2	7.8	
Fall time	t _f		-	2.3	3.5	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-1.5	A
Pulse diode forward current	I _{SM}		-	-	-20	
Body diode voltage	V _{SD}	I _S = -3 A, V _{GS} = 0 V	-	-0.8	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -3 A, di/dt = 100 A/μs, T _J = 25 °C	-	30	60	ns
Body diode reverse recovery charge	Q _{rr}		-	20	40	nC
Reverse recovery fall time	t _a		-	13	-	ns
Reverse recovery rise time	t _b		-	17	-	

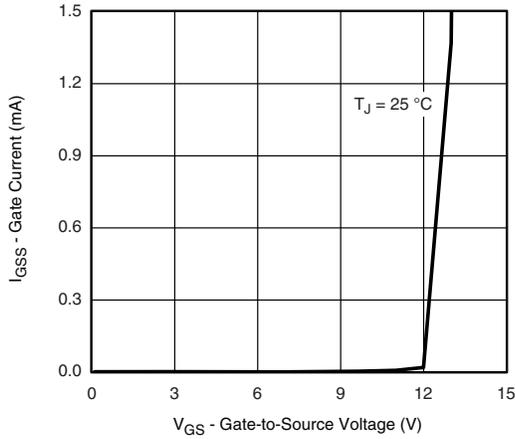
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%
- b. Guaranteed by design, not subject to production testing

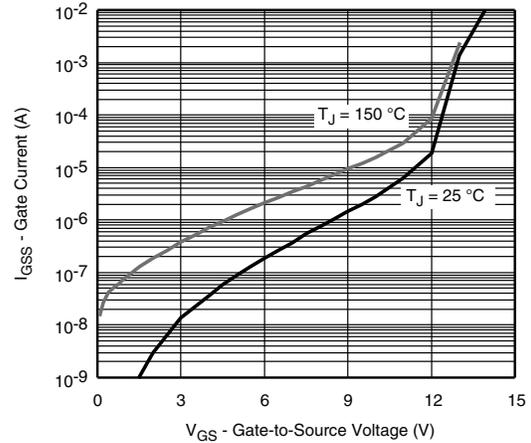
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



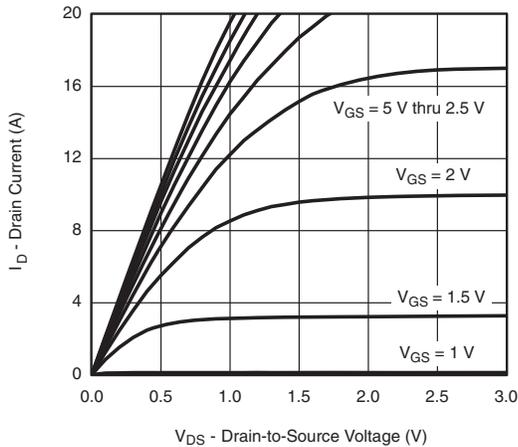
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



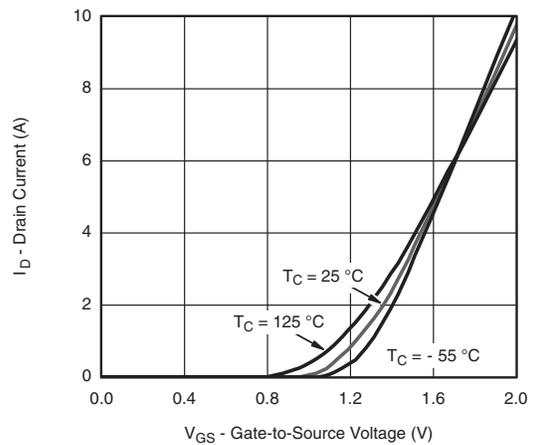
Gate Current vs. Gate-Source Voltage



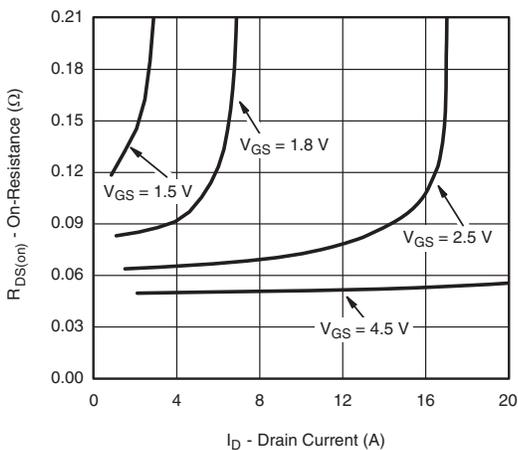
Gate Current vs. Gate-Source Voltage



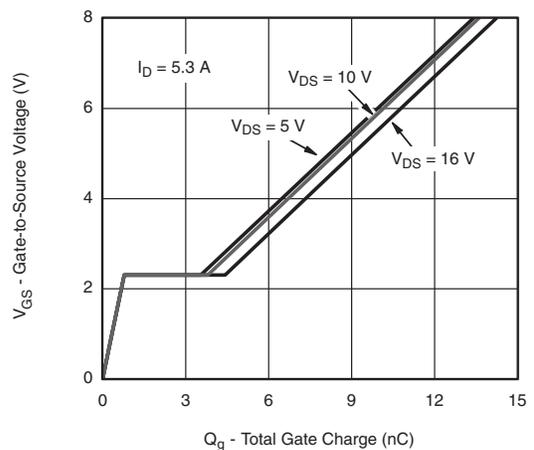
Output Characteristics



Transfer Characteristics



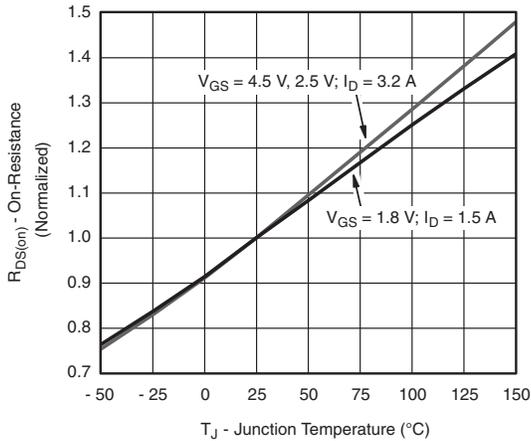
On-Resistance vs. Drain Current



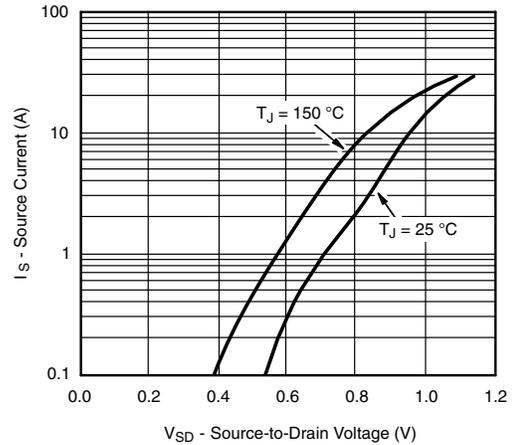
Gate Charge



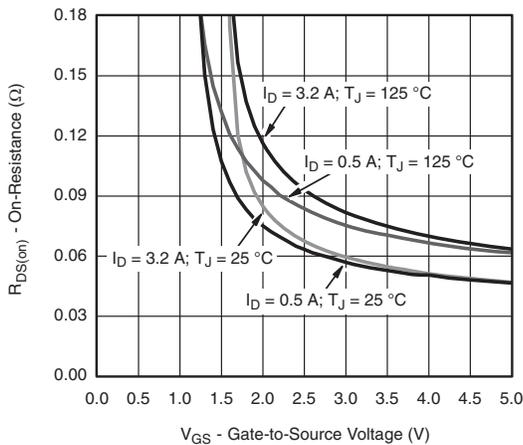
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



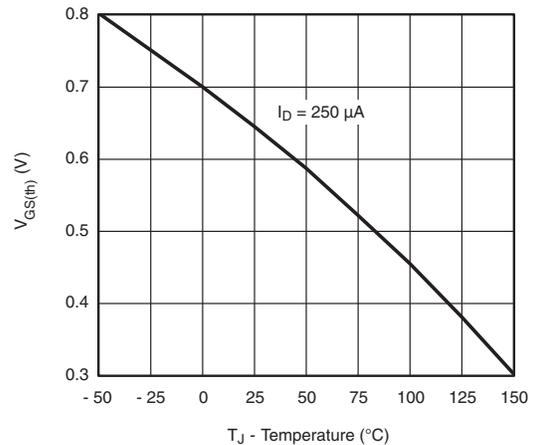
On-Resistance vs. Junction Temperature



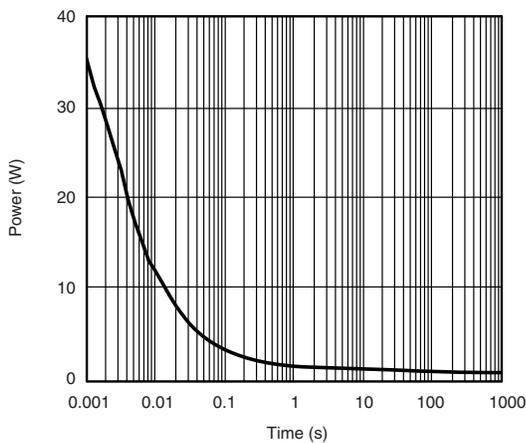
Source-Drain Diode Forward Voltage



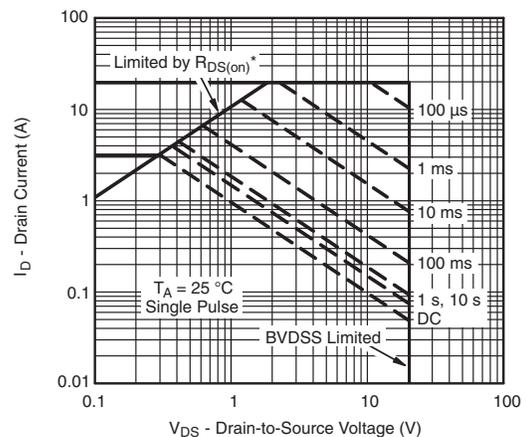
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

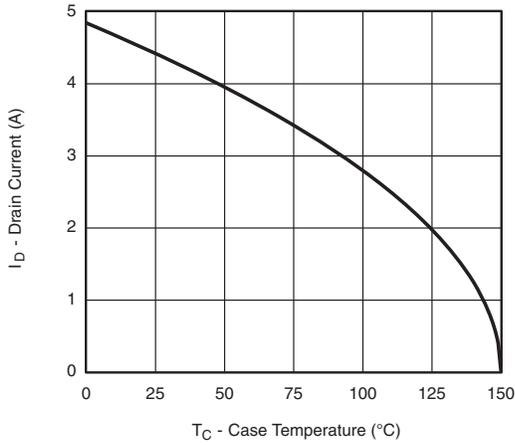


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

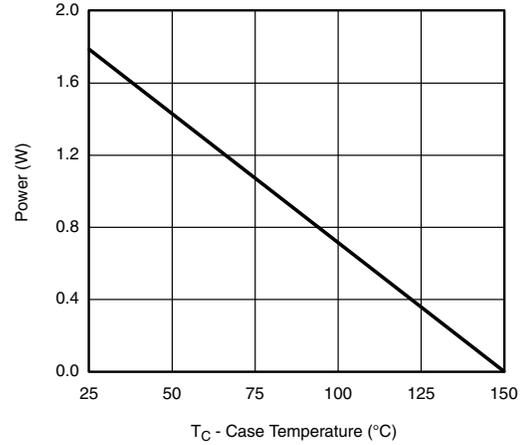
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



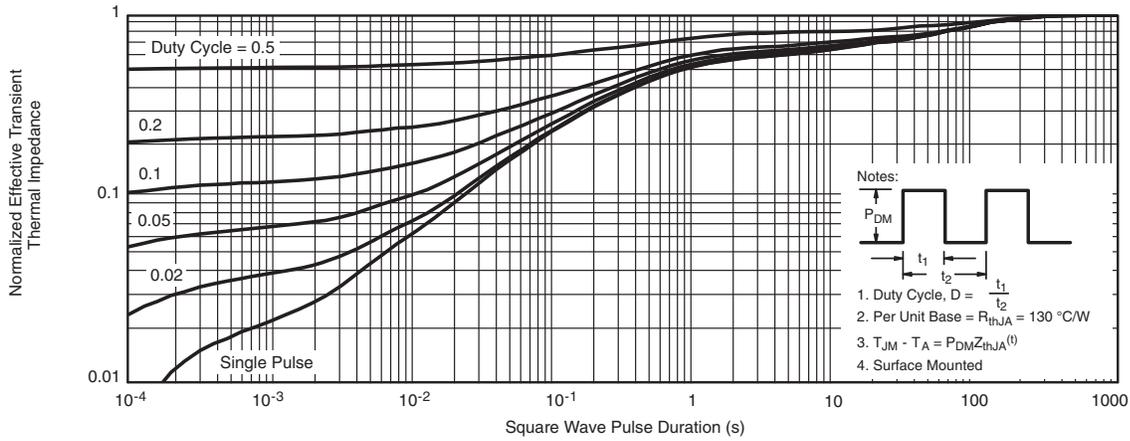
Power Derating

Note

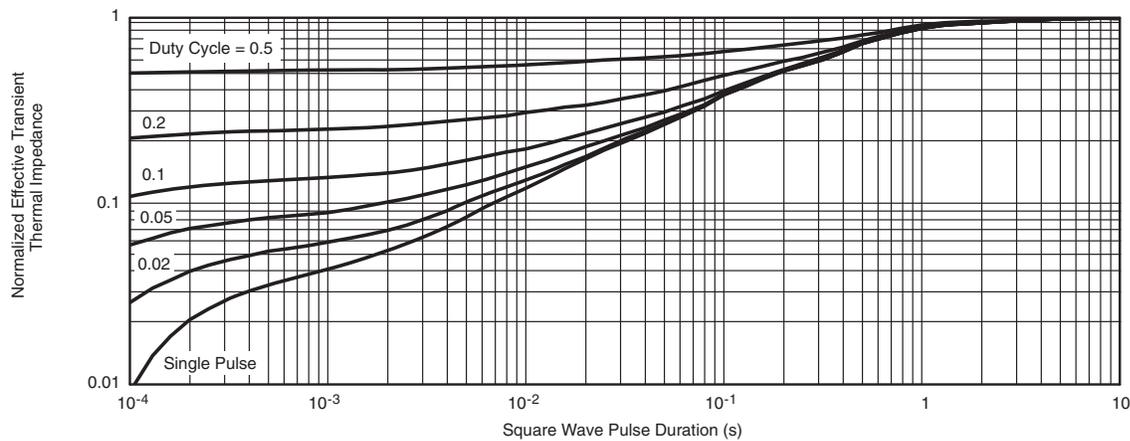
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150 \text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



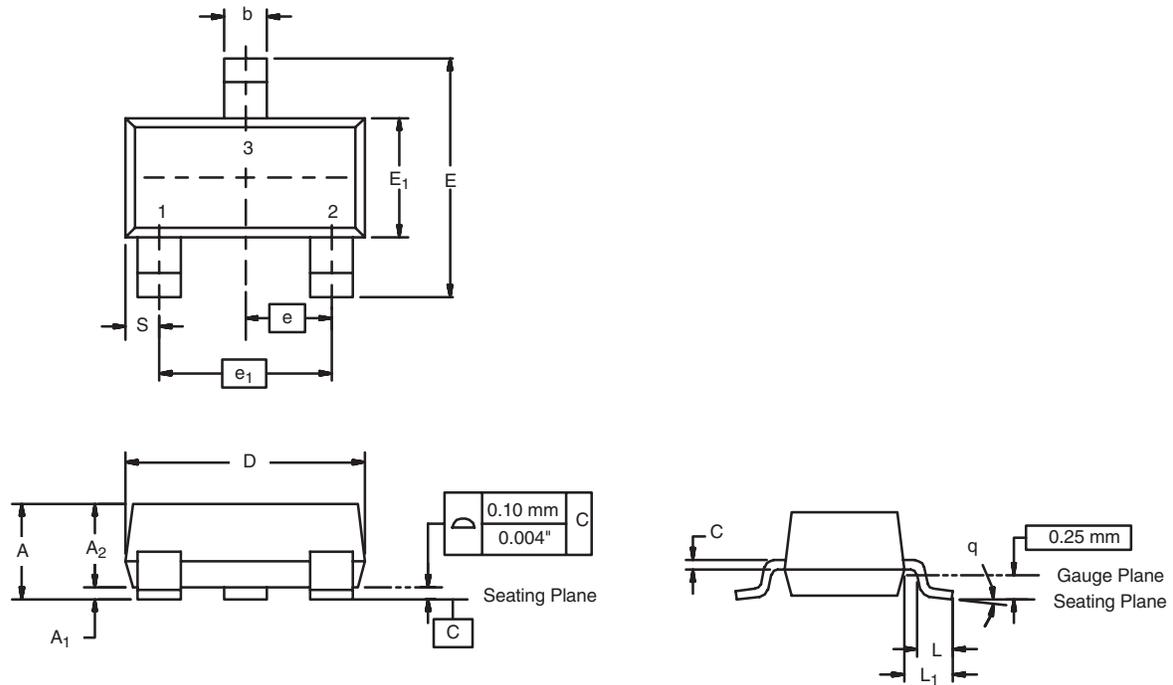
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65905.

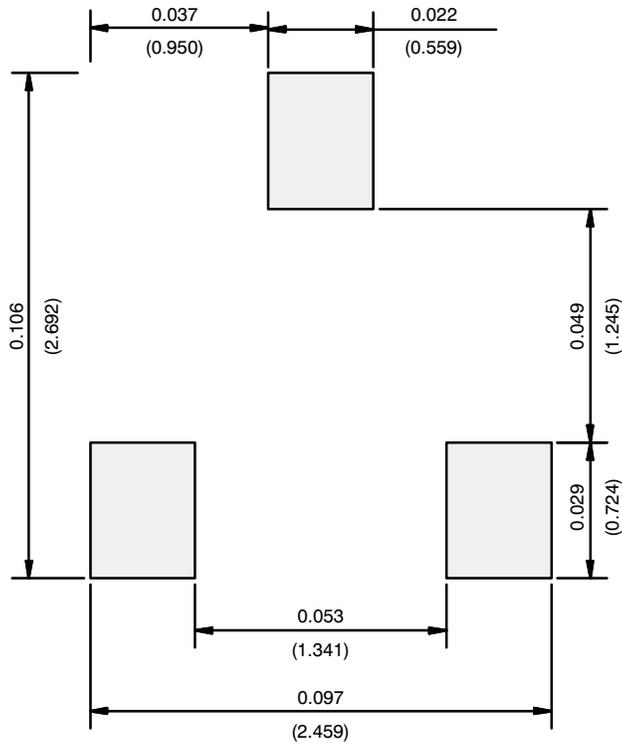
SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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