Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.054 at V_{GS} = - 4.5 V	- 4.5[a]	9.5 nC
	0.070 at V_{GS} = - 2.5 V	- 4.5[a]	
	0.104 at V_{GS} = - 1.8 V	- 4.5[a]	
	0.165 at V_{GS} = - 1.5 V	- 1.5	

FEATURES

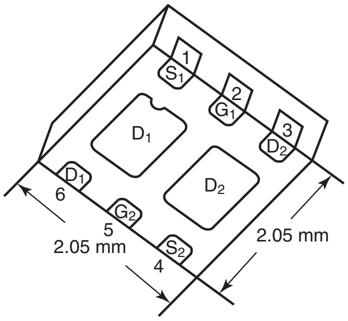
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- Typical ESD Protection: 2500 V
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

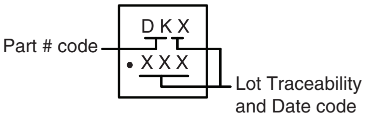
APPLICATIONS

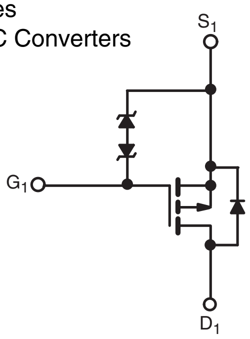
- Charger Switches and Load Switches for Portable Devices
- DC/DC Converters

PowerPAK SC-70-6 Dual

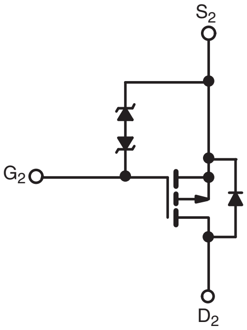


Marking Code





P-Channel MOSFET



P-Channel MOSFET

Ordering Information: SiA923EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 4.5[a]	A
	T_C = 70 °C		- 4.5[a]	
	T_A = 25 °C		- 4.5[a, b, c]	
	T_A = 70 °C		- 4.5[a, b, c]	
Pulsed Drain Current		I_{DM}	- 15	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 4.5[a]	
	T_A = 25 °C		- 1.6[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	W
	T_C = 70 °C		5	
	T_A = 25 °C		1.9[b, c]	
	T_A = 70 °C		1.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	

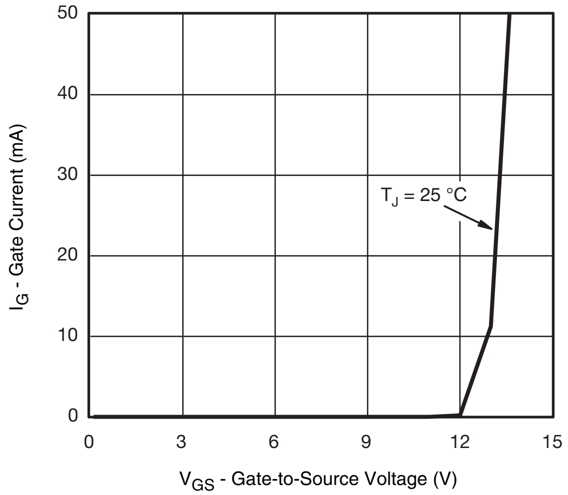
Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 110 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

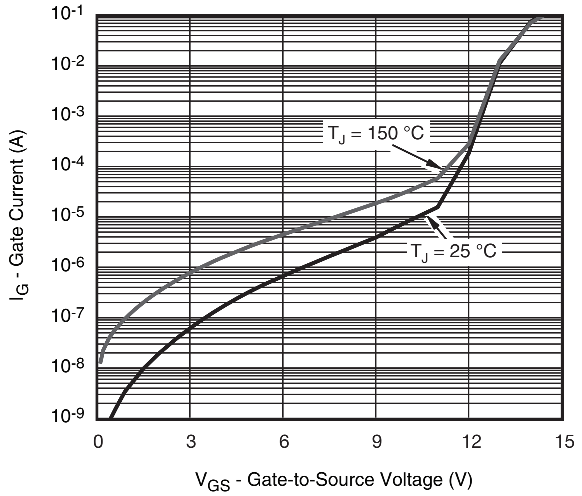
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = - 250$ µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = - 250$ µA		- 15		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = - 250$ µA	- 0.5		- 1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V		± 0.3	± 3	µA
		$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V		± 3	± 30	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = - 20$ V, $V_{GS} = 0$ V			- 1	
		$V_{DS} = - 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq - 5$ V, $V_{GS} = - 4.5$ V	- 15			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	$V_{GS} = - 4.5$ V, $I_D = - 3.8$ A		0.044	0.054	Ω
		$V_{GS} = - 2.5$ V, $I_D = - 3.3$ A		0.057	0.070	
		$V_{GS} = - 1.8$ V, $I_D = - 1$ A		0.075	0.104	
		$V_{GS} = - 1.5$ V, $I_D = - 0.5$ A		0.097	0.165	
Forward Transconductance[a]	g_{fs}	$V_{DS} = - 10$ V, $I_D = - 3.8$ A		11		S
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = - 10$ V, $V_{GS} = - 8$ V, $I_D = - 4.9$ A		16.3	25	nC
		$V_{DS} = - 10$ V, $V_{GS} = - 4.5$ V, $I_D = - 4.9$ A		9.5	14.5	
Gate-Source Charge	Q_{gs}			1.4		
Gate-Drain Charge	Q_{gd}			2.3		
Gate Resistance	R_g	f = 1 MHz	1	5.1	10	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = - 10$ V, $R_L = 2.6$ Ω $I_D \cong - 3.9$ A, $V_{GEN} = - 4.5$ V, $R_g = 1$ Ω		15	25	ns
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = - 10$ V, $R_L = 2.6$ Ω $I_D \cong - 3.9$ A, $V_{GEN} = - 8$ V, $R_g = 1$ Ω		7	15	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			26	40	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			- 4.5	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	$I_S = - 3.9$ A, $V_{GS} = 0$ V		- 0.9	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = - 3.9$ A, dI/dt = 100 A/µs, $T_J = 25$ °C		13	25	ns
Body Diode Reverse Recovery Charge	Q_{rr}			5.5	12	nC
Reverse Recovery Fall Time	t_a			7.5		ns
Reverse Recovery Rise Time	t_b			5.5		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

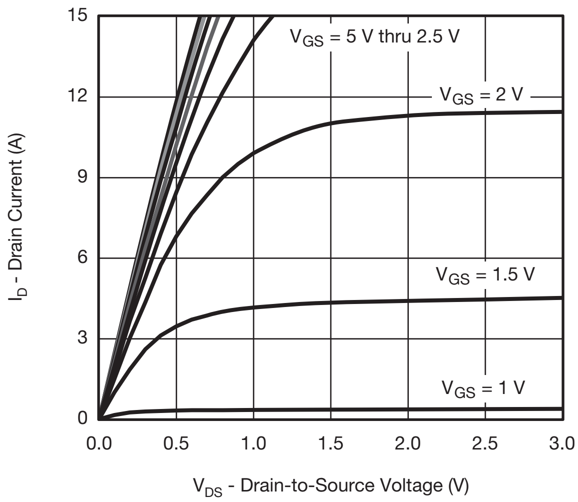
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



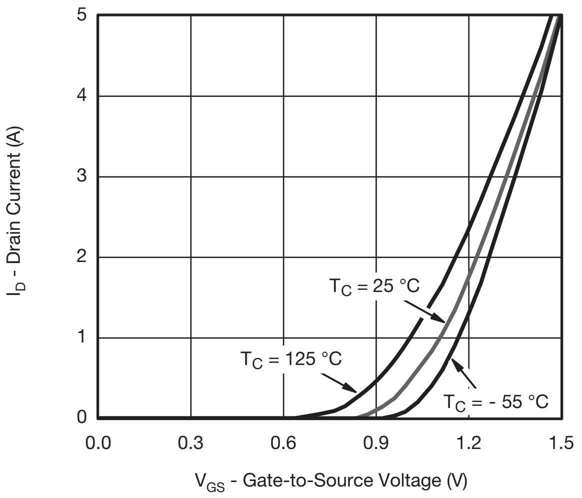
Gate Current vs. Gate-to-Source Voltage



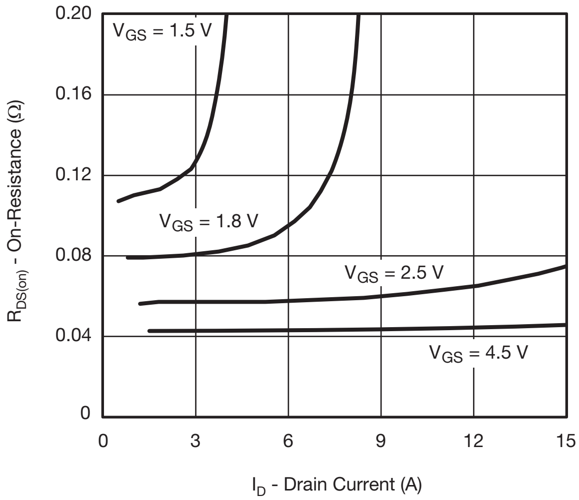
Gate Current vs. Gate-to-Source Voltage



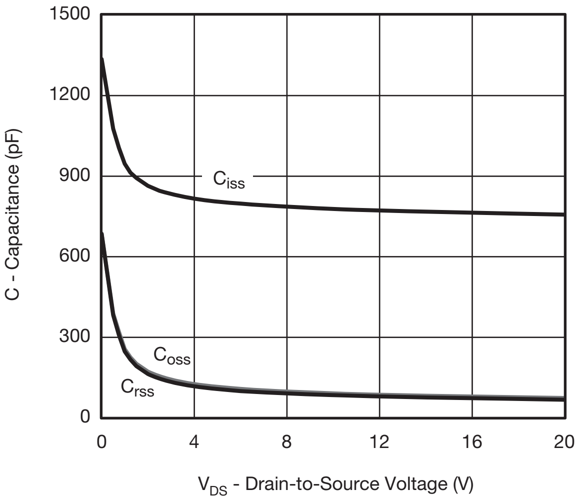
Output Characteristics



Transfer Characteristics

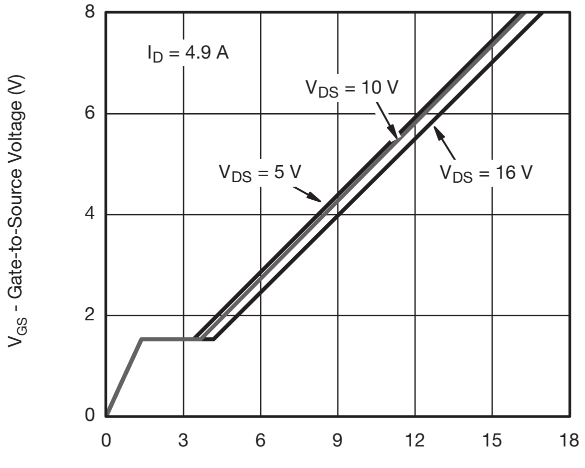


On-Resistance vs. Drain Current and Gate Voltage

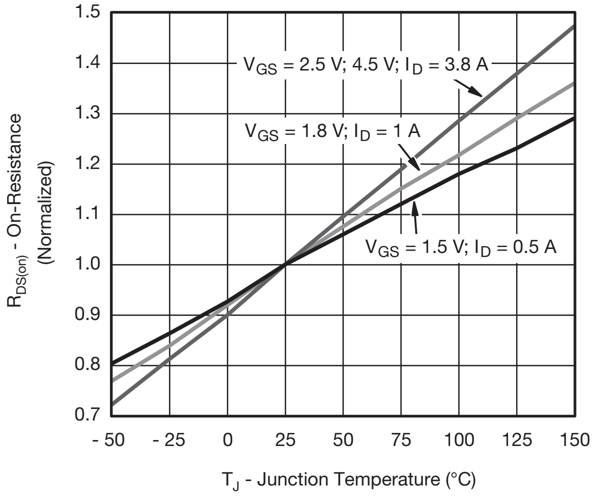


Capacitance

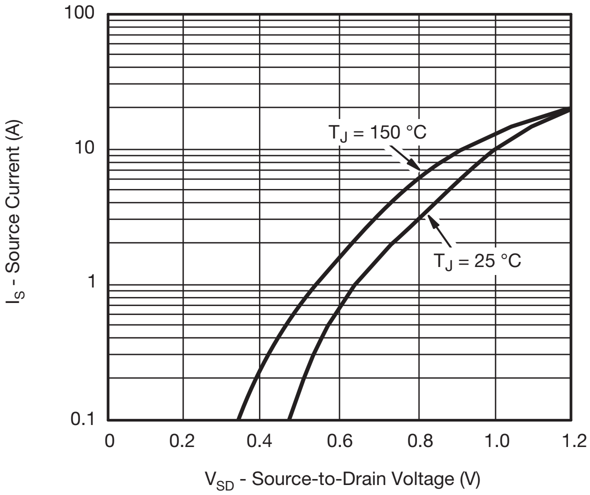
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



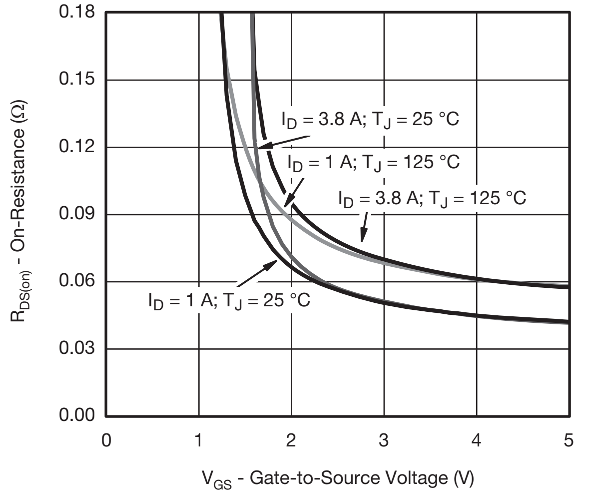
Gate Charge



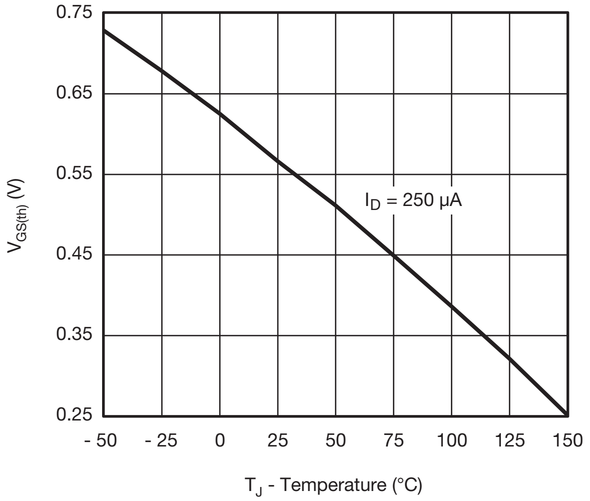
On-Resistance vs. Junction Temperature



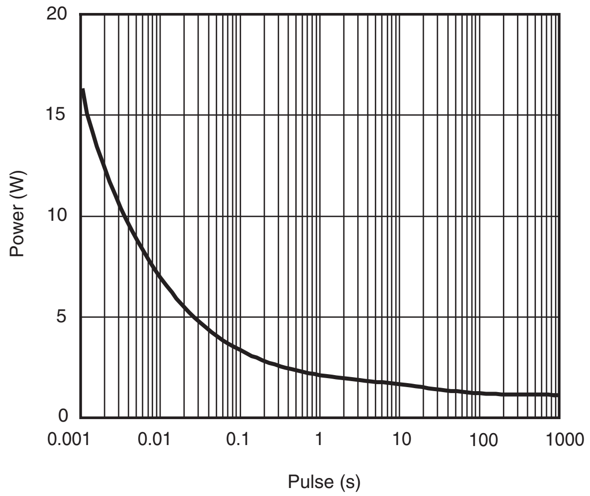
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

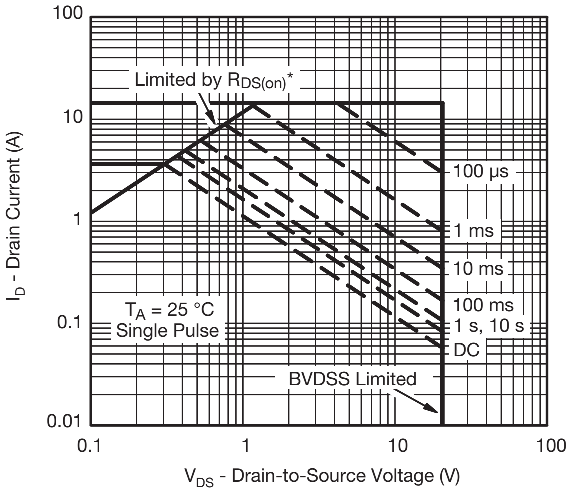


Threshold Voltage



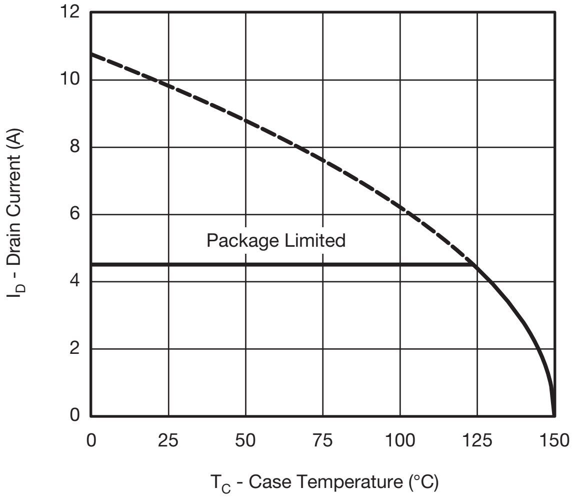
Single Pulse Power, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

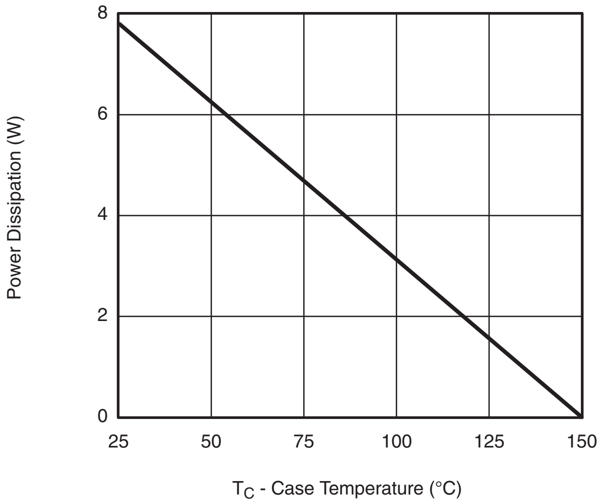


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



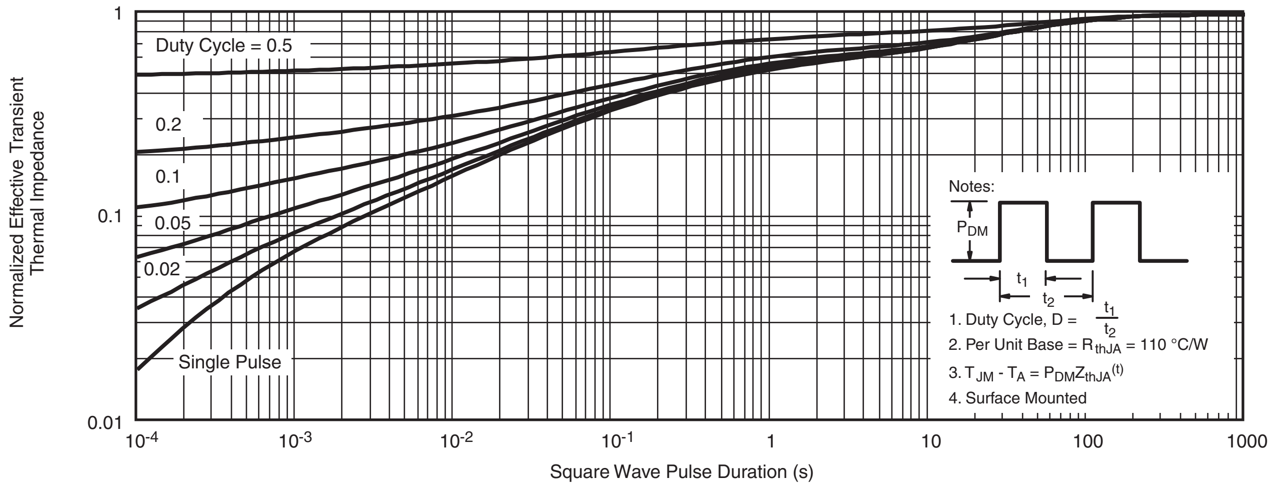
Current Derating*



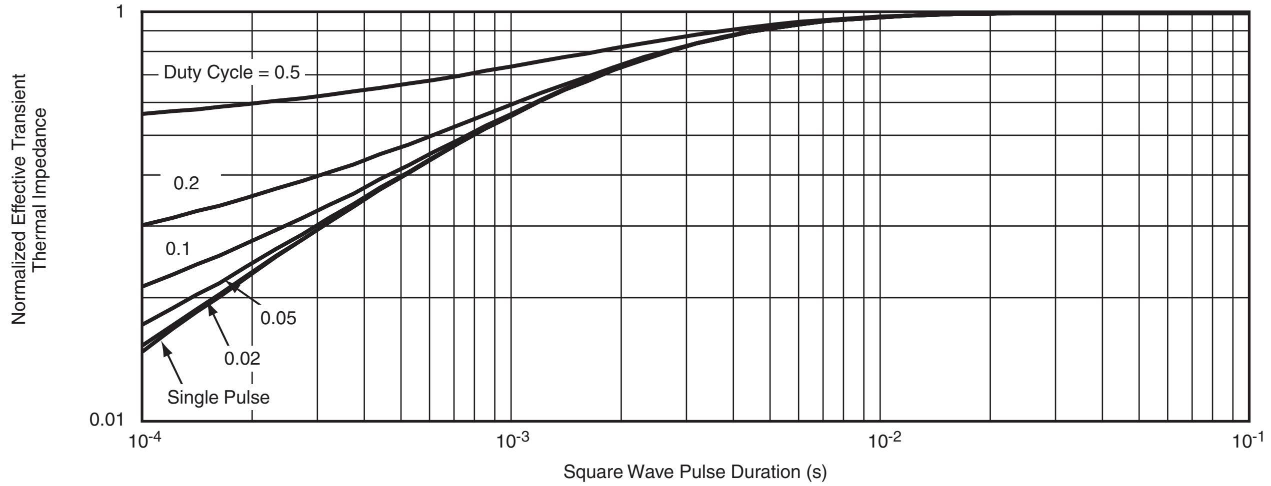
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

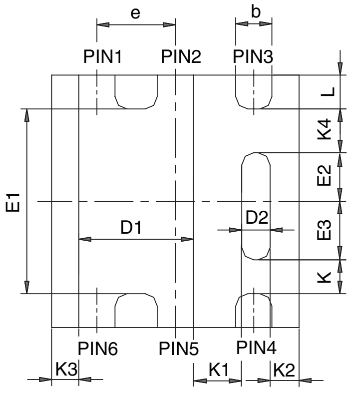


Normalized Thermal Transient Impedance, Junction-to-Ambient

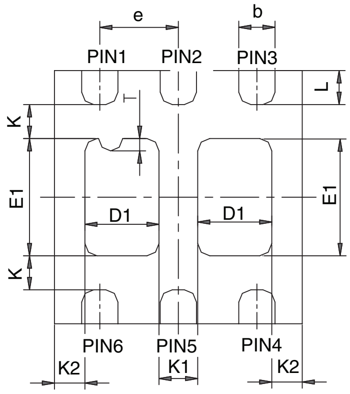


Normalized Thermal Transient Impedance, Junction-to-Case

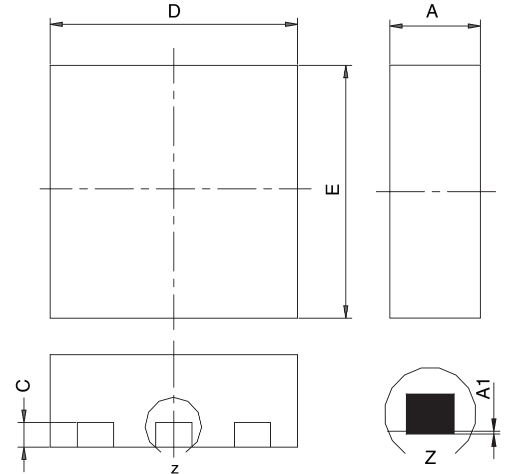
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



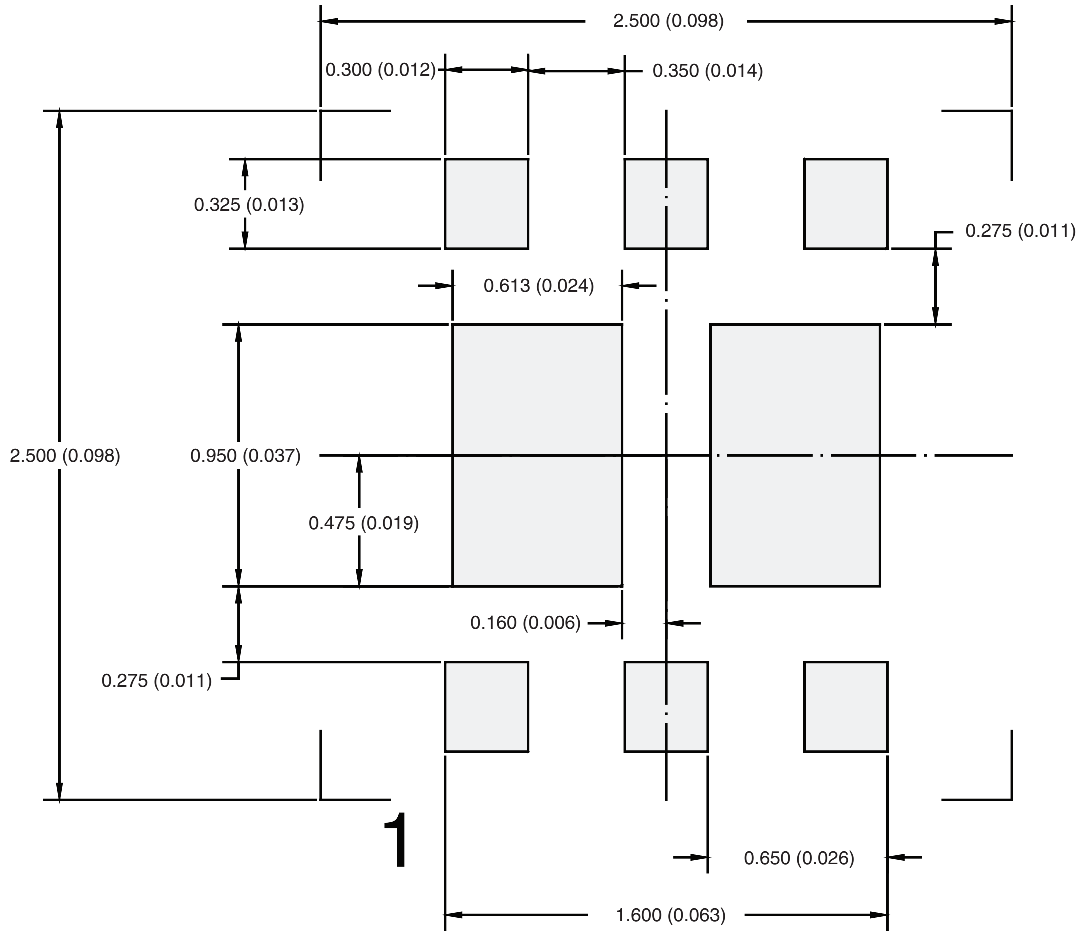
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

Return to Index

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