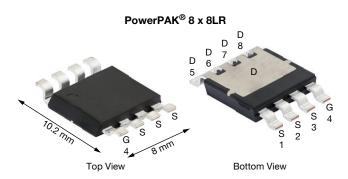
SQJQ112ER

SHAY. www.vishay.com

Vishay Siliconix

Automotive N-Channel 100 V (D-S) 175 °C MOSFET



FEATURES

- TrenchFET[®] Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

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N-Channel MOSFET



PRODUCT SUMMARY			
V _{DS} (V)	100		
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.00253		
I _D (A)	296		
Configuration	Single		

ORDERING INFORMATION				
Package	PowerPAK 8 x 8LR			
Lead (Pb)-free and halogen-free	SQJQ112ER (for detailed order number please see <u>www.vishav.com/doc?79776</u>)			

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	100	v		
Gate-source voltage		V _{GS}	± 20	v		
Continuous drain current	T _C = 25 °C	I_	296			
	T _C = 125 °C	I _D	171			
Continuous source current (diode conduction) Pulsed drain current ^a		I _S	545	A		
		I _{DM}	655			
Single pulse avalanche current	L = 0.1 mH	I _{AS}	69			
Single pulse avalanche energy		E _{AS}	242	mJ		
Maximum power dissipation	T _C = 25 °C	Р	600	w		
	T _C = 125 °C	P _D	200	vv		
Operating junction and storage temperature range Soldering recommendations (peak temperature) ^c		T _J , T _{stg} -55 to +175				
			260			

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient	PCB mount ^b	R _{thJA}	40	°C/W	
Junction-to-case (drain)		R _{thJC}	0.25	C/W	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$

b. When mounted on 1" square PCB (FR4 material)

c. See solder profile (www.vishay.com/doc?73257)

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SPECIFICATIONS ($T_C = 25 \text{ °C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \ \mu A$		100	-	-	v	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		2	3	3.5	v	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 100 V	-	-	1	μA	
Zero gate voltage drain current		$V_{GS} = 0 V$	$V_{DS} = 100 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50		
		$V_{GS} = 0 V$	V_{DS} = 100 V, T _J = 175 °C	-	-	500		
On-state drain current ^a	I _{D(on)}	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	50	-	-	Α	
		$V_{GS} = 10 V$	I _D = 20 A	-	0.0021	0.00253		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 10 V$	$I_D = 20 \text{ A}, \text{T}_\text{J} = 125 \ ^\circ\text{C}$	-	-	0.0054	Ω	
		$V_{GS} = 10 V$	I _D = 20 A, T _J = 175 °C	-	-	0.0068		
Forward transconductance ^b	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$		-	45	-	S	
Dynamic ^b								
Input capacitance	Ciss		: 0 V V _{DS} = 25 V, f = 1 MHz	-	11388	15 945	pF	
Output capacitance	Coss	$V_{GS} = 0 V$		-	1326	1857		
Reverse transfer capacitance	C _{rss}			-	80	112		
Total gate charge ^c	Qg			-	181	272		
Gate-source charge ^c	Q _{gs}	$V_{GS} = 10 \text{ V}$	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	1	48	-	nC	
Gate-drain charge ^c	Q _{gd}			I	37	-		
Gate resistance	Rg	f = 1 MHz		0.7	1.5	2.3	Ω	
Turn-on delay time ^c	t _{d(on)}			-	21	30		
Rise time ^c	t _r		= 50 V, R_L = 2.5 Ω,	-	16	24	ns	
Turn-off delay time ^c	t _{d(off)}	$I_D \cong 20 A$,	V_{GEN} = 10 V, R_g = 1 Ω	-	67	95		
Fall time ^c	t _f			-	16	24		
Source-Drain Diode Ratings and Charact	teristics ^b							
Pulsed current ^a	I _{SM}			-	-	655	А	
Forward voltage	V _{SD}	I _F = 40 A, V _{GS} = 0 V		-	0.7	1.2	V	
Body diode reverse recovery time	t _{rr}	- I _F = 15 A, di/dt = 100 A/μs		-	70	140	ns	
Body diode reverse recovery charge	Q _{rr}			-	172	344	nC	
Reverse recovery fall time	t _a			-	44	-		
Reverse recovery rise time	t _b			-	26	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			-	4.3	-	А	
Notes								

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

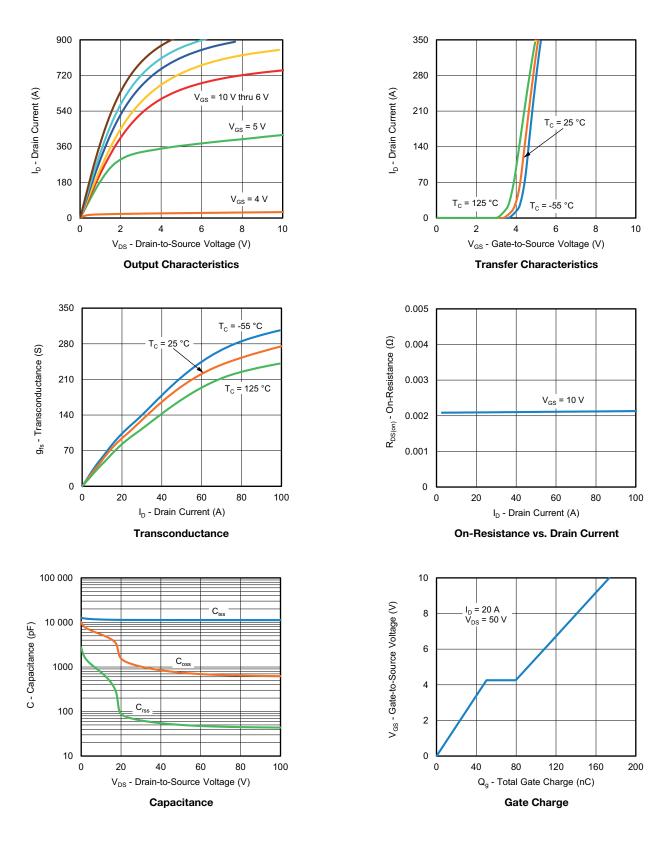
b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



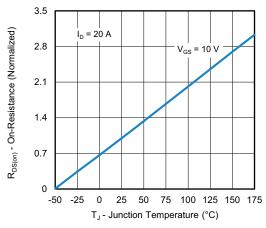
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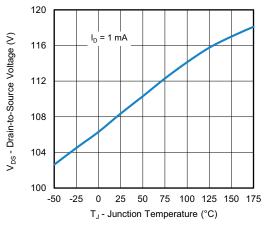
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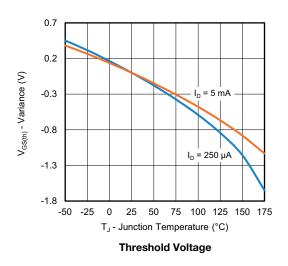
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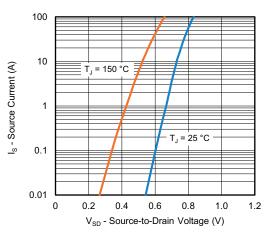


On-Resistance vs. Junction Temperature

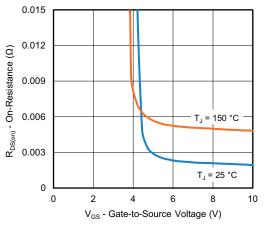


Drain Source Breakdown vs. Junction Temperature

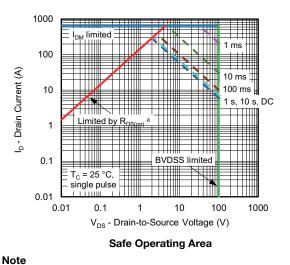




Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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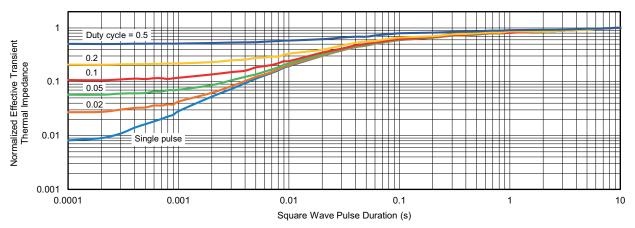
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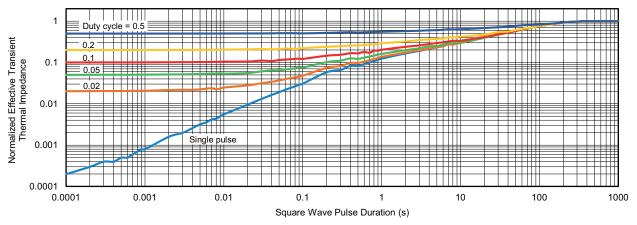
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

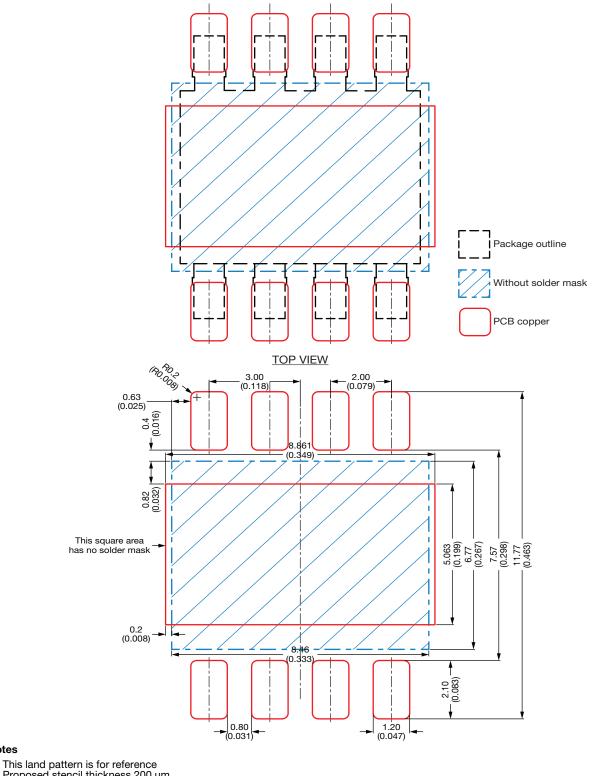
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PAD Pattern



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Recommended Land Pattern PowerPAK® 8 x 8LR



Proposed stencil thickness 200 µm All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023

DWG: 3002

Notes

Revision: 17-Apr-2023

Document Number: 63166

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