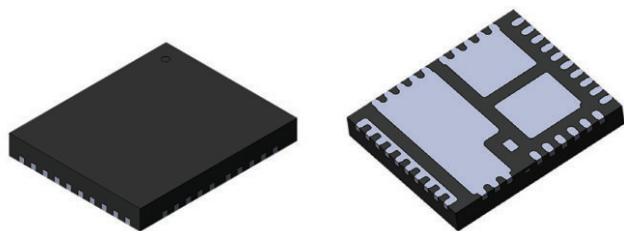


70 A VRPower®, Smart Power Stage With Current Sensing and Temperature Monitor

(Datasheet in Brief)



DESCRIPTION

The SiC832 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's 5 mm x 6 mm MLP package, SiC832 enables voltage regulator design to deliver in excess of 70 A per phase current.

The internal power MOSFETs utilize Vishay's state-of-the-art TrenchFET® Gen IV technology that delivers industry bench mark performance to significantly reduce switching and conduction losses.

The SiC832 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, and integrated bootstrap switch, a thermal monitor that alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers with the support of both 3.3 V and 5 V PWM logic with tri-state. Diode emulation mode can be enabled at light loads through the use of GLCTRL signal. The device also integrates a current monitor to provide a real time scale down of inductor current (I_{MON}). A temperature monitor provides the system an indication of the power stage internal temperature (T_{MON}) and can be used to throttle the system operation down to a safer level if needed. The device also integrates fault alerts such as HS FET over-current, over temperature and HS MOSFET short failures.

FEATURES

- Thermally enhanced PowerPAK® MLP56-39L package
- Optimize MOSFET switching performance with integrated Schottky diode in LS MOSFET
- Up to 70 A output current capability
- High frequency operation up to 2 MHz
- Power MOSFETs optimized for 12 V input stage and 10 % to 15 % duty cycle operation
- 3.3 V / 5 V PWM logic with tri-state and hold-off
- PWM minimum controllable on time of 30 ns
- Diode emulation mode at light loads for high efficiency over the full load range using GLCTRL pin
- Low PWM propagation delay (< 20 ns)
- Current sense monitor (I_{MON})
- Temperature monitor (T_{MON})
- Over temperature alert
- HS MOSFET over-current and short alert
- Under voltage lockout for V_{DRV} and V_{CC}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU, and memory
- DC/DC VR modules

EFFICIENCY

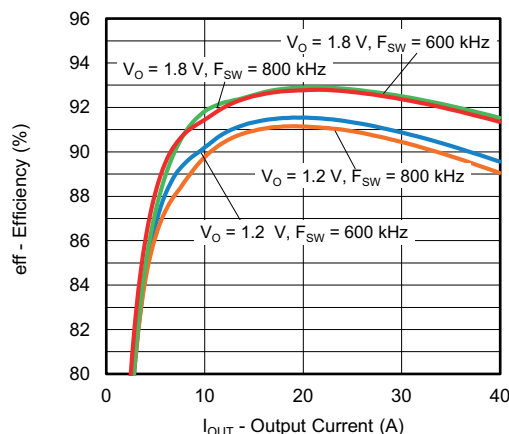


Fig. 1 - Efficiency vs. Output Current
 $(V_{IN} = 12\text{ V}, L = 100\text{ nH}, V_{CC} = V_{DRV} = 5\text{ V})$



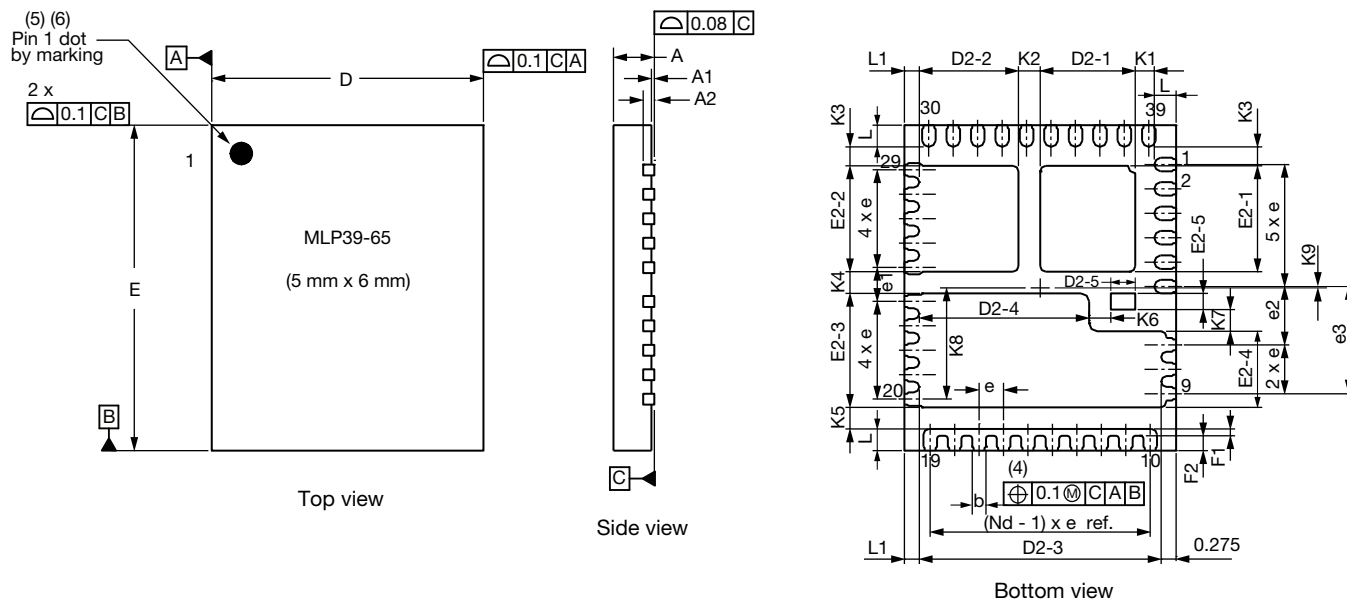
| PRODUCT SUMMARY | | |
|------------------------------------|---|---|
| Part number | SiC832 | SiC832A |
| Description | 70 A smart power stage, 4.5 V _{IN} to 21 V _{IN} , 5 V P _{WM} with diode emulation | 70 A smart power stage, 4.5 V _{IN} to 21 V _{IN} , 3.3 V P _{WM} with diode emulation |
| Input voltage min. (V) | 4.5 | 4.5 |
| Input voltage max. (V) | 21 | 21 |
| Continuous current rating max. (A) | 70 | 70 |
| Switch frequency max. (kHz) | 2000 | 2000 |
| Enable (yes / no) | No | No |
| Monitoring features | T _{MON} , I _{MON} | T _{MON} , I _{MON} |
| Protection | UVLO, OTP, OC flag | UVLO, OTP, OC flag |
| Light load mode | SMOD | SMOD |
| Pulse-width modulation (V) | 5 | 3.3 |
| Package type | PowerPAK MLP39-65 | PowerPAK MLP39-65 |
| Package size (W, L, H) (mm) | 5.0 x 6.0 x 0.75 | 5.0 x 6.0 x 0.75 |
| Status code | 1 | 1 |
| Product type | VRPower (DrMOS) | VRPower (DrMOS) |
| Applications | Computer, industrial, networking | Computer, industrial, networking |

To request the full version of the datasheet, please contact: ICmarketing@vishay.com

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PowerPAK® MLP39-65 Case Outline



| DIM. | MILLIMETERS | | | INCHES | | |
|------------------|-------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A ⁽⁸⁾ | 0.65 | 0.75 | 0.85 | 0.026 | 0.030 | 0.033 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A2 | 0.20 ref. | | | 0.008 ref. | | |
| b ⁽⁴⁾ | 0.20 | 0.25 | 0.30 | 0.078 | 0.098 | 0.011 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| e | 0.450 BSC | | | 0.018 BSC | | |
| e1 | 0.625 BSC | | | 0.025 BSC | | |
| e2 | 1.075 BSC | | | 0.042 BSC | | |
| e3 | 1.975 BSC | | | 0.078 BSC | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| D2-1 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| D2-2 | 1.73 | 1.83 | 1.93 | 0.068 | 0.072 | 0.076 |
| D2-3 | 4.35 | 4.45 | 4.55 | 0.171 | 0.175 | 0.179 |
| D2-4 | 3.03 | 3.13 | 3.23 | 0.119 | 0.123 | 0.127 |
| D2-5 | 0.35 | 0.45 | 0.55 | 0.014 | 0.018 | 0.022 |
| E2-1 | 1.85 | 1.95 | 2.05 | 0.073 | 0.077 | 0.081 |
| E2-2 | 1.85 | 1.95 | 2.05 | 0.073 | 0.077 | 0.081 |
| E2-3 | 2.00 | 2.10 | 2.20 | 0.079 | 0.083 | 0.087 |
| E2-4 | 1.30 | 1.40 | 1.50 | 0.051 | 0.055 | 0.059 |
| E2-5 | 0.20 | 0.30 | 0.40 | 0.008 | 0.012 | 0.016 |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| L1 | 0.18 | 0.28 | 0.38 | 0.007 | 0.011 | 0.015 |
| F1 | 0.125 BSC | | | 0.005 BSC | | |
| F2 | 0.275 BSC | | | 0.011 BSC | | |



| DIM. | MILLIMETERS | | | INCHES | | |
|--|-------------|------------|------|--------|------------|------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| K1 | | 0.35 ref. | | | 0.014 ref. | |
| K2 | | 0.40 ref. | | | 0.016 ref. | |
| K3 | | 0.35 ref. | | | 0.014 ref. | |
| K4 | | 0.40 ref. | | | 0.016 ref. | |
| K5 | | 0.40 ref. | | | 0.016 ref. | |
| K6 | | 0.40 ref. | | | 0.016 ref. | |
| K7 | | 0.40 ref. | | | 0.016 ref. | |
| K8 | | 2.048 ref. | | | 0.081 ref. | |
| K9 | | 0.025 ref. | | | 0.001 ref. | |
| N ⁽³⁾ | | 39 | | | 39 | |
| Nd ⁽³⁾ | | 10 | | | 10 | |
| Ne ⁽³⁾ | | 10 | | | 10 | |
| ECN: T19-0296-Rev. D, 23-Sep-2019 DWG: 6074 | | | | | | |

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994
- (3) N is the number of terminals
Nd is the number of terminals in X-direction and
Ne is the number of terminals in Y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- (5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (6) Exact shape and size of this feature is optional
- (7) Package warpage max. 0.08 mm
- (8) Applied only for terminals



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