Power MOSFET Basics
Understanding Superjunction Technology

by Sanjay Havanur and Philip Zuk

Power MOSFETs based on superjunction technology have become the industry norm in high-voltage switching converters. They offer lower $R_{DS(on)}$ simultaneously with reduced gate and output charges, which allows for more efficient switching at any given frequency. Prior to the availability of superjunction MOSFETs the dominant design platform for high-voltage devices was based on planar technology. However, fast switching at high voltages poses its own challenges in AC/DC power supplies and inverters. Designers making the transition from planar to superjunction MOSFETs often have to accommodate EMI, voltage spikes, and noise-related concerns by compromising switching speed. This application note will compare the characteristics of the two platforms so that the benefits of superjunction technology are fully understood and utilized.

In order to understand the differences between the two technologies, we need to start with the basics. Fig. 1a shows the simple structure of a conventional planar high-voltage MOSFET. Planar MOSFETs typically have a high drain-to-source resistance per unit of silicon area, and come with relatively higher drain source resistances. Lower $R_{DS(on)}$ values could be achieved with high cell density and large die sizes. However, large cell densities and die sizes also come with high gate and output charges, which increase the switching losses as well as costs. There is also a limit to how low the total silicon resistance can go. The total $R_{DS(on)}$ for the device can be expressed as the sum of three components: the channel, epi, and the substrate.

$$R_{DS(on)} = R_{ch} + R_{epi} + R_{sub}$$

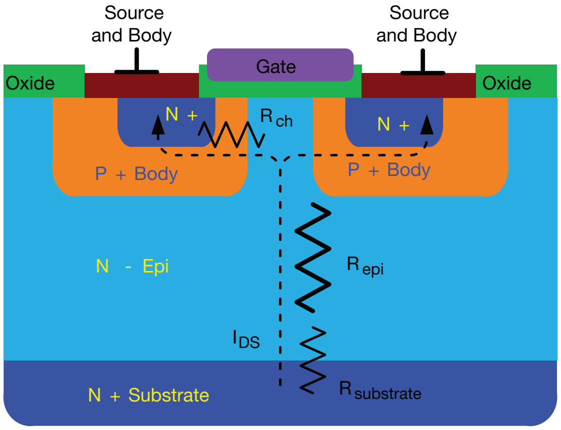
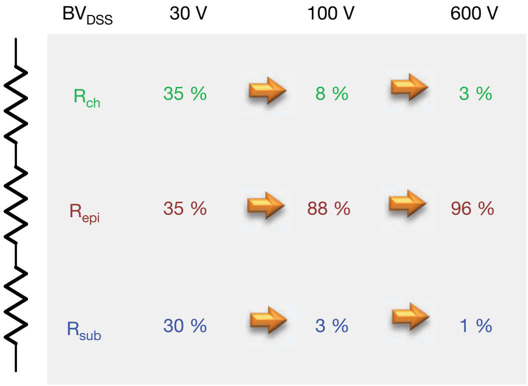


Fig. 1a - Conventional Planar MOSFET Structure



BV_{DSS}	30 V		100 V		600 V
R_{ch}	35 %	⇨	8 %	⇨	3 %
R_{epi}	35 %	⇨	88 %	⇨	96 %
R_{sub}	30 %	⇨	3 %	⇨	1 %

Fig. 1b - Resistive Components of a Planar MOSFET

Fig. 1b shows a breakdown of different components that make up the $R_{DS(on)}$ in a planar MOSFET. For low-voltage MOSFETs the three components are comparable. However, as the voltage rating is increased, the epitaxial layer needs to be thicker and more lightly doped to block high voltages. For every doubling of the voltage rating, the area required to maintain the same $R_{DS(on)}$ increases more than five-fold. For 600 V rated MOSFETs, more than 95 % of the resistance comes from the epitaxial layer. It is obvious that for any significant reduction in the $R_{DS(on)}$ value, it is necessary to find a way of heavily doping the drift region and drastically reducing the epi resistance.

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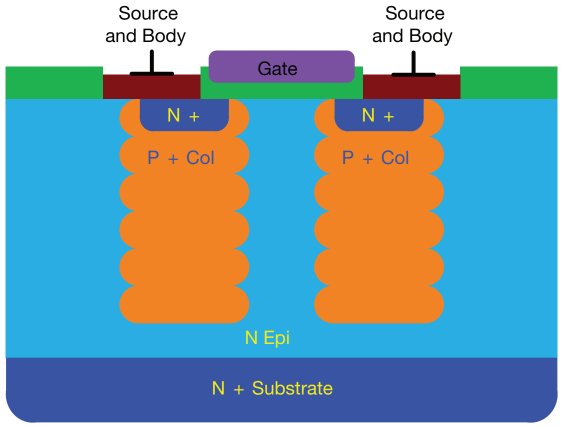

Fig. 2 - Superjunction MOSFET Structure

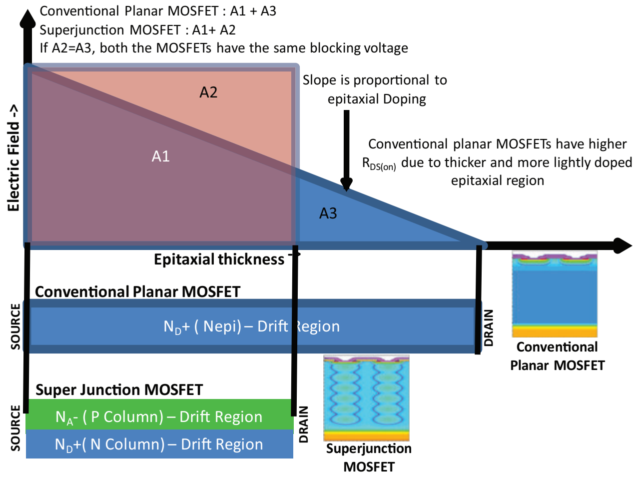

Fig. 3 - Blocking Voltage and On-resistance Comparison for Planar and Superjunction MOSFETs

Figure 2 shows the physical structure of superjunction MOSFETs based on the idea of charge balancing. The drift region now has multiple P columns, which cancel the charge in the surrounding N regions under reverse bias. As a result, the N_{epi} can now be thinner and heavily doped since the combined structure offers a much higher resistance to applied reverse voltage. As the N region becomes more heavily doped, its on-resistance per unit area decreases.

Figure 3 compares the electric field in the drift region vs. epi thickness for the two technologies. In conventional planar MOSFETs, the blocking voltage is defined both by the epi thickness and the doping (N_D+), or slope of the line. If additional blocking voltage is required, not only does the epi have to be made thicker, but the epi doping line also has to change. This results in a disproportionate increase in $R_{DS(on)}$ for higher-voltage MOSFETs. For every doubling of voltage rating, keeping the same die size, the $R_{DS(on)}$ can increase anywhere from three- to five-fold.

Superjunction MOSFETs can use a thinner epi (A1 + A2) for a given blocking voltage than conventional planar devices (A1 + A3). The doping of the N region (N_D+) is balanced out by the doping of the P column (N_A-), resulting in no slope. In other words, because of the charge balancing mechanism, only the thickness of the epi defines the blocking voltage. As a result, the superjunction structure has a linear relationship between on-resistance and breakdown voltage. The on-resistance increases linearly with an increase in breakdown voltage. For the same breakdown voltage and die size, the on-resistance of a superjunction MOSFET will be much less than a conventional planar device.

Superjunction devices from Vishay are available under the E series of high-voltage MOSFETs in ratings from 500 V to 650 V. They are offered in a variety of packages, from small SMT footprints like the PowerPAK® SO8 and PowerPAK 8 x 8 to the standard TO-xxx packages. Typical specific on-resistance varies from 20 mΩ -cm^2, down to 10 mΩ-cm^2, depending on the breakdown voltage and technology generation. The on-resistance x area product of conventional planar MOSFETs can be three to five times higher, again depending on the voltage rating. For example, while the lowest $R_{DS(on)}$ achievable for a 600 V device in the TO-220 package is 275 mΩ, superjunction devices from Vishay are available down to 50 mΩ in the same package. Of course with every new generation of design platforms, better devices with lower $R_{DS(on)}$ will be available in the future.

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CAPACITANCES

The reduction in resistance for superjunction devices has obvious benefits, such as lower conduction losses or smaller dies for the same $R_{DS(on)}$. Additionally, the reduction in the chip area can lead to lower capacitances and gate and output charges, which reduces dynamic losses. In low-voltage trench or planar MOSFETs, there is usually a trade-off between lowering the $R_{DS(on)}$ at the cost of higher capacitances. In the case of superjunction technology the compromise is minimal. The charge balancing mechanism achieves simultaneous reduction in $R_{DS(on)}$ and device capacitances, making it a win-win solution. Table 1 compares the characteristics of two devices with close $R_{DS(on)}$ values. The superjunction device has 15 % to 25 % improvement for every parameter, except for E_{as} and I_{as}. This is because the superjunction device, despite a 20 % reduction in $R_{DS(on)}$, has a die size that is only one third of the comparable planar. The smaller size affects current and power ratings. A large die size has lower current density and better heat sinking capabilities. As a result, for a given on-resistance, the conventional planar MOSFETs are inherently more rugged compared to superjunction devices. However, at currents and switching frequencies typically used in high-voltage power converters, the superjunction device will always offer lower loss and better efficiency.

TABLE 1: COMPARISON OF 600 V PLANAR VS. SUPERJUNCTION DEVICES

DEVICE	TECHNOLOGY	$R_{DS(on)}$	Q_{gs}	Q_{gd}	Q_g	Q_{rr}	E_{oss}	E_{as} / I_{as}
		mΩ	nC				µJ	mJ/A
		TYPICAL						
SiHP17N60D	Planar	275	14	22	45	7000	8.9	165 / 4.2
SiHP15N60E	Superjunction	230	11	17	38	5400	6.1	102 / 12

Table 2 shows another comparison, this time for 500 V devices. The SiHG32N50D is a planar MOSFET with a 125 mΩ typical $R_{DS(on)}$ rating. The die is large, in fact the largest die that can fit into a TO-247 package. This can be compared with the superjunction SiHA25N50E in the smaller, isolated thin lead TO-220F package, which offers the same $R_{DS(on)}$ but better specifications on every parameter except UIS ruggedness. It should be noted that Vishay is quite conservative in derating the inductive switching specifications. A 100 % derating factor is applied on the measured failure current, which translates to a derating factor of four for UIS energy E_{as}.

TABLE 2: COMPARISON OF 500 V PLANAR VS. SUPERJUNCTION DEVICES

DEVICE	TECHNOLOGY	PACKAGE	$R_{DS(on)}$	Q_{gs}	Q_{gd}	Q_g	Q_{rr}	E_{oss}	E_{as} / I_{as}
			mΩ	nC				µJ	mJ/A
			TYPICAL						
SiHG32N50D	Planar	TO-247	125	18	29	64	7	23.8	225 / 14
SiHA25N50E	Superjunction	TO-220F	125	14	25	57	5.3	13.1	53 / 6.8

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Fig. 4 defines the capacitances for which the charge specifications are provided. For the two 600 V devices compared above, the capacitance curves are shown in Fig. 5. Note that the capacitance scale is logarithmic.

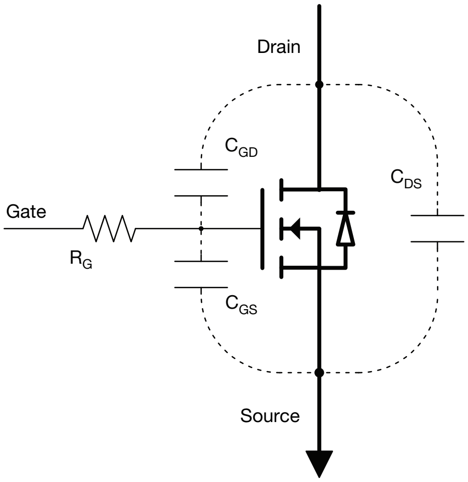

Fig. 4 - MOSFET Capacitance Definitions

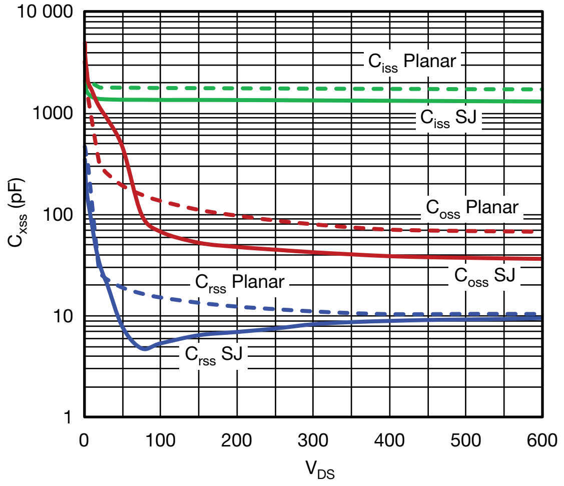

Fig. 5 - Capacitance Comparison for Planar SiHP17N60D and Superjunction SiHP15N60E MOSFETs

Gate Charge Considerations

In any switching circuit the gate drive design is a trade-off between switching speed and noise. Superjunction devices offer high switching speeds at high voltages, which also demand extra attention to drive design. Poor design may cause voltage spikes, erratic switching, and higher EMI. Another major concern with ultra-low capacitances is an increased sensitivity to coupling and noise, which shows up as gate source oscillation. Designers are then forced to slow down the switching speed by introducing high gate resistances or low drive currents, which ultimately reduce the system efficiency.

Vishay application note AN-608, "Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance," gives the detailed theory behind the switching behavior of conventional MOSFETs (www.vishay.com/docs/73217/73217.pdf).
Particular reference is made to the gate charge curve as shown in Fig. 4 and Fig. 5 of the application note, which depict the rise and fall of V_{DS} as the gate is discharged and charged. Typically the Q_{gd} of a MOSFET can be used for estimating the V_{DS} voltage rise and fall times during switching. Assuming a constant current source driving the gate,

$t_{vfall} = Q_{gd} / I_{gon}$ and $t_{vrise} = Q_{gd} / I_{goff}$.

This simple model cannot be used for superjunction devices, whose structure and switching behaviors are more complex. As an example, Fig. 6 shows the gate charge curve for the SiHP33N60E with a V_{DS} curve superposed on it. One feature of superjunction MOSFETs when compared to planar devices is the wide variations in their capacitances as a function of V_{DS}. In a superjunction MOSFET, because of the 100:1 drop in C_{rss} from 0 V to 600 V, the observed switching durations will appear to be much smaller than those estimated from the datasheet values of Q_{gd}. While there is no analytical method to predict the actual transition times, which in turn depend on application conditions, designers should be aware that good switching performance can be achieved with lower gate drive currents. This translates into smaller and lower-cost gate drivers compared to those used for planar MOSFETs.

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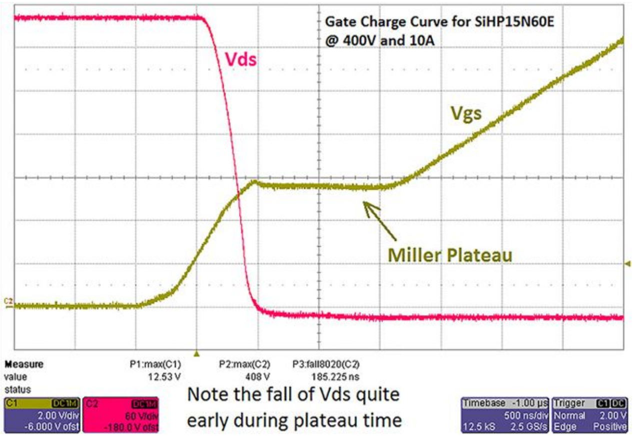

Note the fall of Vds quite early during plateau time

Fig. 6 - Gate Charge Curve vs. V_{DS} for SiHP15N60E

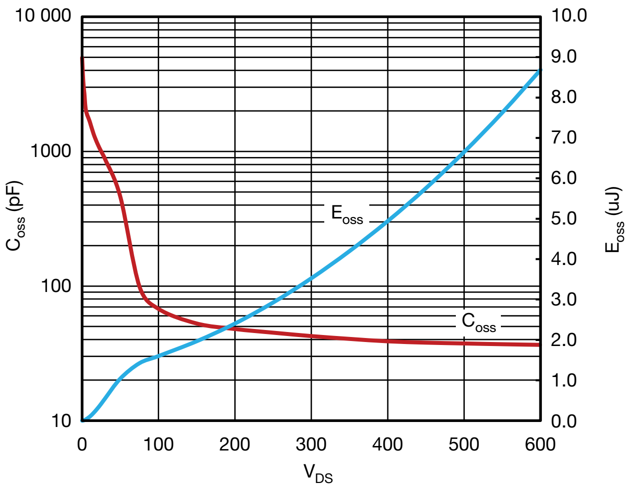

Fig. 7 - Capacitance and Stored Energy vs. V_{DS} for SiHP15N60E

C_{oss}, $C_{o(tr)}$, $C_{o(er)}$, and E_{oss}

Fig. 5 also shows that C_{oss} for the superjunction device is nearly 40 % lower, leading to reduced stored energy and faster switching, while at the same time achieving lower loss. The output capacitance C_{oss} of all MOSFETs shows non-linear characteristics with respect to applied voltage V_{DS}. The non-linearity is even more pronounced in the case of superjunction MOSFETs, with a variation of 100:1 in value from 0 V to 600 V. This poses a challenge to designers who need effective values for stored charge and energy in the C_{oss}. The superjunction datasheets typically provide two effective values for C_{oss}, defined as follows:

$C_{o(tr)}$ - defines the value of a fixed capacitor, which has the same stored charge as the variable C_{oss} at 80 % of the rated voltage.

$C_{o(er)}$ - defines the value of a fixed capacitor, which has the same stored energy as the variable C_{oss} at 80 % of the rated voltage.

Several studies have emphasized the impact of stored energy E_{oss} on system efficiency under different operating conditions. Recognizing the importance, Vishay has started providing complete E_{oss} curves for all high-voltage MOSFETs, all the way up to rated voltage as shown in Fig. 7.

Body Diode Characteristics

Because of their combination of lower $R_{DS(on)}$ and low capacitances, superjunction MOSFETs are also the devices of choice for all high-frequency switching applications, including ZVS bridges. In a ZVS or synchronous application, the body diode of the MOSFET is not subject to hard commutation. The diode current is softly commutated to the MOSFET channel and the diode recovers voltage blocking capability when the MOSFET is turned off. However, this does not mean that diode recovery can be taken for granted in ZVS bridges under all operating conditions, including transients. Lower Q_{rr}, short carrier lifetime, and soft recovery characteristics are still important requirements. Superjunction MOSFETs do have the advantage of lower Q_{rr} and t_{rr} over planar devices and therefore are better suited in ZVS applications. However, where the ability of the body diode to recover blocking voltage is considered critical, further improvements in the recovery characteristics are desirable. Recognizing the need, Vishay has introduced the EF series of superjunction MOSFETs in which, using additional processes during manufacturing, the Q_{rr} of the body diode is reduced by a factor of 5 to 7.

Conclusions

The superjunction structure is a major development in high-voltage MOSFET technology and offers significant benefits. $R_{DS(on)}$, gate capacitances, and output charge are all simultaneously reduced, along with die size. To make the best use of these fast and efficient devices, designers have to pay greater attention to their system design, particularly towards reducing PCB parasitics. Superjunction MOSFETs have much lower gate charges and can be driven with low-current gate drivers. Their output capacitances, while highly non-linear, offer lower stored energy E_{oss} and related output losses. Vishay superjunction devices are available in different packages, voltage ratings, and body diode characteristics to suit a wide variety of applications.