Vishay Siliconix

## **E-Series Power MOSFET**

### **DESCRIPTION**

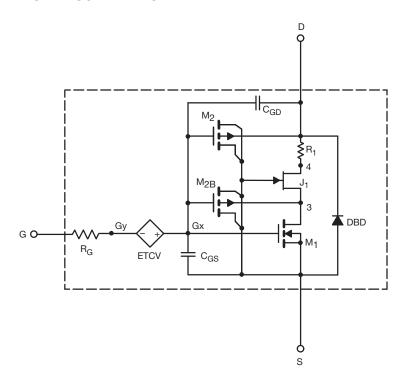
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer
to the appropriate datasheet of the same number for guaranteed specification limits.



# **SPICE Device Model SiHD14N60E**

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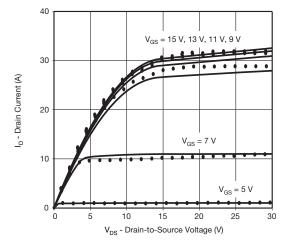
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	3.1	-	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A	0.290	0.255	Ω
Forward Transconductance	g <sub>fs</sub>	$V_{DS} = 30 \text{ V}, I_D = 7 \text{ A}$	6	3.8	S
Dynamic					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	1370	1160	pF
Output Capacitance	Coss		108	64	
Reverse Transfer Capacitance	C <sub>rss</sub>		14	6	
Total Gate Charge	Qg	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A	33	33	nC
Gate-Source Charge	$Q_{gs}$		8	8	
Gate-Drain Charge	$Q_{gd}$		14	14	
Drain-Source Body Diode Characteristi	cs				
Diode Forward Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C}, \ I_S = 7  \text{A}, \ V_{GS} = 0  \text{V}$	0.9	-	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 ^{\circ}\text{C}, I_F = I_S = 7 \text{A},$ $dI/dt = 100 \text{A/\mu s}, V_R = 25 \text{V}$	260	274	ns
Reverse Recovery Charge	Q <sub>rr</sub>		3.3	3.3	μC

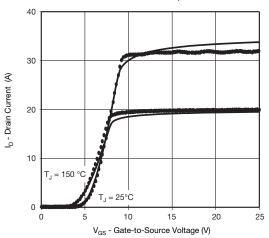


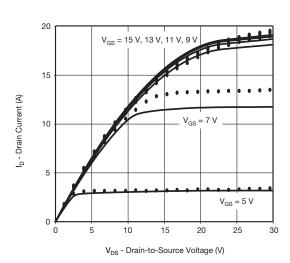
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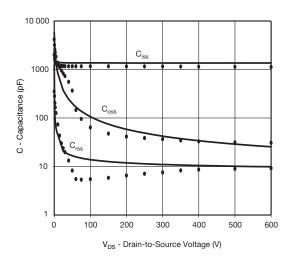
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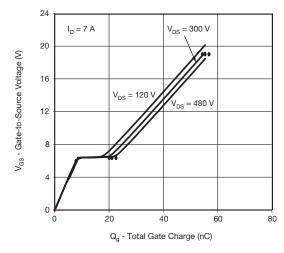
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25 \, ^{\circ}\text{C}$ , unless otherwise noted)

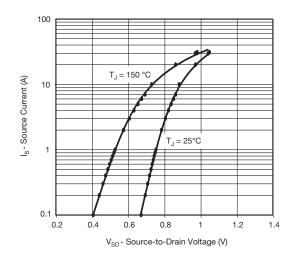












#### Note

Dots and squares represent measured data.
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