

## Dual P-Channel 20 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
- 20	0.059 at $V_{GS} = - 4.5$ V	- 6 <sup>a</sup>	6.9 nC
	0.096 at $V_{GS} = - 2.5$ V	- 6 <sup>a</sup>	

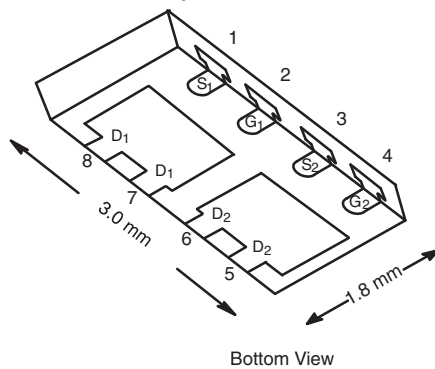
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- Typical ESD Performance 1500 V in HBM
- Compliant to RoHS Directive 2002/95/EC

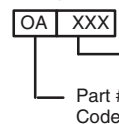


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PowerPAK ChipFET Dual

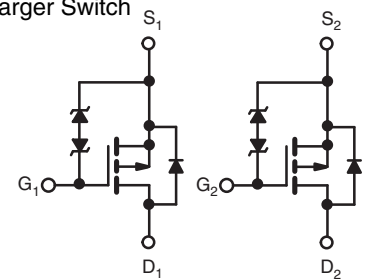


Marking Code



### APPLICATIONS

- Load Switch and Charger Switch for Portable Devices
- DC/DC Converters



Ordering Information: Si5999EDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current ( $t = 300 \mu\text{s}$ )	$I_{DM}$	- 20	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	- 1.9 <sup>b, c</sup>
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	43	55	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	9.5	12	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is  $105^\circ\text{C/W}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 20			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 16		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			3		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 0.6		- 1.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			± 10	μA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 4.5 V			± 1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 3.5 A		0.047	0.059	Ω
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1.5 A		0.077	0.096	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 3.5 A		11		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		496		pF
Output Capacitance	C <sub>oss</sub>			141		
Reverse Transfer Capacitance	C <sub>rss</sub>			121		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 5 A		13.2	20	nC
		V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5 A		6.9	10.5	
			Q <sub>gs</sub>		1.6	
Gate-Source Charge	Q <sub>gs</sub>			1.8		
Gate-Drain Charge	Q <sub>gd</sub>					
Gate Resistance	R <sub>g</sub>	f = 1 MHz	2	8	16	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 2.5 Ω I <sub>D</sub> ≅ - 4 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		17	26	ns
Rise Time	t <sub>r</sub>			21	32	
Turn-Off Delay Time	t <sub>d(off)</sub>			26	40	
Fall Time	t <sub>f</sub>			13	20	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 2.5 Ω I <sub>D</sub> ≅ - 4 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		6	12	
Rise Time	t <sub>r</sub>			11	22	
Turn-Off Delay Time	t <sub>d(off)</sub>			23	35	
Fall Time	t <sub>f</sub>			11	22	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 6	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 20	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 4 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 4 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		24	48	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>			14		ns
Reverse Recovery Rise Time	t <sub>b</sub>			10		

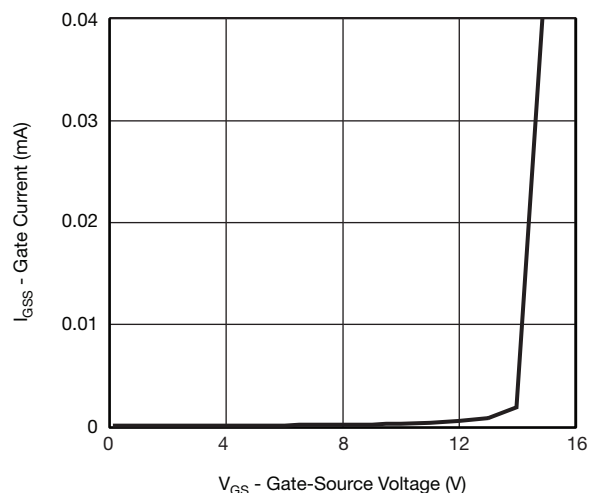
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

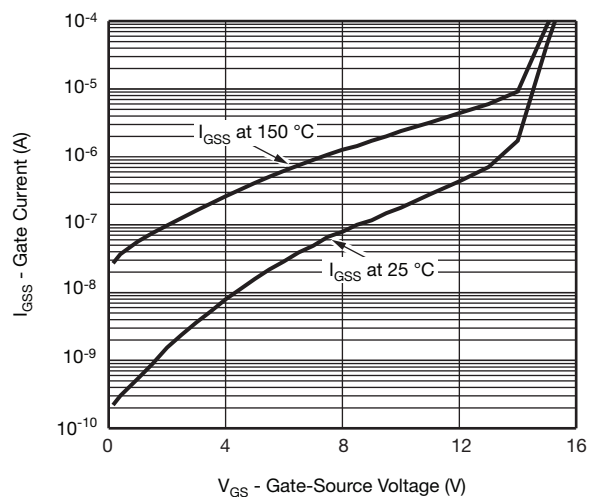
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

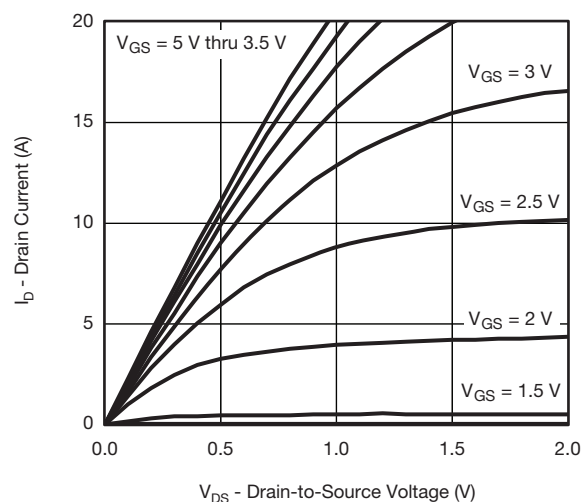
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



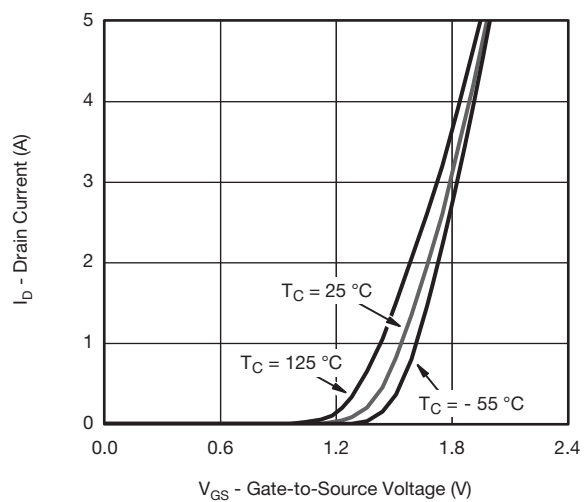
**Gate Current vs. Gate-Source Voltage**



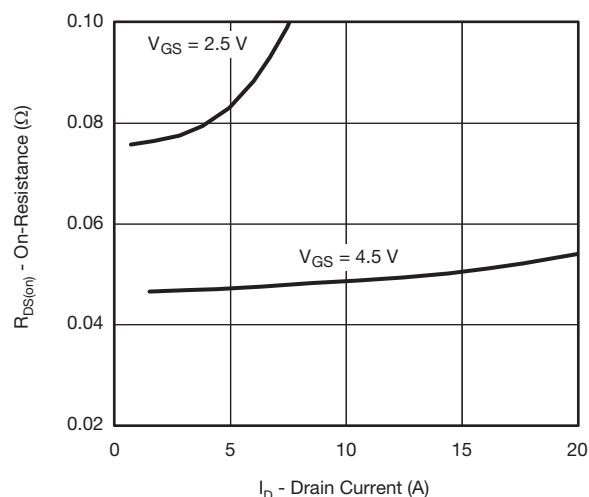
**Gate Current vs. Gate-Source Voltage**



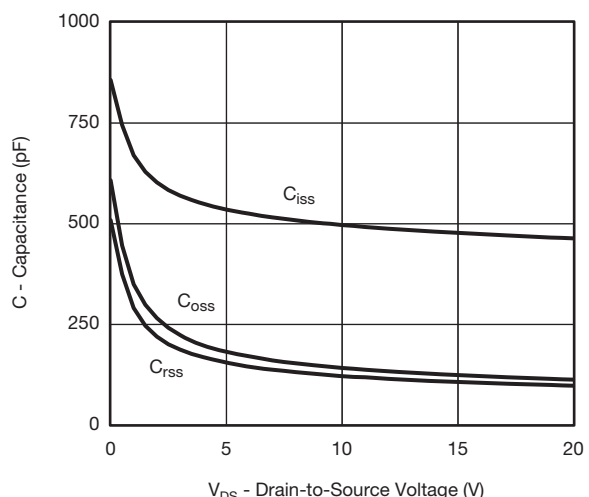
**Output Characteristics**



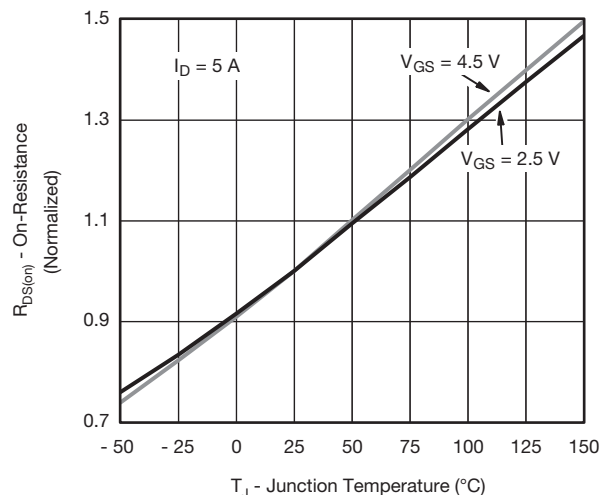
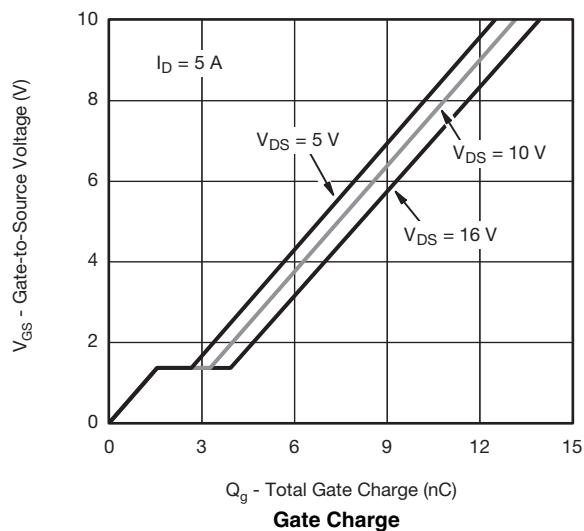
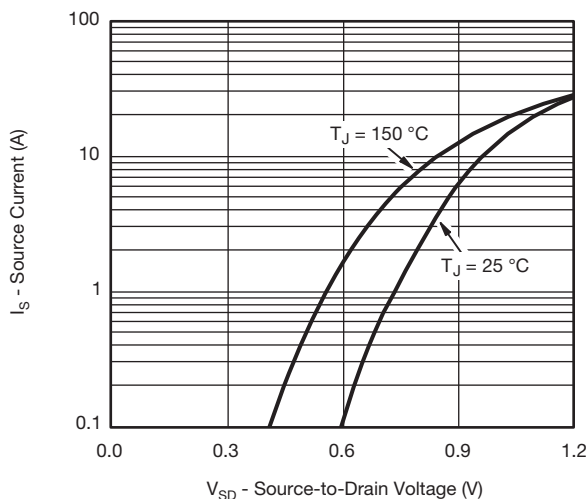
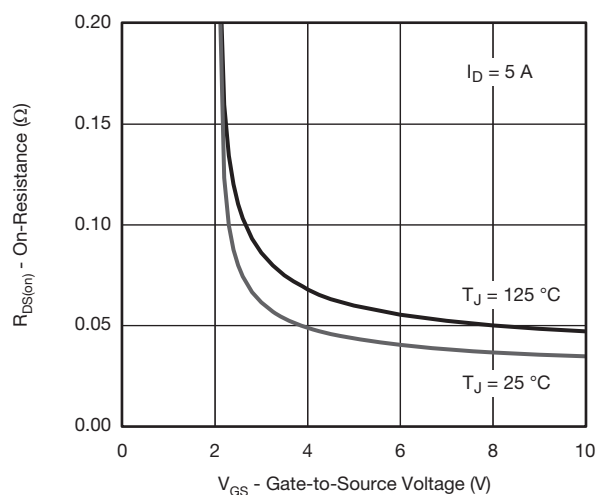
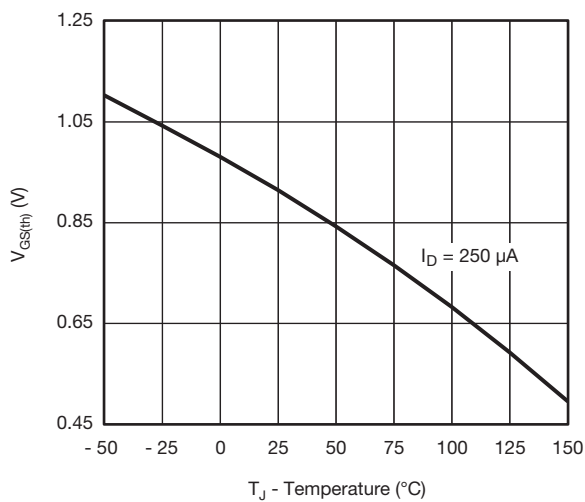
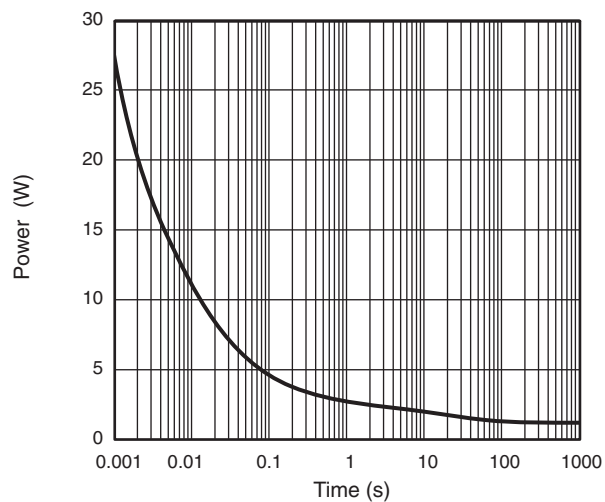
**Transfer Characteristics**



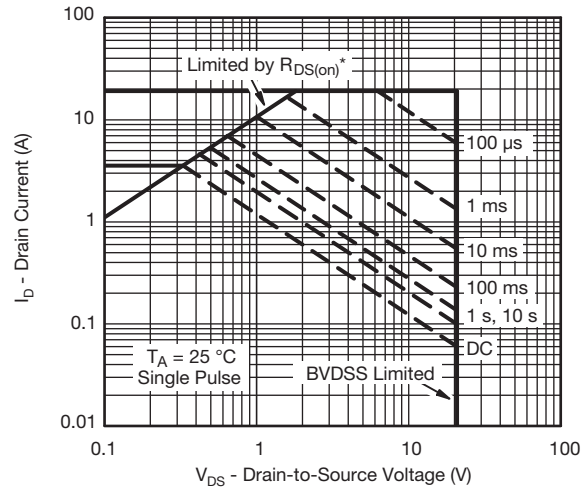
**On-Resistance vs. Drain Current**



**Capacitance**

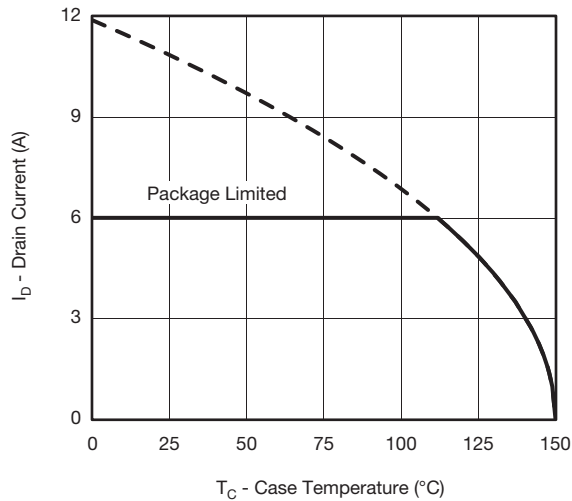
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

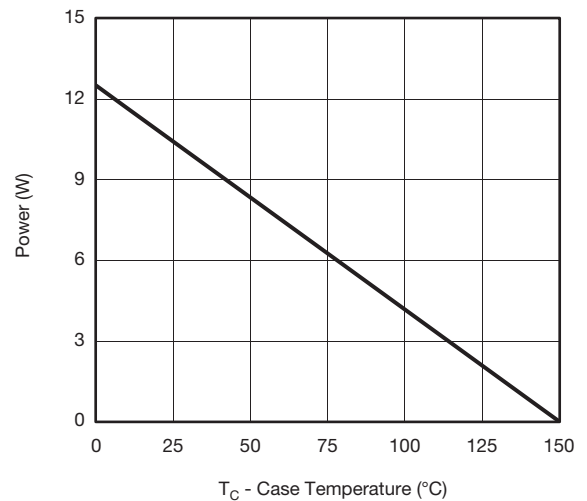


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

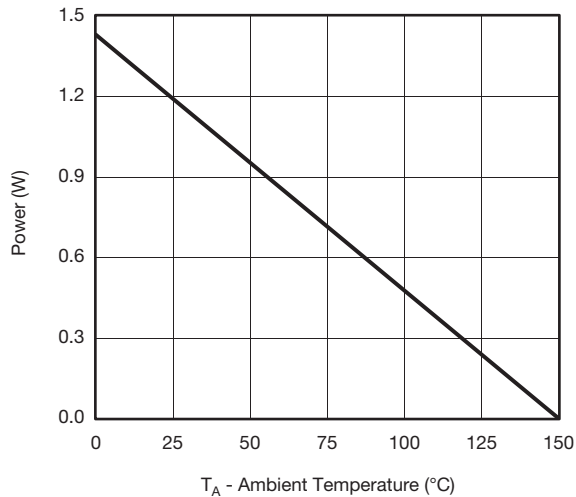
**Safe Operating Area, Junction-to-Ambient**



**Current Derating\***

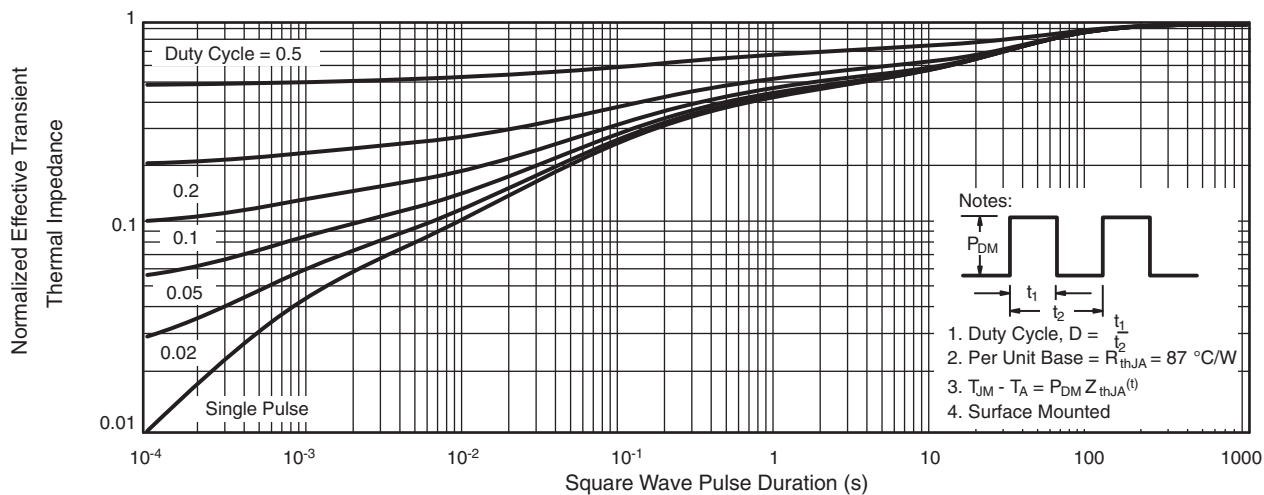
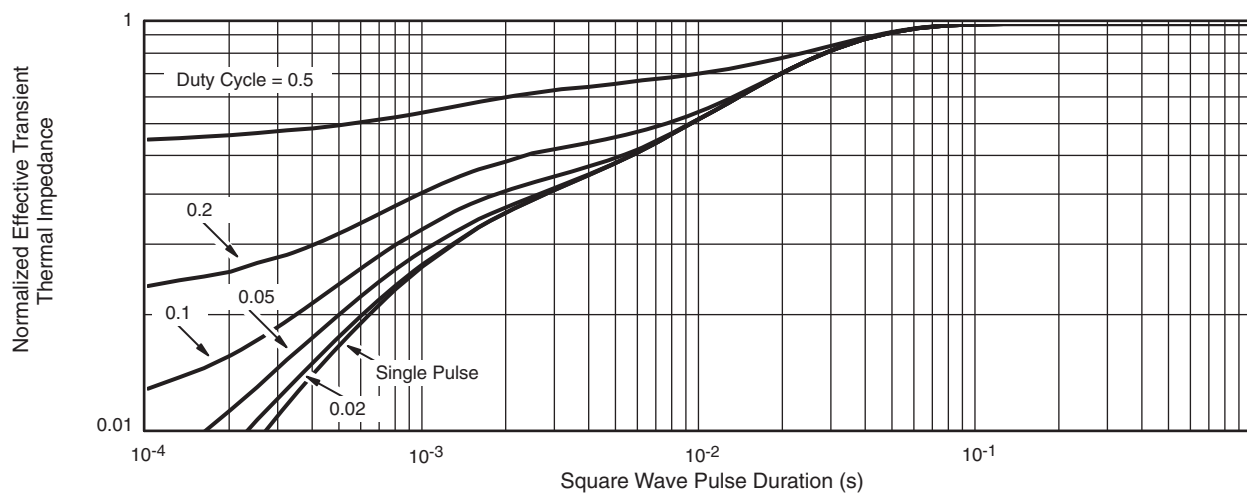


**Power Derating, Junction-to-Case**



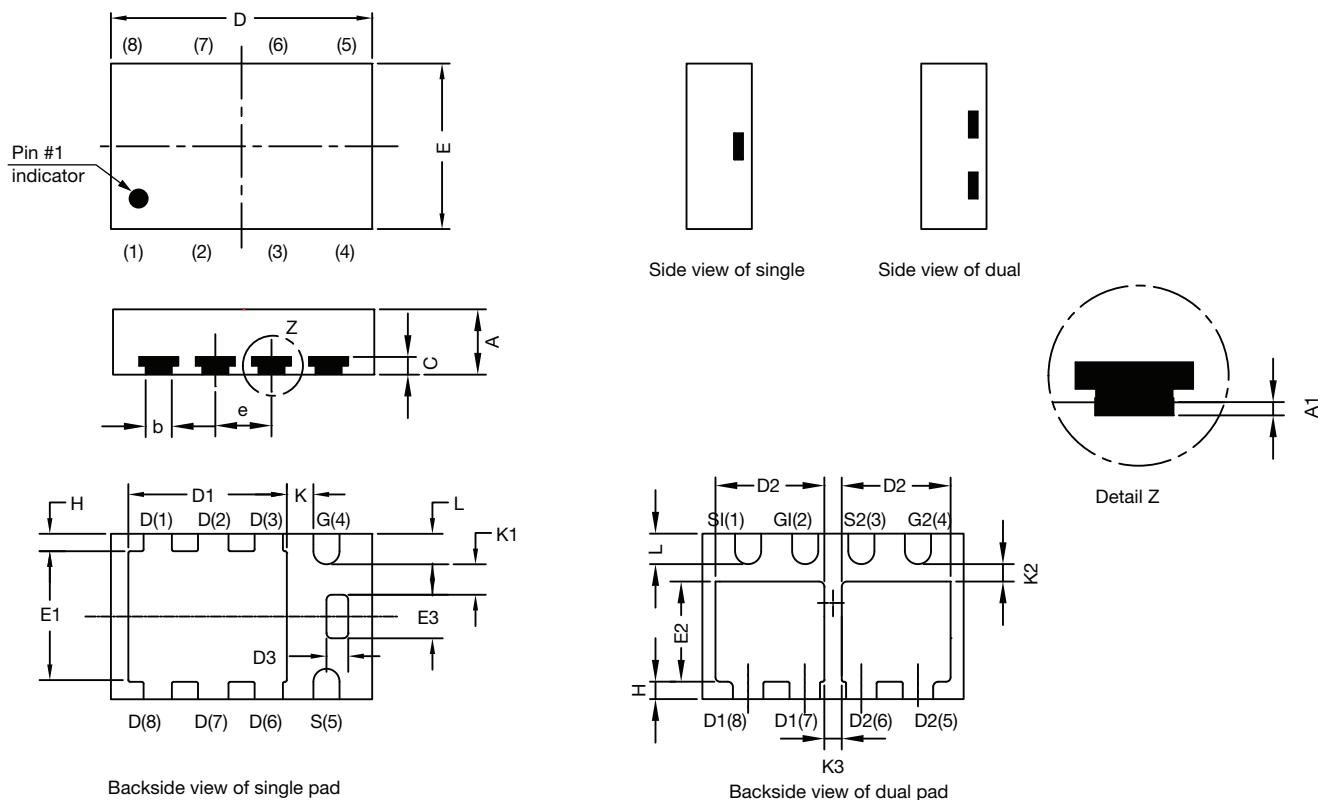
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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## PowerPAK® ChipFET® Case Outline

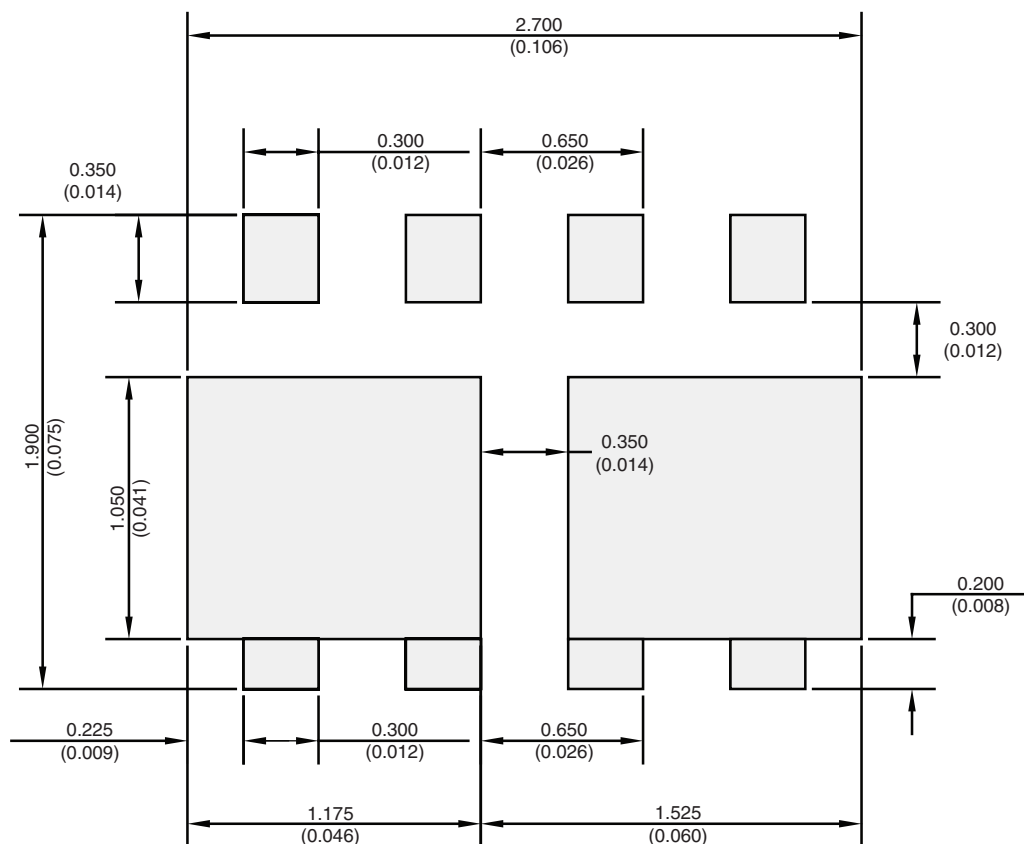


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14						
DWG: 5940						

### Note

- Millimeters will govern

## RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads  
Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image  
Pin #1 Location is Top Left Corner





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