Dual P-Channel 40 V (D-S) MOSFET

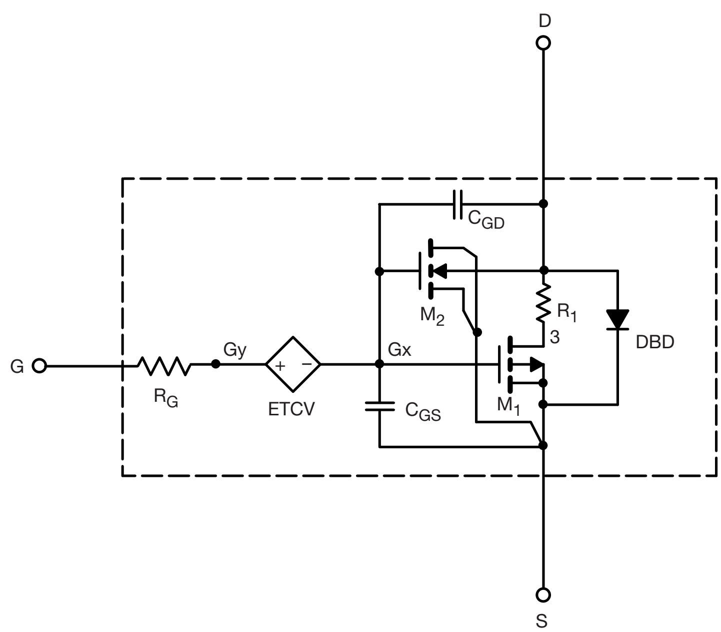
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



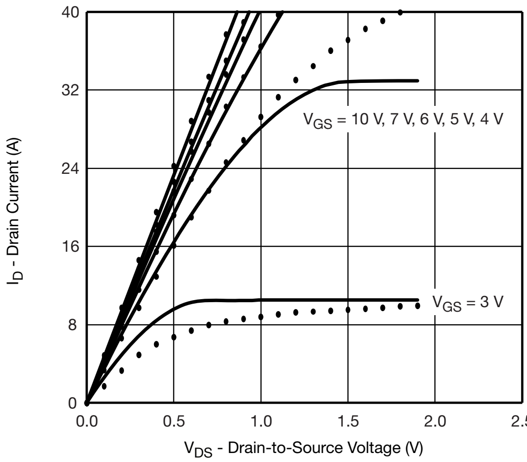
Note
This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

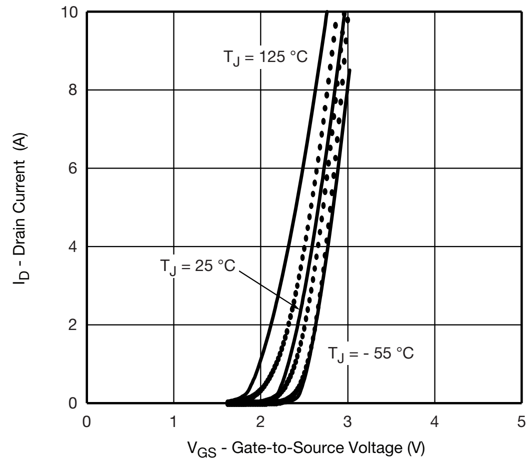
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	1.5	-	V
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 8 A	0.021	0.021	Ω
		V_{GS} = - 4.5 V, I_D = - 5 A	0.026	0.027	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 8 A	18	22	S
Diode Forward Voltage	V_{SD}	I_S = - 2 A	- 0.74	- 0.75	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz	2020	2000	pF
Output Capacitance	C_{oss}		246	240	
Reverse Transfer Capacitance	C_{rss}		201	202	
Total Gate Charge	Q_g	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 10 A	41	41.5	nC
		V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_D = - 10 A	22	21.7	
Gate-Source Charge	Q_{gs}		5.6	5.6	
Gate-Drain Charge	Q_{gd}		9.8	9.8	

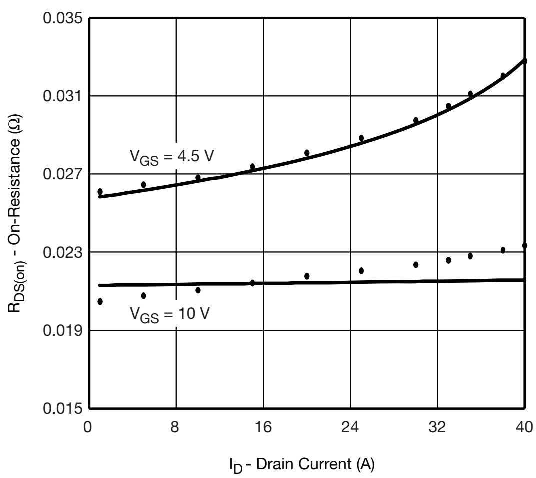
Notes

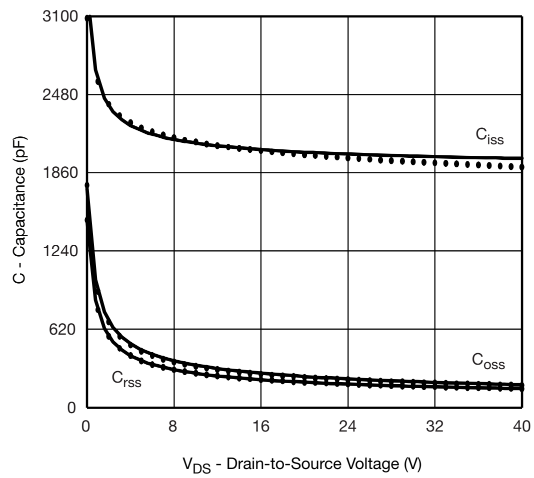
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

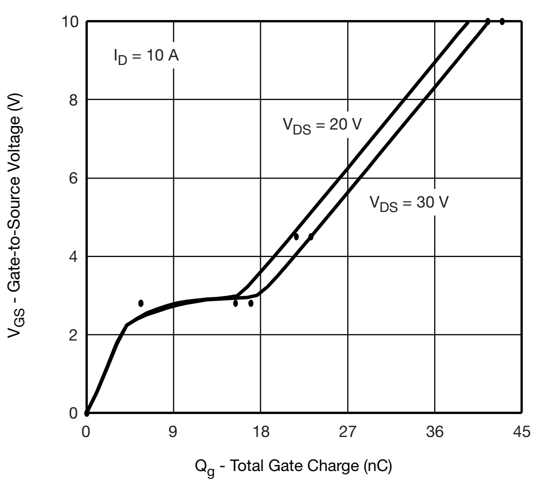
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

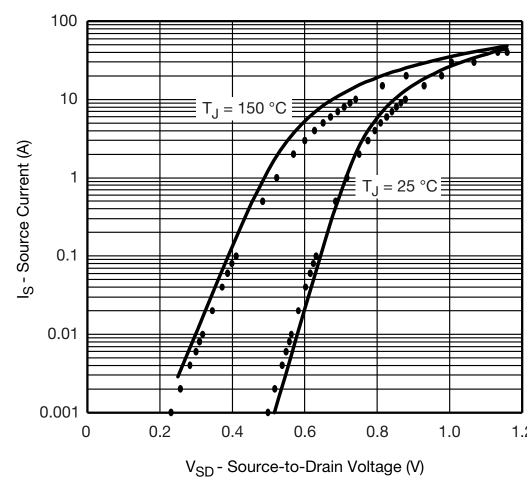












Note

Dots and squares represent measured data.

Disclaimer

All product specifications and data are subject to change without notice.

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