

## P-Channel 60 V (D-S) 175 °C MOSFET

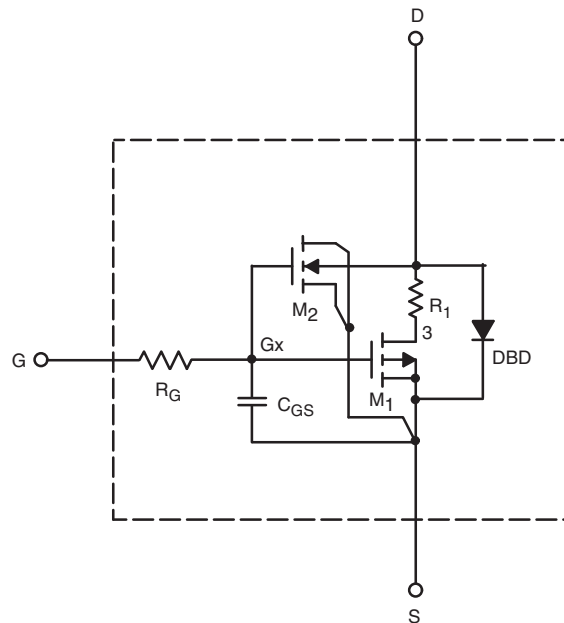
### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



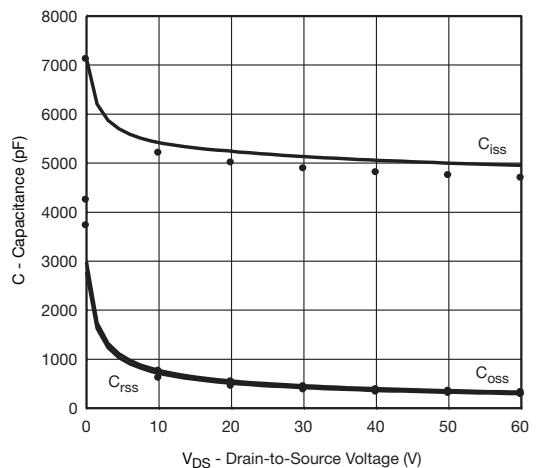
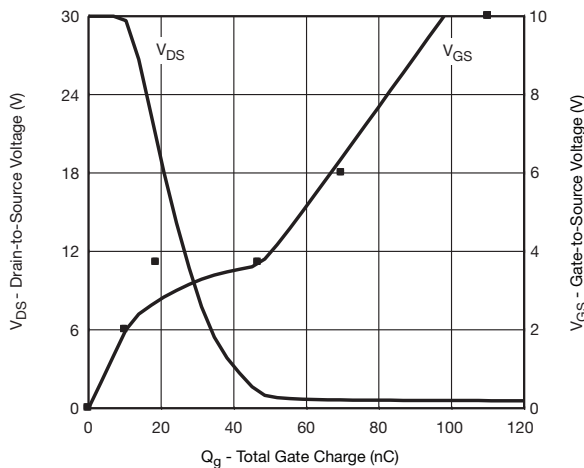
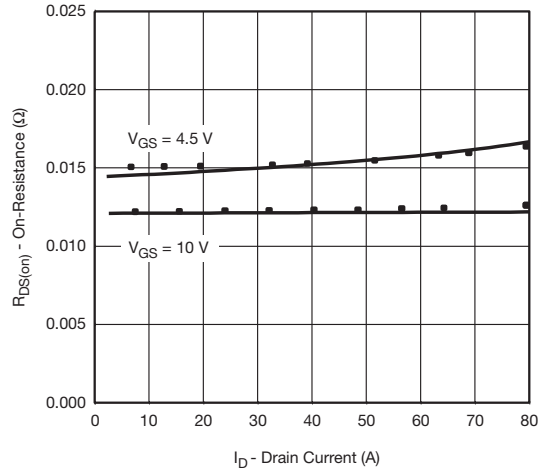
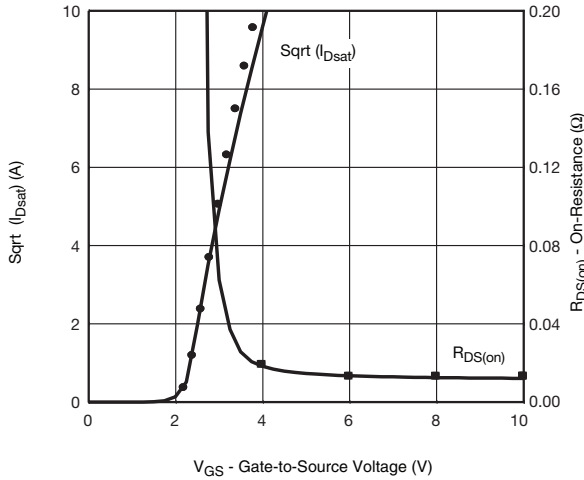
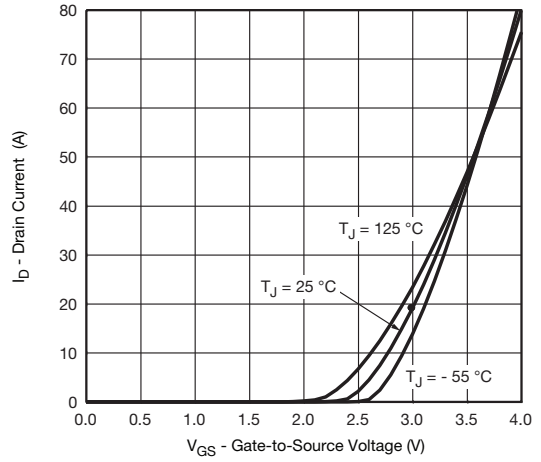
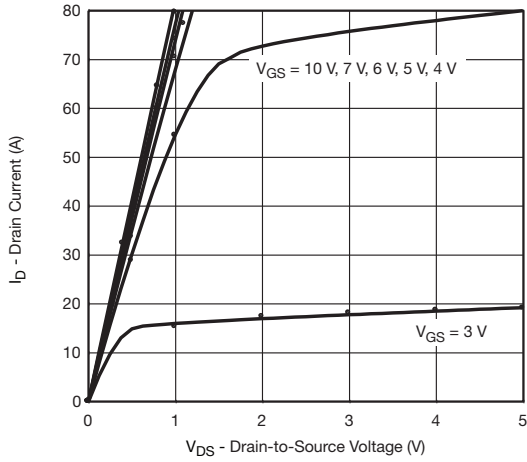
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	1.7	-	V
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -17\text{ A}$	0.012	0.012	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -17\text{ A}, T_J = 125\text{ }^\circ\text{C}$	0.019	-	
		$V_{GS} = -10\text{ V}, I_D = -17\text{ A}, T_J = 175\text{ }^\circ\text{C}$	0.023	-	
		$V_{GS} = -4.5\text{ V}, I_D = -14\text{ A}$	0.015	-	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -17\text{ A}$	49	61	S
Diode Forward Voltage	$V_{SD}$	$I_S = -50\text{ A}, V_{GS} = 0\text{ V}$	-0.91	-1	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	5180	4950	pF
Output Capacitance	$C_{oss}$		497	480	
Reverse Transfer Capacitance	$C_{rss}$		455	405	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -30\text{ V}, V_{GS} = -10\text{ V}, I_D = -50\text{ A}$	100	110	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		19	19	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		28	28	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -30\text{ V}, R_L = 0.60\text{ }\Omega,$ $I_D \cong -50\text{ A}, V_{GEN} = -10\text{ V}, R_g = 2.5\text{ }\Omega$	31	15	ns
Rise Time <sup>c</sup>	$t_r$		29	70	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$		200	175	
Fall Time <sup>c</sup>	$t_f$		57	175	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -50\text{ V}, dI/dt = 100\text{ A}/\mu\text{s}$	35	45	

**Notes**

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.



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