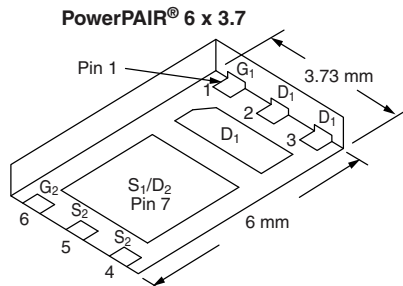


Dual N-Channel 30 V (D-S) MOSFETs with Schottky Diode

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1	30	0.0093 at V _{GS} = 10 V	16 ^a	7.7 nC
		0.0130 at V _{GS} = 4.5 V	16 ^a	
Channel-2	30	0.0047 at V _{GS} = 10 V	35 ^a	17 nC
		0.0059 at V _{GS} = 4.5 V	35 ^a	



Ordering Information: SiZ790DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

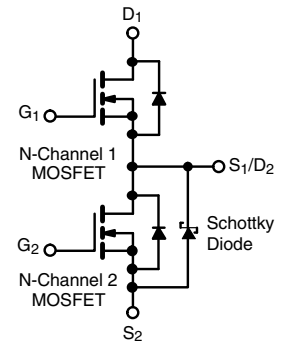
- Halogen-free According to IEC 61249-2-21 Definition
- SkyFET[®] Monolithic TrenchFET[®] Power MOSFETs and Schottky Diode
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- System Power
 - Notebook
 - Server
- POL
- Synchronous Buck Converter



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V _{DS}	30		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	16 ^a	35 ^a	A
		T _C = 70 °C	16 ^a	35 ^a	
		T _A = 25 °C	12.9 ^{b, c}	23.4 ^{b, c}	
		T _A = 70 °C	10.3 ^{b, c}	18.7 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	70	100		
Continuous Source Drain Diode Current	I _S	T _C = 25 °C	16 ^a	35 ^a	
		T _A = 25 °C	3.2 ^{b, c}	3.8 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	16	30		
Single Pulse Avalanche Energy	E _{AS}	13	45	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	27	48	W
		T _C = 70 °C	17	31	
		T _A = 25 °C	3.9 ^{b, c}	4.6 ^{b, c}	
		T _A = 70 °C	2.5 ^{b, c}	3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	24	32	20	27	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	3.5	4.6	2	2.6		

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 67 °C/W for channel-1 and 65 °C/W for channel-2.

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30			V
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	30			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1		2.2	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1.1		2.2	
Gate Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			± 100	nA
			Ch-2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2		50	200	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			5	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2		140	1400	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	15			A
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		0.0075	0.0093	Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0038	0.0047	
		$V_{GS} = 4.5\text{ V}, I_D = 13\text{ A}$	Ch-1		0.0105	0.0130	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0048	0.0059	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$	Ch-1		48		S
		$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	Ch-2		85		
Dynamic^a							
Input Capacitance	C_{iss}	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		830		pF
			Ch-2		1980		
Output Capacitance	C_{oss}	Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		185		
			Ch-2		455		
Reverse Transfer Capacitance	C_{rss}		Ch-1		80		
			Ch-2		165		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		15.6	24	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		36	54	
		Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-1		7.7	12	
			Ch-2		17	26	
Gate-Source Charge	Q_{gs}	Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		2.6		
			Ch-2		5.7		
Gate-Drain Charge	Q_{gd}		Ch-1		3		
			Ch-2		5		
Gate Resistance	R_g	$f = 1\text{ MHz}$	Ch-1	0.2	1	2	Ω
			Ch-2	0.2	0.9	1.8	

Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



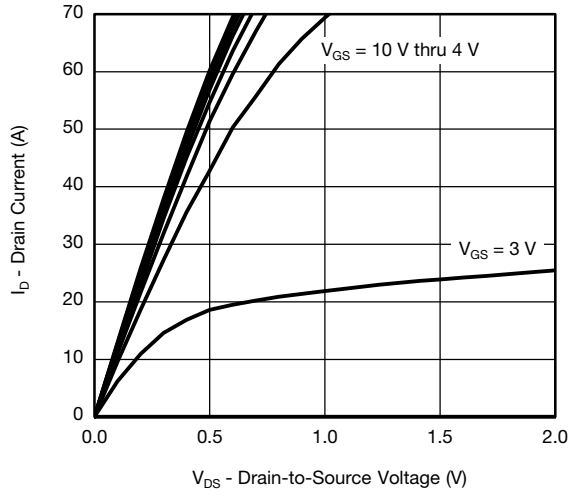
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic^a							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		10	20	ns
Rise Time	t_r		Ch-2		20	40	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		15	30	
			Ch-2		15	30	
Fall Time	t_f	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		15	30	
			Ch-2		7	15	
Turn-On Delay Time	$t_{d(on)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	Ch-1		10	20	
			Ch-2		25	50	
Rise Time	t_r	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	Ch-1		5	10	
			Ch-2		10	20	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	Ch-1		15	30	
			Ch-2		10	20	
Fall Time	t_f	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	Ch-1		17	35	
			Ch-2		25	50	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			16	A
			Ch-2			35	
Pulse Diode Forward Current ^a	I_{SM}		Ch-1			70	
			Ch-2			100	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
		$I_S = 2\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-2		0.38	0.48	
Body Diode Reverse Recovery Time	t_{rr}	Channel-1 $I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	30	ns
			Ch-2		20	40	
Body Diode Reverse Recovery Charge	Q_{rr}	Channel-2 $I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	Ch-1		6	12	nC
			Ch-2		15	32	
Reverse Recovery Fall Time	t_a		Ch-1		9		ns
			Ch-2		10.5		
Reverse Recovery Rise Time	t_b		Ch-1		6		
			Ch-2		9.5		

Notes:

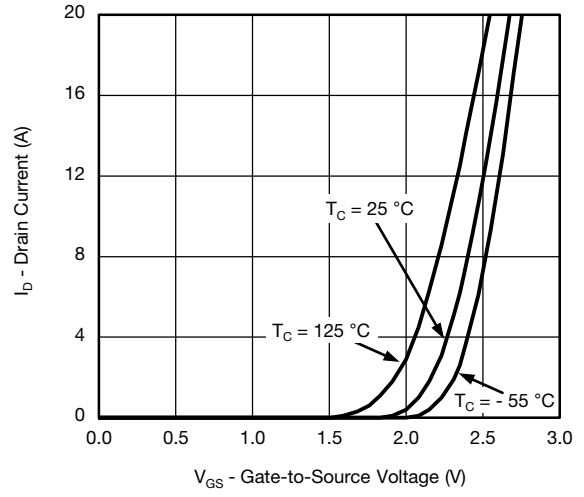
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

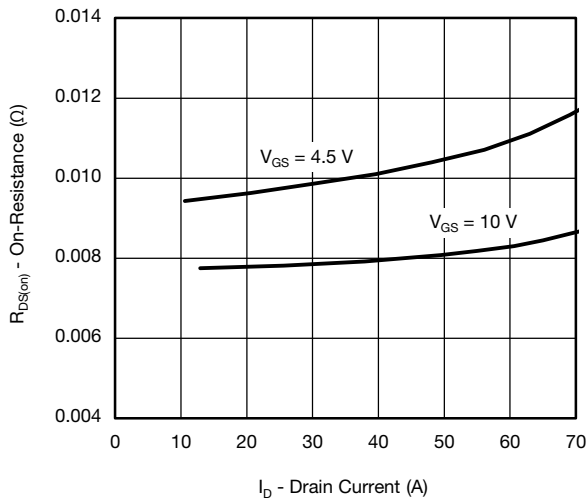
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



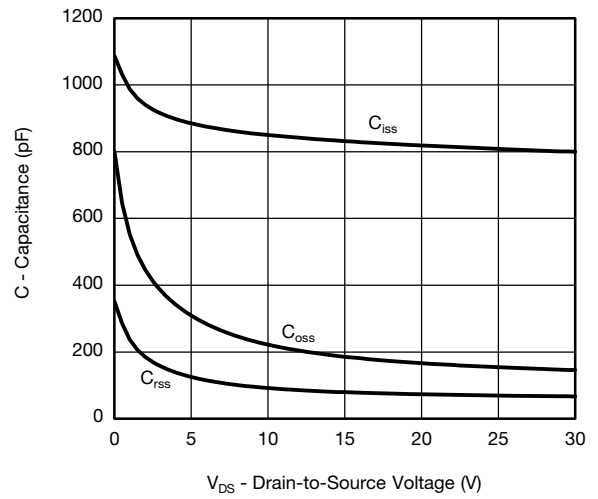
Output Characteristics



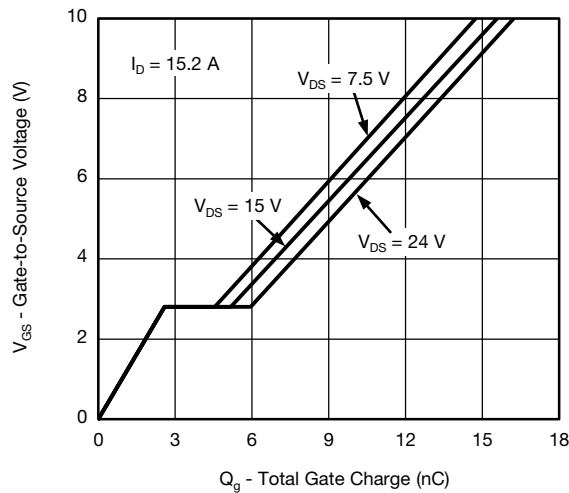
Transfer Characteristics



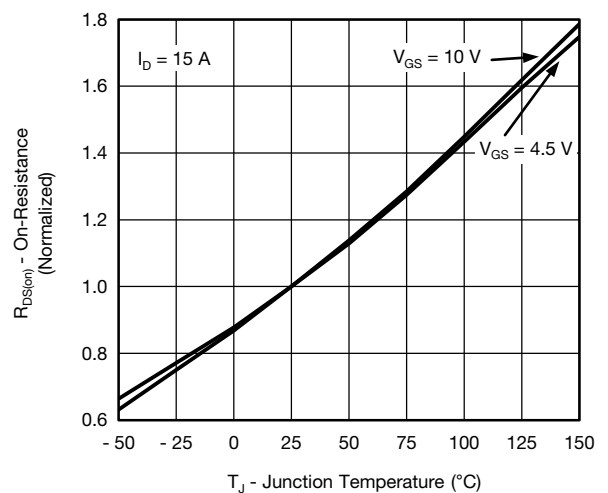
On-Resistance vs. Drain Current



Capacitance

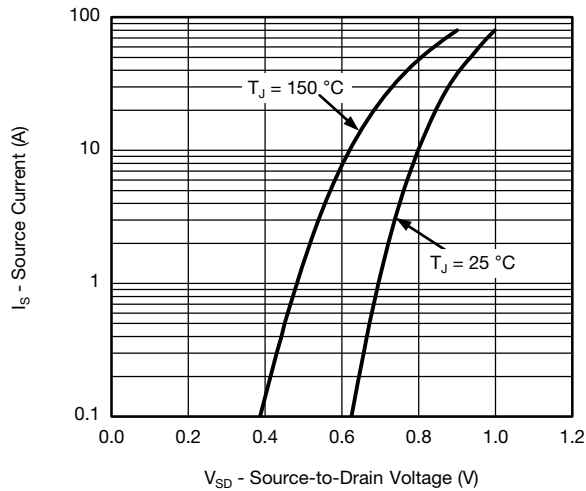


Gate Charge

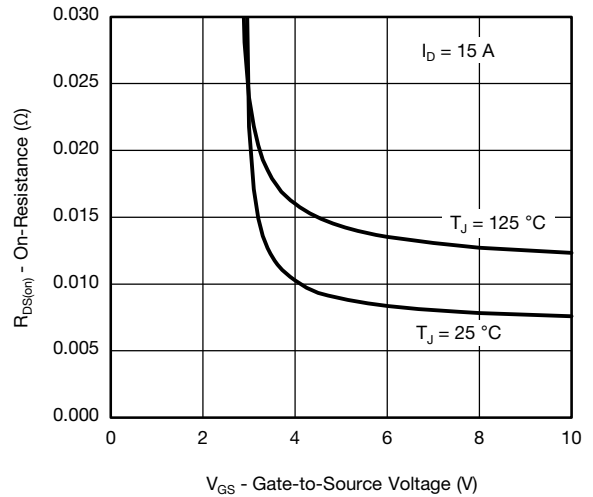


On-Resistance vs. Junction Temperature

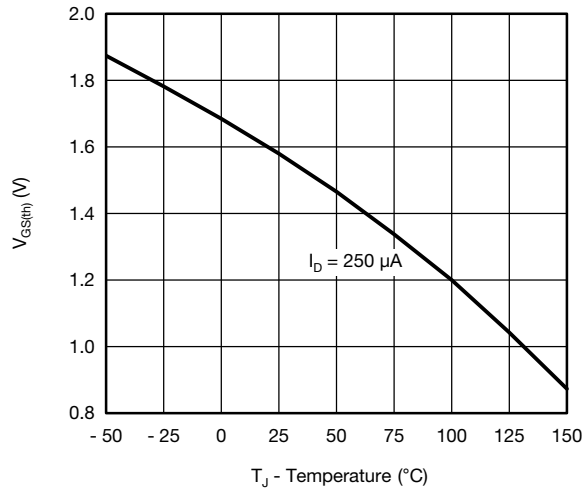
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



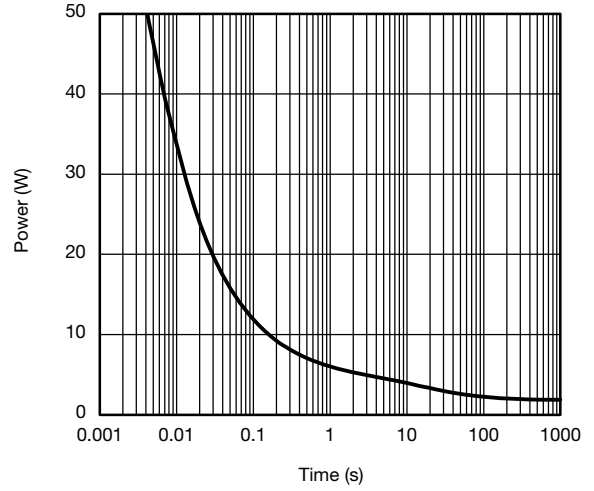
Source-Drain Diode Forward Voltage



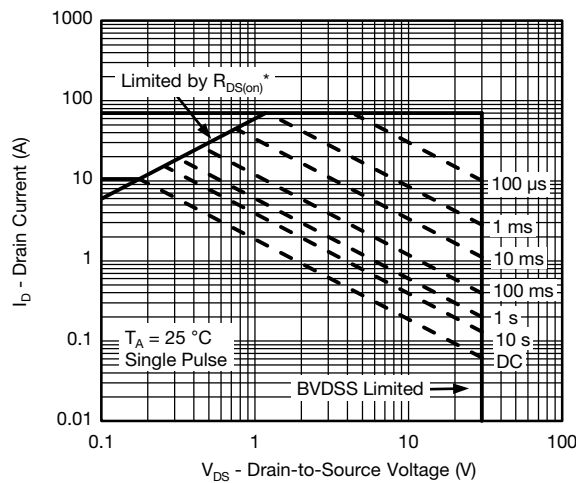
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

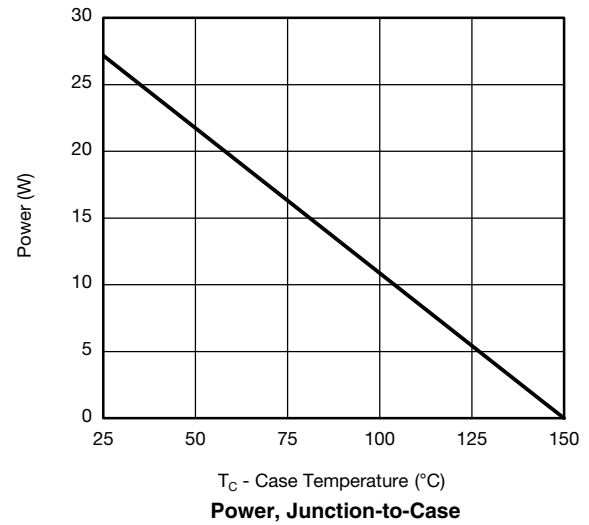
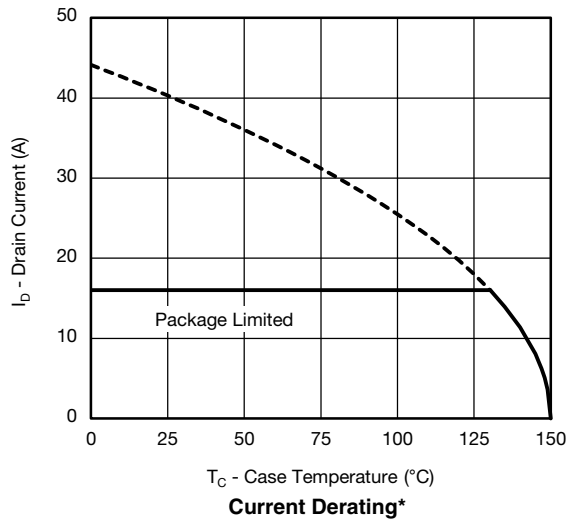


Single Pulse Power



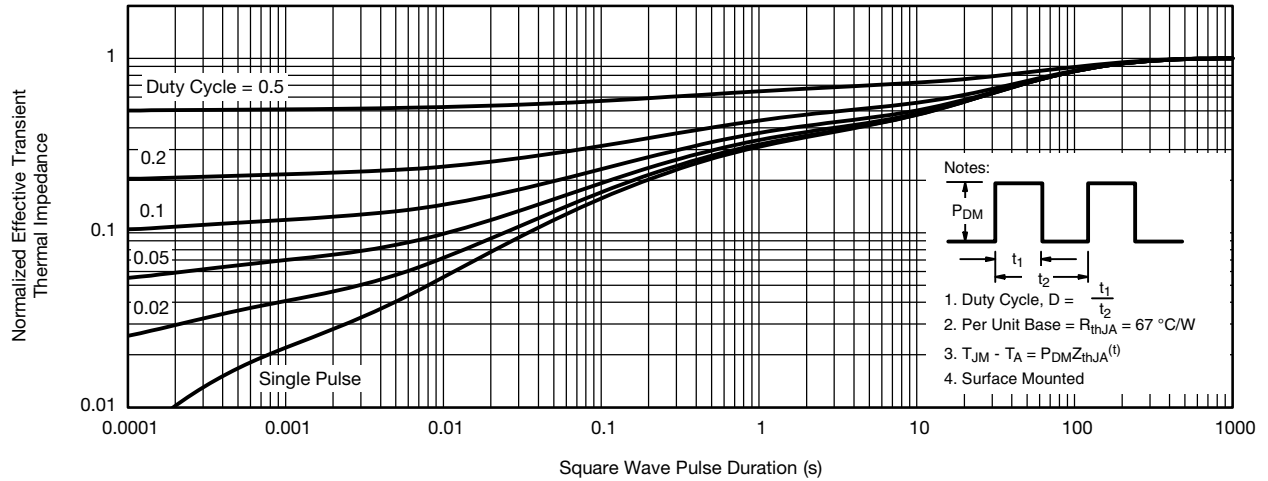
Safe Operating Area, Junction-to-Ambient

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

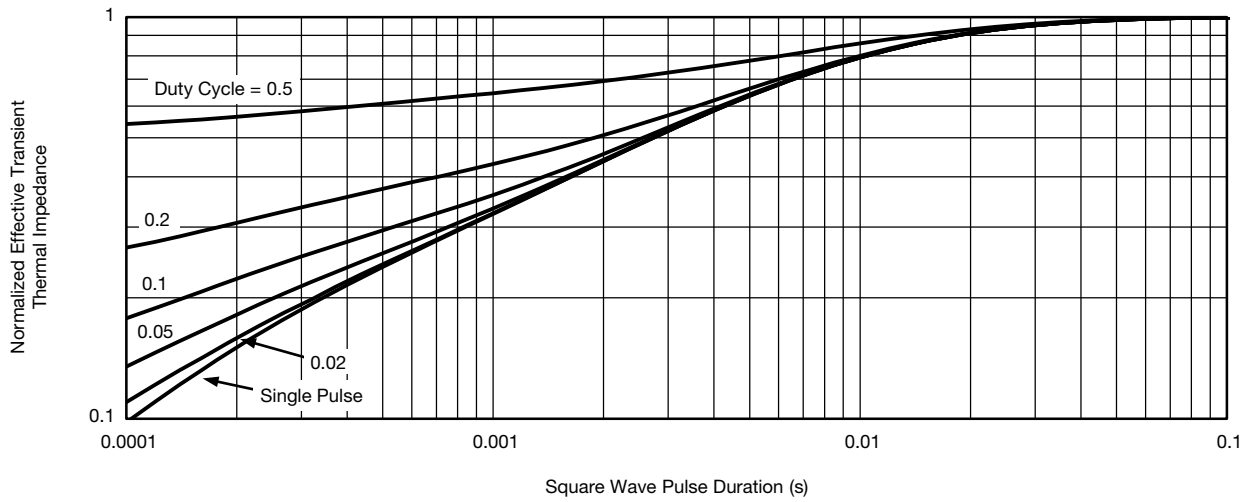


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

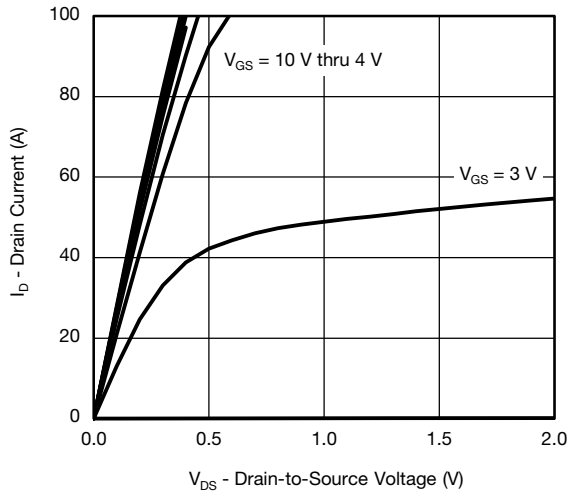


Normalized Thermal Transient Impedance, Junction-to-Ambient

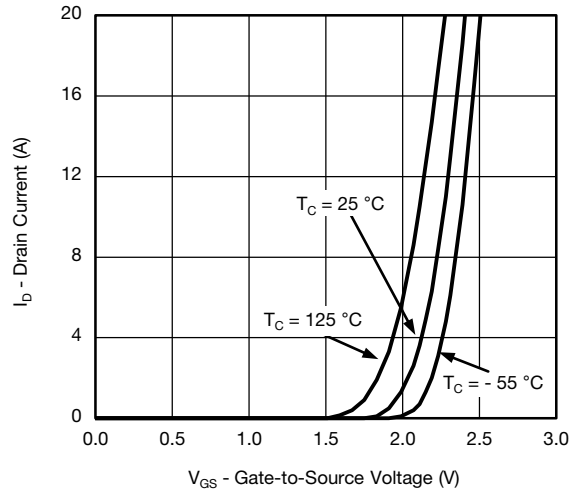


Normalized Thermal Transient Impedance, Junction-to-Case

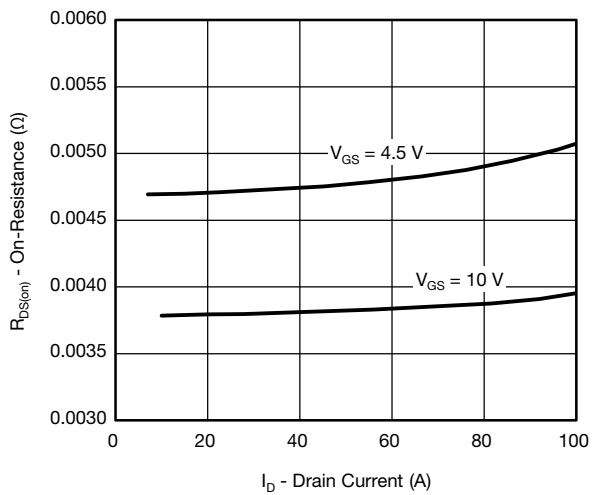
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



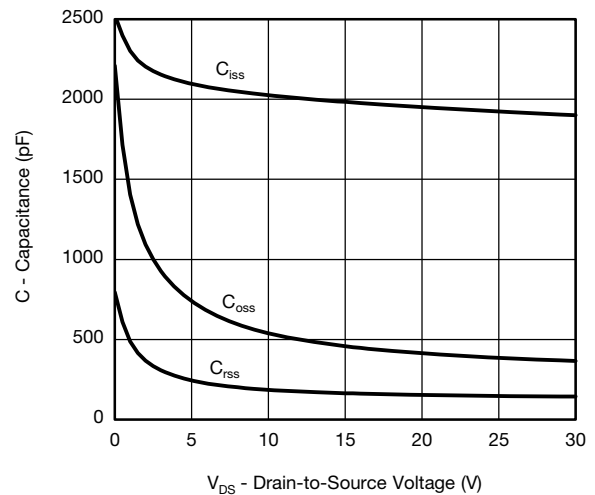
Output Characteristics



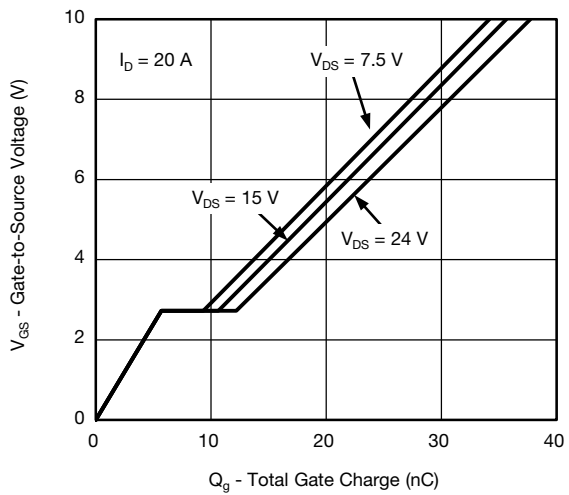
Transfer Characteristics



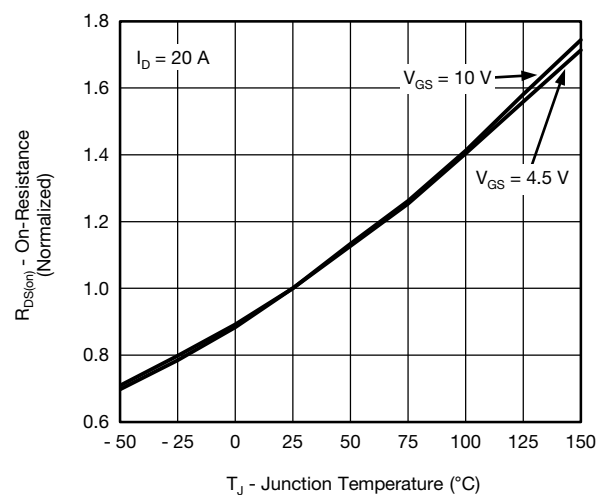
On-Resistance vs. Drain Current



Capacitance

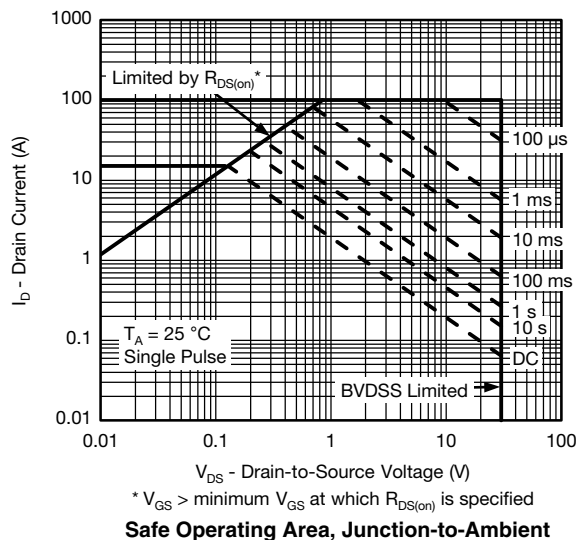
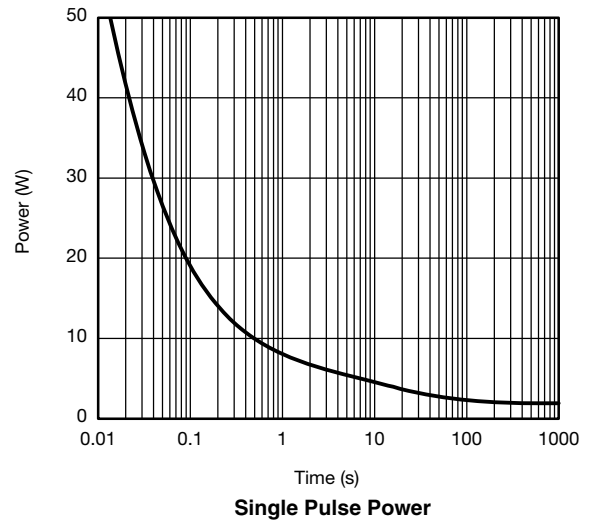
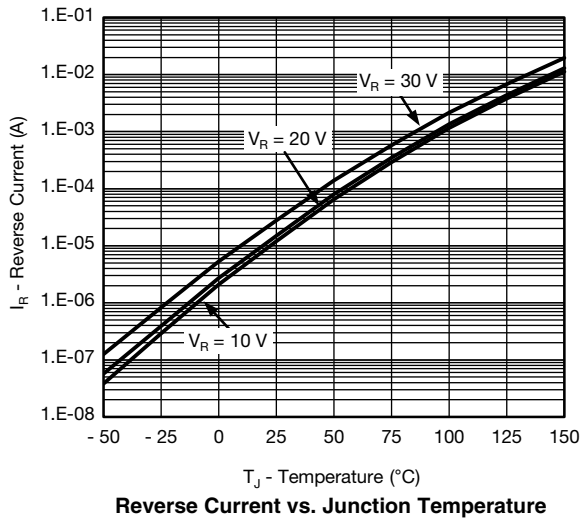
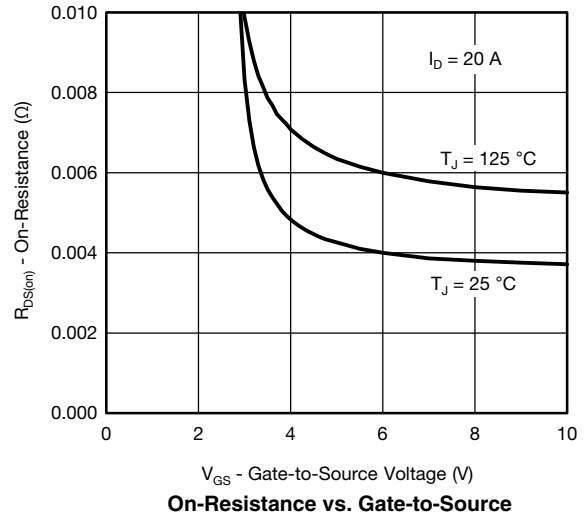
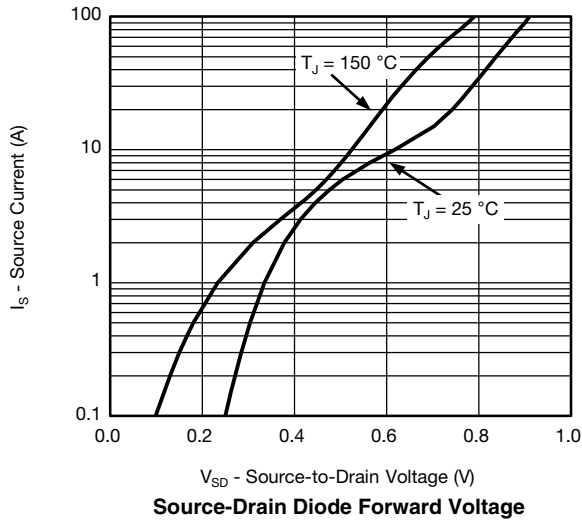


Gate Charge

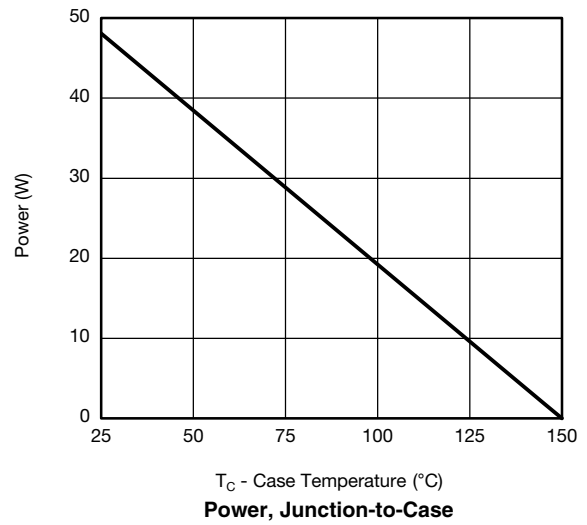
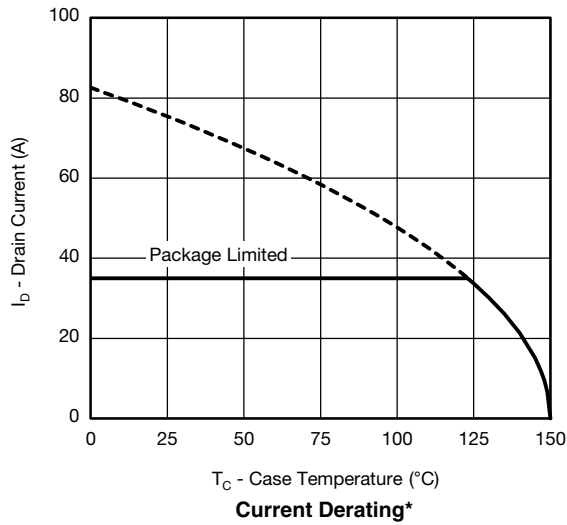


On-Resistance vs. Junction Temperature

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

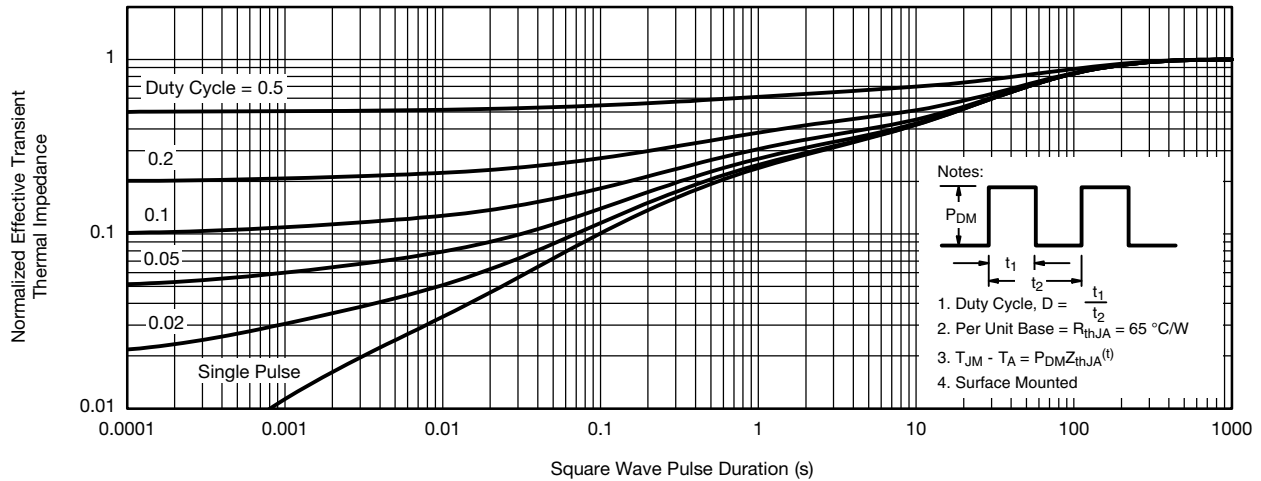


CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

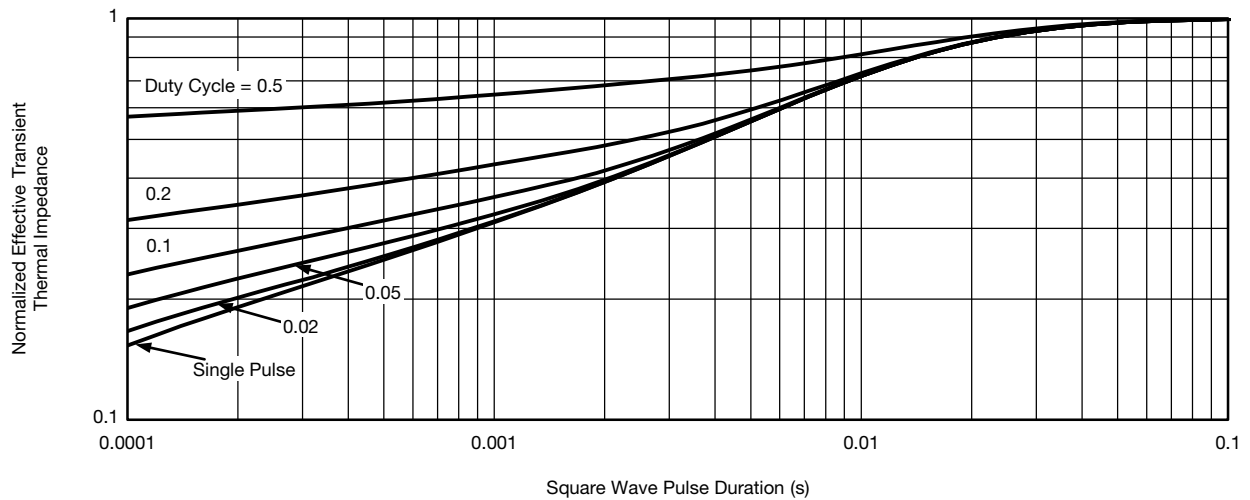


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67669.

PowerPAIR™ 6 x 3.7 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08 DWG: 5979						

RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7



Recommended PAD for PowerPAIR 6 x 3.7
Dimensions in inches (mm)
Keep-out 0.3520 (8.94) x 0.4390 (11.151)



Disclaimer

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