

Vishay Siliconix

N-Channel 30 V (D-S) MOSFET with Schottky Diode

DESCRIPTION

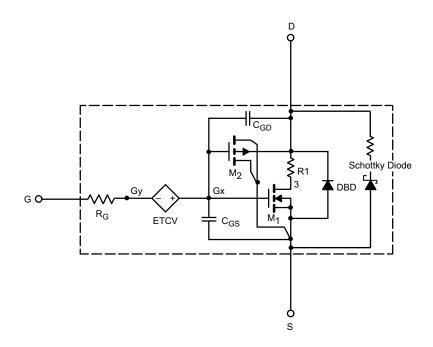
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.





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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.7	-	٧
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	0.0031	0.0029	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	0.0047	0.0041	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	76	85	S
Diode Forward Voltage ^a	V_{SD}	I _S = 5 A	0.50	0.51	V
Dynamic ^b					
Input Capacitance	C _{iss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	1920	1873	pF
Output Capacitance	Coss		788	760	
Reverse Transfer Capacitance	C _{rss}		86	52	
Total Gate Charge ^c	Q_g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	23	24	- nC
		$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	11.3	11.2	
Gate-Source Charge ^c	Q_{gs}		4.6	4.6	
Gate-Drain Charge ^c	Q_{gd}		2	2	

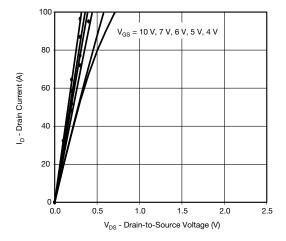
Notes

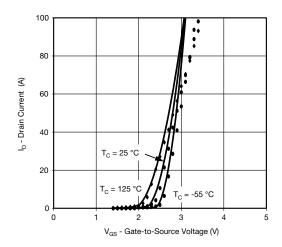
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

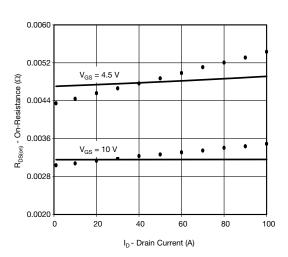
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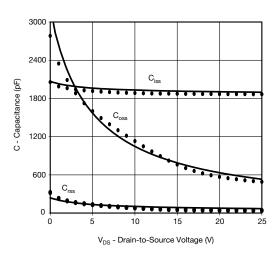
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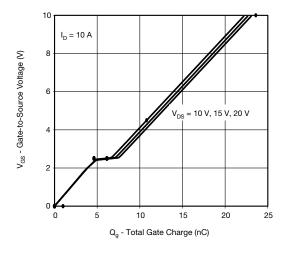
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}\text{C}$, unless otherwise noted)

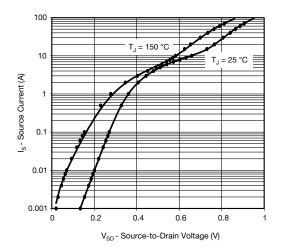












Note

· Dots and squares represent measured data.

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