Power MOSFETs

Power MOSFET Basics: Understanding the Turn-On Process

by Sanjay Havanur

The question of how to turn on a MOSFET might sound trivial, since ease of switching is a major advantage of field-effect transistors. Unlike bipolar junction transistors, these are majority carrier devices. One does not have to worry about current gain, tailoring the base current to match the extremes of h_{fe} and variable collector currents, or providing negative drives. Since MOSFETs are voltage driven, many users assume that they will turn on when a voltage, equal to or greater than the threshold, is applied to the gate. However, the question of how to turn on a MOSFET or, at a more basic level, what is the minimum voltage that should be applied to the gate, needs reappraisal with more and more converters being controlled digitally. While digital control offers the next level of flexibility and functionality, the DSPs, FPGAs, and other programmable devices with which it is implemented are designed to operate with low supply voltages. It is necessary to boost the final PWM signal to the level required by the MOSFET gate. This is where things begin to go wrong, because of the misconceptions about what really turns on a MOSFET. Many digital designers look at the gate threshold voltage and jump to the conclusion that, just as with their digital logic, the MOSFET will change state as soon as the threshold is crossed.

TABLE 1 - GATE THRESHOLD SPECIFICATION FOR SIR826ADP (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Gate-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	80	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	47	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.7	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.2	-	2.8	V

First, the threshold voltage $V_{GS(th)}$ is not intended for system designers. It is the gate voltage at which the drain current crosses the threshold of 250 µA. It is also measured under conditions that do not occur in real-world applications. In some cases a fixed V_{DS} of 5 V or higher may be used as the test condition, but is usually measured with gate and drain shorted together as stated. This does not require searching for fine print, it is clearly stated in the datasheet. Table 1 shows the $V_{GS(th)}$ specification and test conditions for the SiR826ADP. In many applications there are concerns about the so called "induced" gate voltage, such as in the low-side MOSFET of a synchronous buck. Again, taking the gate voltage above the threshold does not automatically drive the device into a shoot-through-induced failure. $V_{GS(th)}$ is a MOSFET designer's parameter and defines the point where the device is at the threshold of turning on. It is an indication of the beginning, nowhere near the end. Gate voltage should be held below the threshold in the off state to minimize the leakage. But during turn-on, system designers can, and should, ignore it altogether.

Another curve given on the datasheet refers to the MOSFET turning on with increasing gate voltage - the transfer characteristics. This is illustrated for the same SiR826ADP device in figure 1. However, the transfer characteristics are more a measure of current variation with respect to temperature and applied gate voltage. The V_{DS} is maintained at a constant but high value, sometimes as much as 15 V, and not always disclosed in the datasheet. In the curve shown below, at a current of 20 A it is not enough to apply 3.2 V to the gate. The combination would maintain a V_{DS} of 10 V typical and a continuous dissipation of 200 W. The transfer curve is quite important when the MOSFET is operated in the linear mode, but has little relevance for switching operations.

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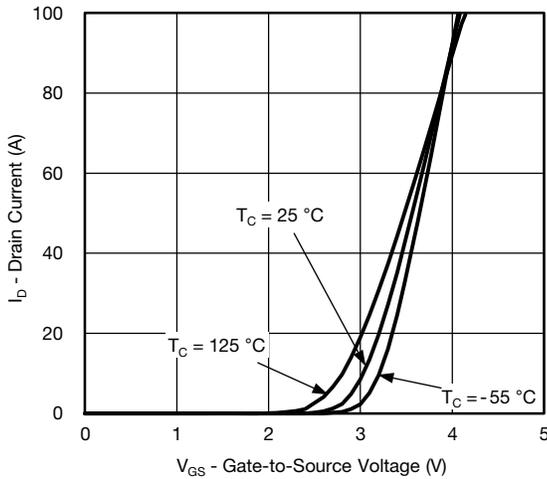
Fig. 1 - Transfer Characteristics
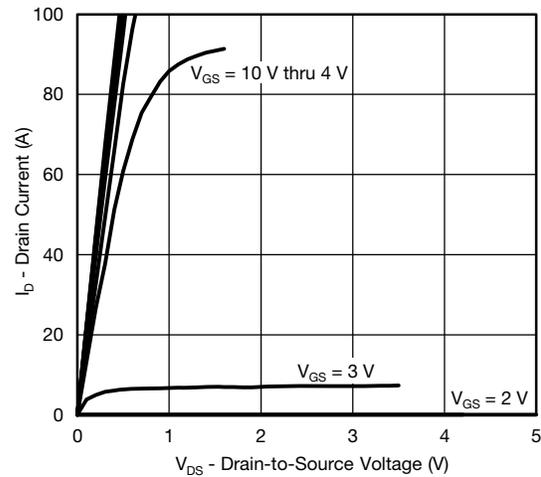
Fig. 2 - Output Characteristics

The curve that has data with the MOSFET fully on is called the output characteristics, as shown in figure 2. Here, the MOSFET forward drop is measured as a function of current for different values of V_{GS}. Designers may refer to this curve to ensure that the gate voltage is sufficient. For each gate voltage where $R_{DS(on)}$ is guaranteed, there is a range where the V_{DS} drop maintains strict linearity with current, beginning from zero. For lower values of gate voltage, as the current is increased the curve loses linearity, goes through a knee, and flattens out. Figure 3 shows the detailed output characteristics for gate voltages between 2.5 V to 3.6 V. MOSFET users usually think of this as the linear mode. However, device designers refer to the gray area as the current saturation region - for the given gate voltage, the current that can be delivered has reached its saturation limit. Any increase in applied V_{DS} will be sustained with only a slight increase in the current, whereas even a slight change in current can lead to a relatively large increase in V_{DS}. For higher gate voltages, when the MOSFET has been fully turned on, any operating point will be located in the area shaded in green to the left, marked as the resistive (or ohmic) region. Note that all curves are typical, with no minimum or maximum limits, and derived at 25 °C. At lower temperatures the gate voltage required to keep the device in the resistive region will be higher, increasing at the rate of 0.3 %/°C.
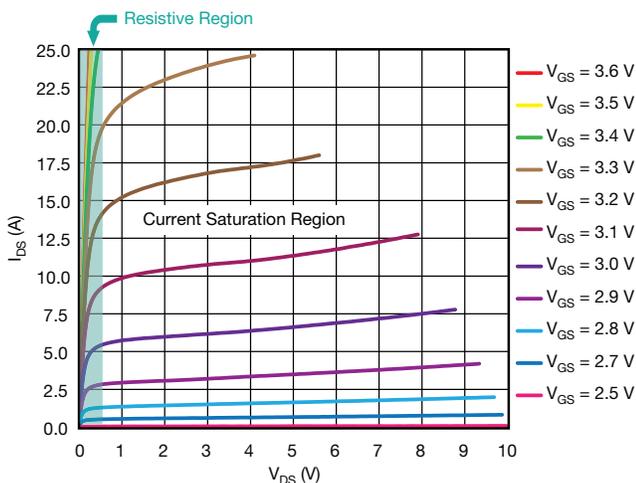
Fig. 3 - Expanded Output Characteristics
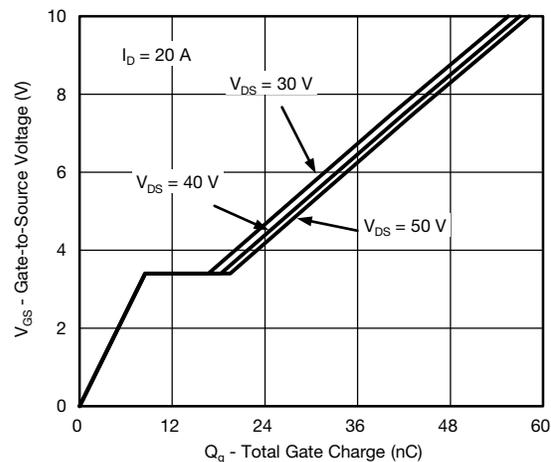
Fig. 4 - Gate Charge Characteristics

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When confronted with the output characteristics, designers invariably demand to know the $R_{DS(on)}$ at their particular operating conditions. Typically it will be at a combination of V_{GS} and I_{DS}, where the curve has strayed from the straight and narrow line into the gray area. For example, in the case above it could be a gate voltage $V_{GS} = 3.1$ V and a startup current of 10 A. They understand $R_{DS(on)}$ will be higher than specified, but can the MOSFET manufacturer provide an approximate indication? Since both V_{DS} and I_{DS} are available on the curve, there is a temptation, often succumbed to, to divide the two and arrive at the "effective" $R_{DS(on)}$. Unfortunately there is no $R_{DS(on)}$ to calculate here. It does not exist under the given conditions. Any segment of the load line that represents a resistance must pass through the origin in a linear fashion. One can of course model the load line in its entirety as a non-linear resistance. If nothing else it will ensure that any understanding of real-world behavior is maintained at the origin (0, 0).

The real clue to turning on the MOSFET is provided by the gate charge curve shown in figure 4. While the curve is routinely offered for every MOSFET, its implications are not always understood by designers. In addition, recent developments in MOSFET technology, like trench and shielded gates and charge-compensating superjunction structures, demand a fresh appraisal of this information. To start with, the term "gate charge" itself is somewhat misleading. The linearized and segmented curve does not look like the charging voltage of any capacitor, no matter how non-linear its value. In reality the gate charge curve represents a superposition of two capacitors which are not in parallel, have different values, and carry different voltages. In the literature, the effective capacitance as seen from gate terminal is defined as

$$C_{iss} = C_{gs} + C_{gd}.$$

While this is a convenient entity to measure and specify in the datasheet, it is worth noting that C_{iss} is not a physical capacitance. It would be a misconception to imagine that the MOSFET is turned on by simply applying a voltage to "the gate capacitance C_{iss}." As shown in figure 5, prior to turn-on the gate source capacitance C_{gs} is uncharged, but the gate drain capacitance C_{gd} has a negative voltage / charge which needs to be removed. Both capacitors are non-linear, whose values can vary widely with respect to applied voltage. The switching characteristics, therefore, are dependent more on their stored charges rather than the capacitance value at any given voltage.
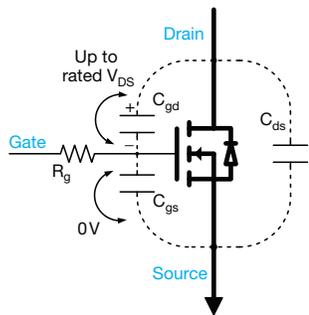

**Fig. 5 - Gate Capacitances with Initial Voltages**
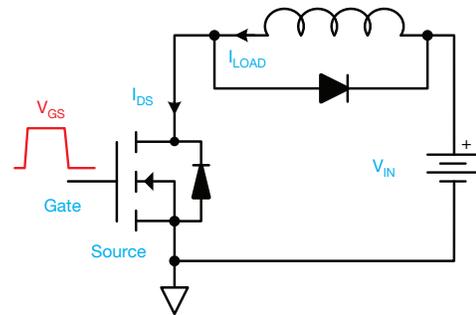
Fig. 6 - Simplified Inductive Turn-On Circuit

Since the two component capacitances that make up C_{iss} are physically different and are charged to different voltages, the turn-on process also has two stages. The exact sequence is different for inductive and resistive loads; however, in most practical applications the load is heavily inductive and can be described using the circuit model shown in fig 6. With reference to the timing diagram in figure 7,

T0 - T1: C_{gs} is charged from zero to $V_{GS(th)}$. There is no change in V_{DS} or I_{DS}.

T1 - T2: Current begins to rise in the device as the gate voltage rises from $V_{GS(th)}$ to the plateau voltage V_{gp}. I_{DS} rises from 0 A to the full load current, but there is no change in V_{DS}. The charge associated is the integral of C_{gs} from 0 V to V_{gp} and specified in the datasheets as Q_{gs}.

T2 - T3: The flat region between T2 and T3 is also known as the Miller plateau. Prior to turn-on, C_{gd} is charged to supply voltage V_{IN} and holds it till I_{DS} has peaked to I_{LOAD} at T2. Between T2 and T3, the negative charge of $(V_{IN} - V_{gp})$ is converted to the positive charge corresponding to the plateau voltage V_{gp}. This is also seen as the fall of the drain voltage from V_{IN} to near zero. The charge associated is approximately the integral of C_{gd} from zero to V_{IN} and specified in the datasheets as Q_{gd}.

T3 - T4: As the gate voltage rises from V_{gp} to V_{GS}, there is very little change in V_{DS} or I_{DS}. However, the effective $R_{DS(on)}$ reduces marginally with rising gate voltage. At some voltage above V_{gp}, the manufacturers feel confident enough to guarantee an upper limit on the effective $R_{DS(on)}$.

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When the load is inductive, the rise of the current in the MOSFET channel must be completed before the voltage begins to fall. At the beginning of the plateau, the device is off with simultaneous high current and voltage across drain and source. Between T2 and T3, a charge of Q_{gd} is delivered to the gate, and at the end of it the MOSFET characteristic has changed from constant current to constant resistance mode. During this entire transition there is no significant change in the gate voltage V_{gp}, which is why it is not meaningful to associate the turning on of a MOSFET with any specific gate voltage.

Similar analysis can be made for turn-off, where the same two charges must be removed from the gate in reverse order. While the sum of Q_{gs} and Q_{gd} guarantees that the MOSFET will be fully on, it does not guarantee how fast. The rate of change in voltage or current is determined by the rate at which the gate charge components are applied or removed, which is nothing but the gate drive current. While fast rise and fall times are necessary to reduce switching losses, they also introduce system-level problems of high peak voltages, ringing, and EMI, especially during inductive turn-off.
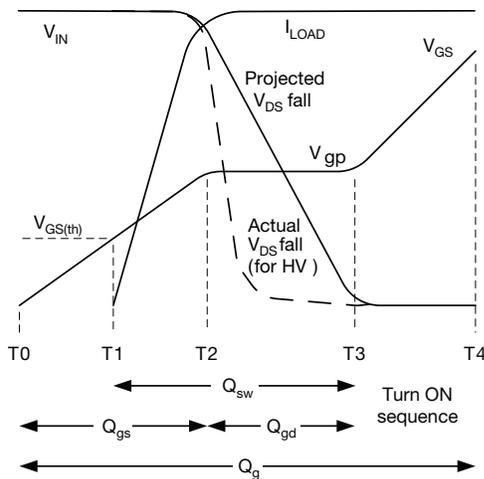
Fig. 7 - Gate Charge Components and Timings
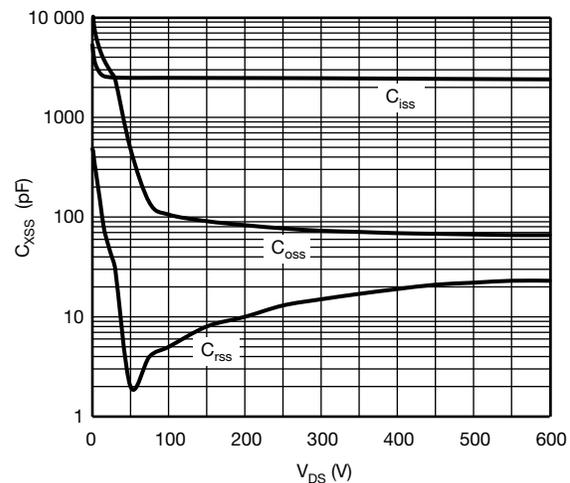
Fig. 8 - Capacitance Variations w.r.t. Applied V_{DS}

The simplified linear voltage fall shown in figure 7 assumes a constant value of C_{gd}, which is rarely true for real MOSFETs. In particular, the C_{gd} of a high-voltage superjunction MOSFET shows extreme non-linear behavior, as illustrated in figure 8 for the SiHF35N60E. There is more than a 200:1 variation in C_{rss} value within the first 100 V. As a result, the actual fall time of voltage against the gate charge curve may look more like the red dashed line in figure 7. The rise and fall times, and their corresponding dV/dt values, depend more on the C_{rss} values at higher voltages rather than the integral of the entire curve specified as Q_{gd}. While comparing devices across different design platforms, users need to be aware that a MOSFET with half the Q_{gd} will not necessarily switch twice as fast or have half the switching losses. Depending on the shape of the C_{gd} curve and its value at higher voltages, it is quite possible to have a device that has low Q_{gd} in the datasheet but shows no increase in switching speed.

CONCLUSIONS

In the real world, turning on a MOSFET is not an event but a process. Designers have to stop thinking of applying a $V_{GS(th)}$, or some other voltage, as an input at the gate which will toggle the output from high to low $R_{DS(on)}$. Questions like what is the $R_{DS(on)}$ at a gate voltage below some value or the other, are not valid because it is not the gate voltage per se that turns on a MOSFET. It is the two charges Q_{gs} and Q_{gd}, injected into the device through the gate pin, that do the job. The gate voltage will rise above $V_{GS(th)}$ and V_{gp} in the process, but that is secondary. The speed with which a modern power MOSFET turns on or off is also not a simple function of Q_{gs} or Q_{gd}. A detailed study of both the gate charge curve and capacitance characteristics is necessary to compare switching speeds, especially for superjunction MOSFETs.

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