

## N- and P-Channel 40 V (D-S) 175 °C MOSFET

### DESCRIPTION

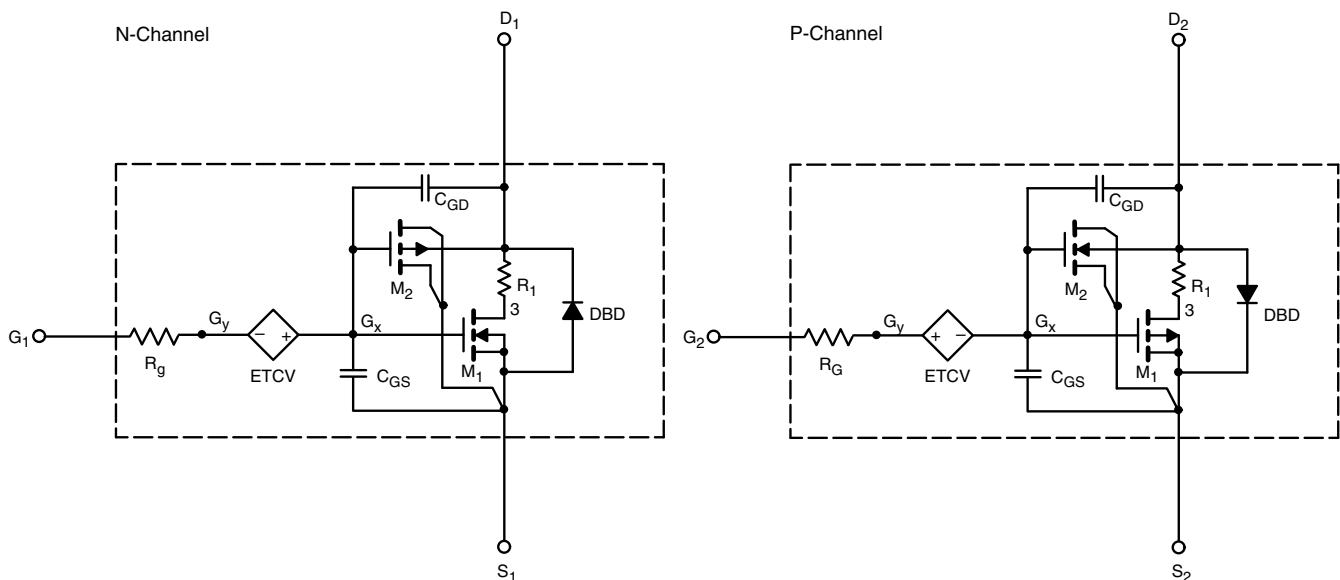
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N- and p-channel vertical DMOS
- Macro model (Sub-circuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



| SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted) |                     |   |      |                |               |      |
|---|---------------------|---|------|----------------|---------------|------|
| PARAMETER   | SYMBOL              | TEST CONDITIONS   |      | SIMULATED DATA | MEASURED DATA | UNIT |
| <b>Static</b>   |                     |   |      |                |               |      |
| Gate-Source Threshold Voltage                                   | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA   | N-Ch | 2              | -             | V    |
|   |                     | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA  | P-Ch | 2              | -             |      |
| Drain-Source On-State Resistance <sup>a</sup>                   | R <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.8 A  | N-Ch | 0.0074         | 0.0077        | Ω    |
|   |                     | V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6 A  | P-Ch | 0.0200         | 0.0220        |      |
|   |                     | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8.9 A   | N-Ch | 0.0095         | 0.0094        |      |
|   |                     | V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.7 A   | P-Ch | 0.0350         | 0.0360        |      |
| Forward Transconductance <sup>a</sup>                           | g <sub>fs</sub>     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.8 A  | N-Ch | 50             | 65            | S    |
|   |                     | V <sub>DS</sub> = -15 V, I <sub>D</sub> = -6 A  | P-Ch | 15             | 16            |      |
| Diode Forward Voltage <sup>a</sup>                              | V <sub>SD</sub>     | I <sub>S</sub> = 6.5 A, V <sub>GS</sub> = 0 V   | N-Ch | 0.79           | 0.79          | V    |
|   |                     | I <sub>S</sub> = -3.4 A, V <sub>GS</sub> = 0 V  | P-Ch | -0.78          | -0.78         |      |
| <b>Dynamic <sup>b</sup></b>                                     |                     |   |      |                |               |      |
| Input Capacitance   | C <sub>iss</sub>    | N-Channel<br>V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz<br><br>P-Channel<br>V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, f = 1 MHz                             | N-Ch | 1500           | 1474          | pF   |
| Output Capacitance  | C <sub>oss</sub>    |   | P-Ch | 1320           | 1302          |      |
|   |                     |   | N-Ch | 223            | 218           |      |
| Reverse Transfer Capacitance                                    | C <sub>rss</sub>    |   | P-Ch | 223            | 222           |      |
|   |                     |   | N-Ch | 91             | 89            |      |
| P-Ch  | 154                 |   | 154  |                |               |      |
| Total Gate Charge   | Q <sub>g</sub>      | N-Channel<br>V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A<br><br>P-Channel<br>V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A | N-Ch | 24             | 25.5          | nC   |
| Gate-Source Charge  | Q <sub>gs</sub>     |   | P-Ch | 27             | 30.2          |      |
|   |                     |   | N-Ch | 4.4            | 4.4           |      |
| Gate-Drain Charge   | Q <sub>gd</sub>     |   | P-Ch | 4.1            | 4.1           |      |
|   |                     |   | N-Ch | 4.3            | 4.3           |      |
| P-Ch  | 7.4                 |   | 7.4  |                |               |      |

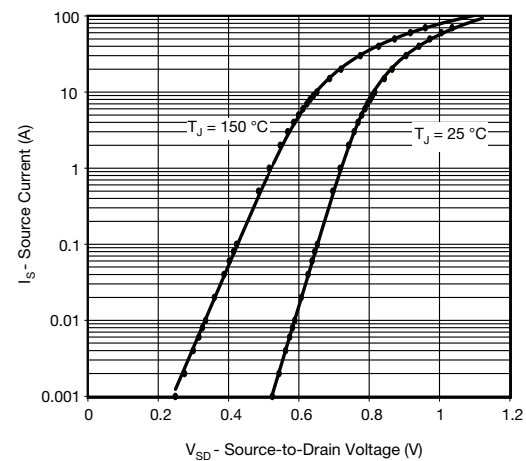
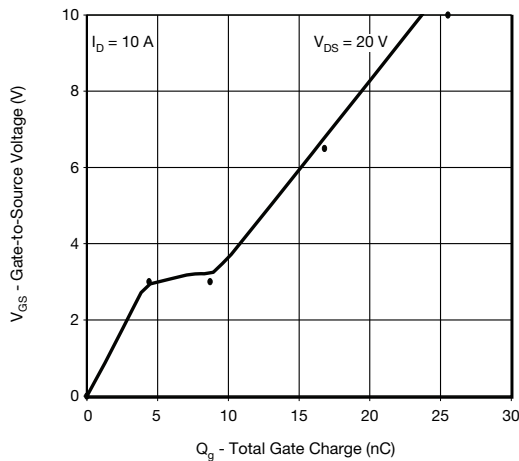
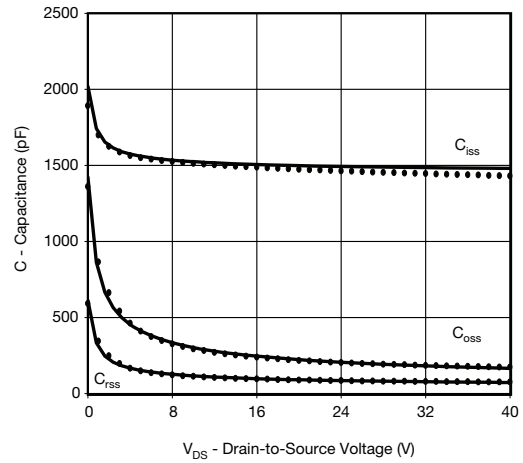
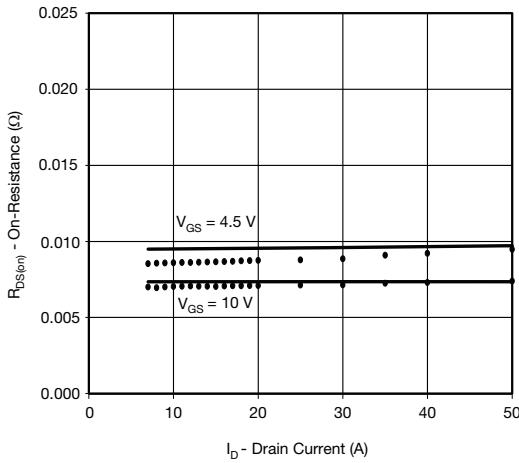
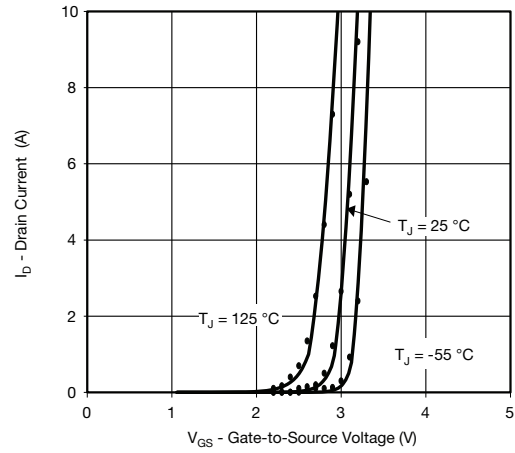
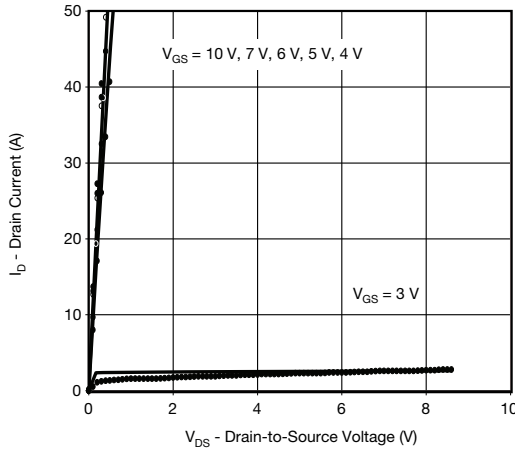
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

### N-Channel MOSFET



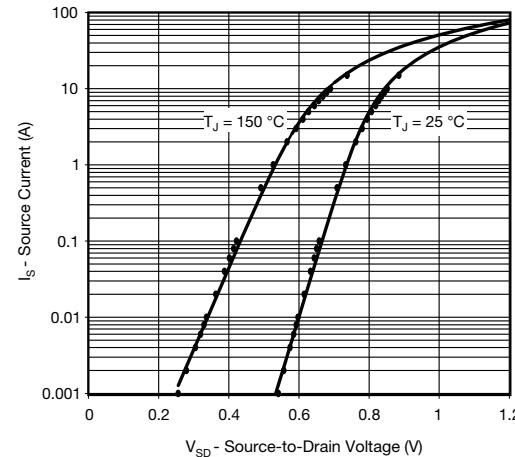
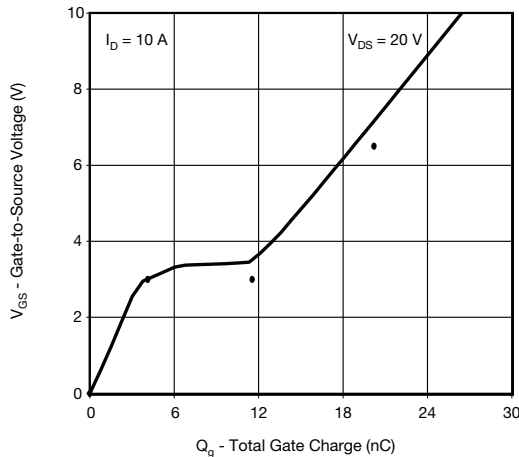
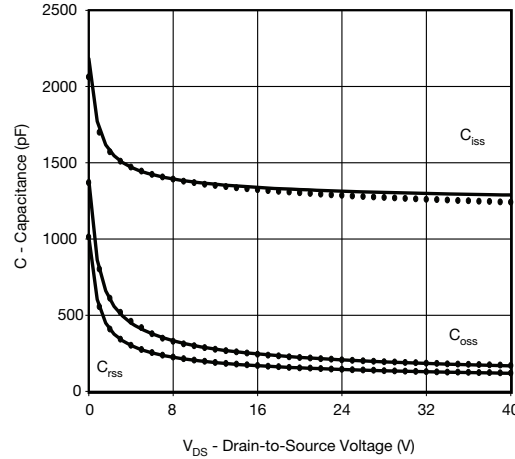
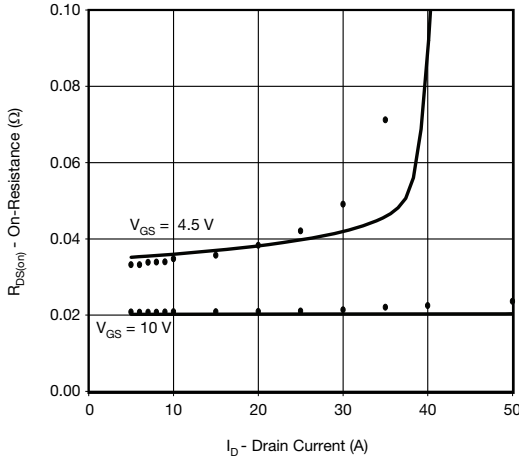
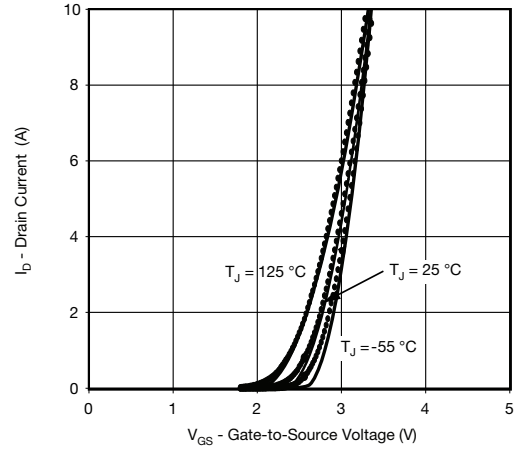
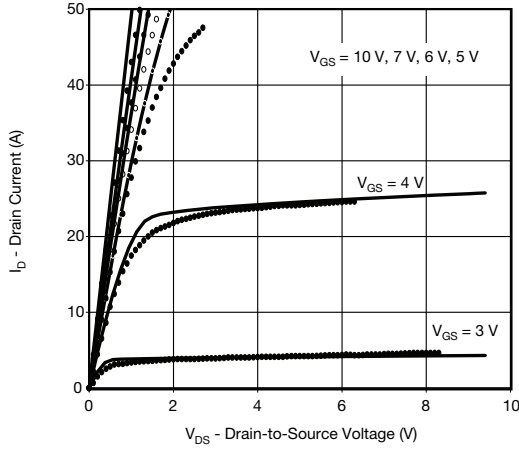
### Note

- Dots and squares represent measured data.



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

### P-Channel MOSFET



#### Note

- Dots and squares represent measured data.

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