P-Channel 20 V (D-S) MOSFET

DESCRIPTION

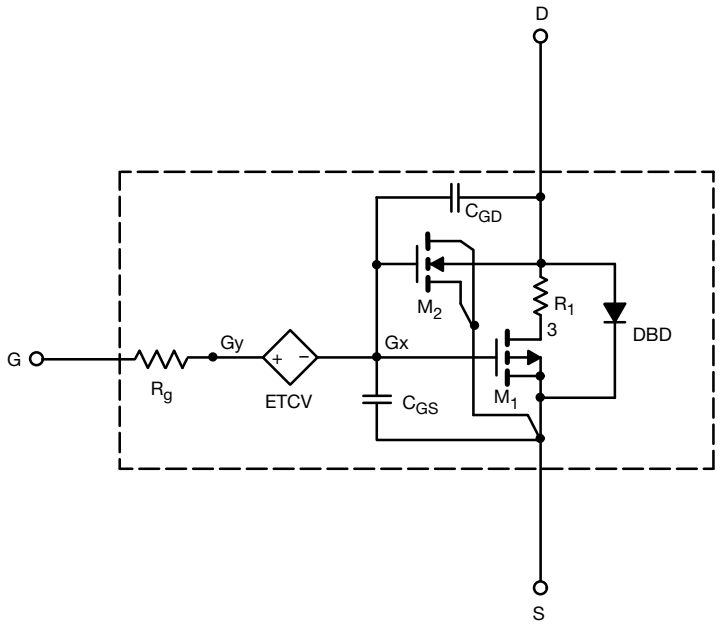
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (Sub-circuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUB-CIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

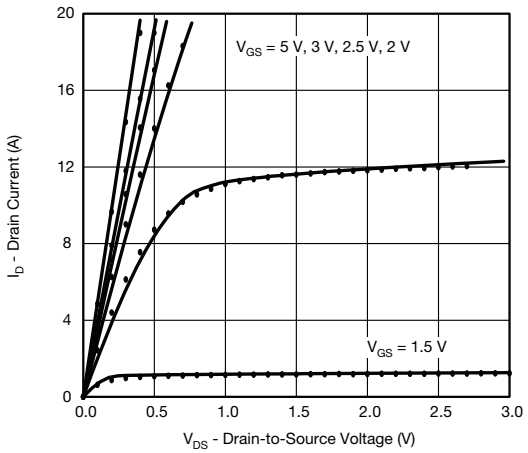
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	0.7	-	V
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D = -5.2 A	0.022	0.025	Ω
		V_{GS} = -2.5 V, I_D = -4.8 A	0.029	0.030	
		V_{GS} = -1.8 V, I_D = -2 A	0.038	0.040	
Forward Transconductance [a]	g_{fs}	V_{DS} = -6 V, I_D = -5.2 A	22	20	S
Diode Forward Voltage	V_{SD}	I_S = -4.2 A	-0.8	-0.8	V
Dynamic [b]					
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	1310	1300	pF
Output Capacitance	C_{oss}		226	210	
Reverse Transfer Capacitance	C_{rss}		196	180	
Total Gate Charge	Q_g	V_{DS} = -10 V, V_{GS} = -8 V, I_D = -5.2 A	26	30	nC
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -5.2 A	16	16	
Gate-Source Charge	Q_{gs}		2.1	2.1	
Gate-Drain Charge	Q_{gd}		4.8	4.8	

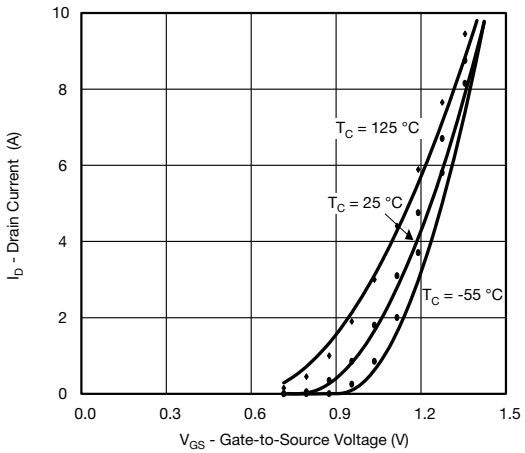
Notes

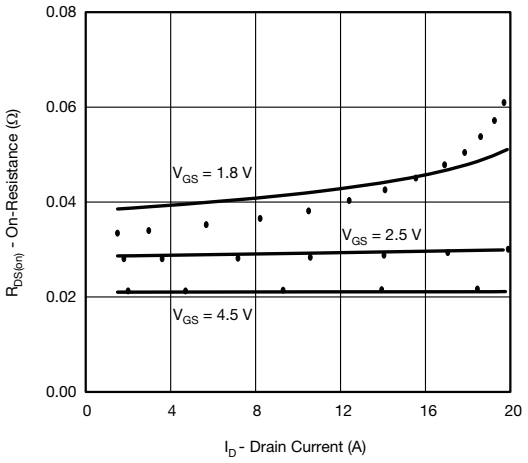
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

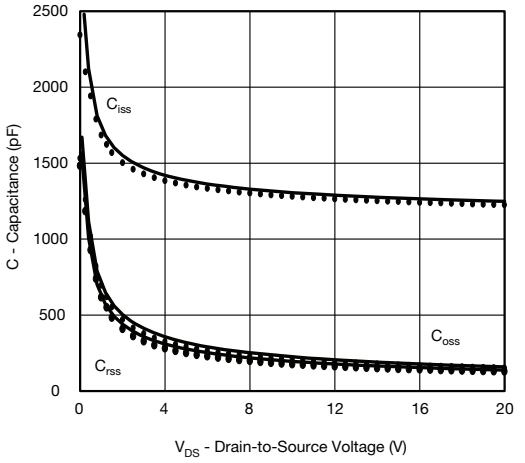
b. Guaranteed by design, not subject to production testing.

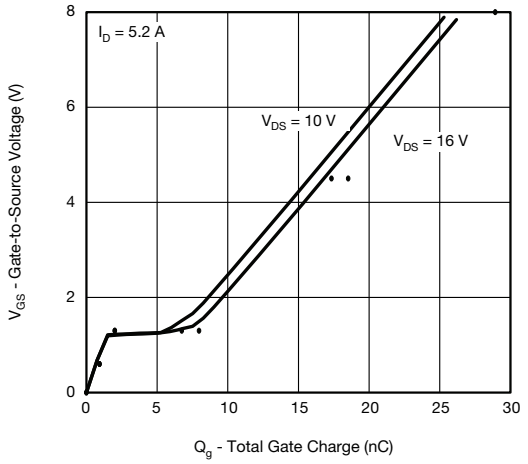
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

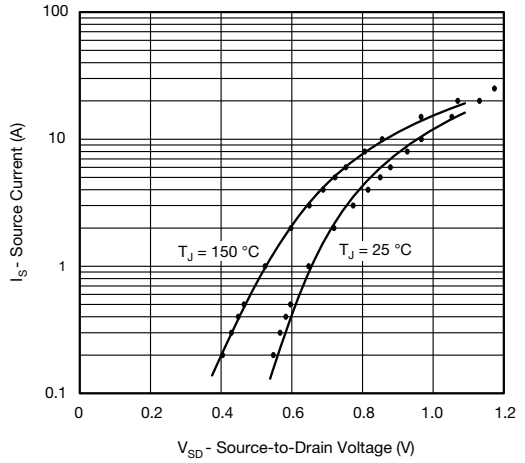












Note

- Dots and squares represent measured data.

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