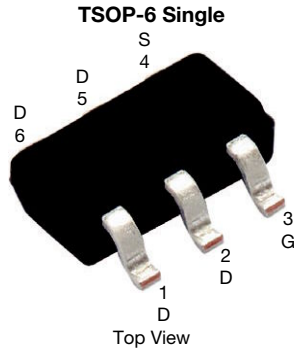


P-Channel 30 V (D-S) MOSFET



Marking code: AU

PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.034
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.053
Q_g typ. (nC)	11.5
I_D (A) ^a	-8
Configuration	Single

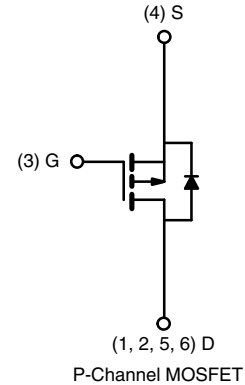
FEATURES

- TrenchFET[®] power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- Load Switch



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3483CDV-T1-E3
Lead (Pb)-free and halogen-free	Si3483CDV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	-30	V	
Gate-source voltage	V_{GS}	± 20		
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-8 ^a	A
		$T_C = 70$ °C	-7	
		$T_A = 25$ °C	-6.1 ^{b, c}	
		$T_A = 70$ °C	-4.9 ^{b, c}	
Pulsed drain current	I_{DM}	-25	A	
Continuous source-drain diode current	I_S	$T_C = 25$ °C		
		$T_A = 25$ °C	-1.67 ^{b, c}	
Maximum power dissipation	P_D	$T_C = 25$ °C	4.2	W
		$T_C = 70$ °C	2.7	
		$T_A = 25$ °C	2 ^{b, c}	
		$T_A = 70$ °C	1.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{b, d}	R_{thJA}	55	62.5	°C/W	
Maximum junction-to-foot (drain)	R_{thJF}	25	30		

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 110 °C/W



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-30	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-32	-	mV/ $^\circ\text{C}$	
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	5	-		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1	-	-3	V	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	-1	μA	
		$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^\circ\text{C}$	-	-	-10		
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -10\text{ V}$	-20	-	-	A	
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -6.1\text{ A}$	-	0.027	0.034	Ω	
		$V_{GS} = -4.5\text{ V}$, $I_D = -2\text{ A}$	-	0.044	0.053		
Forward transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -6.1\text{ A}$	-	13	-	S	
Dynamic ^b							
Input capacitance	C_{iss}	$V_{DS} = -15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	1000	-	μF	
Output capacitance	C_{oss}		-	170	-		
Reverse transfer capacitance	C_{rss}		-	140	-		
Total gate charge	Q_g	$V_{DS} = -15\text{ V}$, $V_{GS} = -10\text{ V}$, $I_D = -6.1\text{ A}$	-	22	33	nC	
		$V_{DS} = -15\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -6.1\text{ A}$	-	11.5	18		
Gate-source charge	Q_{gs}		-	3.4	-		
Gate-drain charge	Q_{gd}		-	5.7	-		
Gate resistance	R_g	$f = 1\text{ MHz}$	-	5.6	-	Ω	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 3.1\text{ }\Omega$ $I_D \cong -4.9\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	45	70	ns	
Rise time	t_r		-	135	205		
Turn-off delay time	$t_{d(off)}$		-	25	40		
Fall time	t_f		-	15	25		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 3.1\text{ }\Omega$ $I_D \cong -4.9\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	-	10	15		
Rise time	t_r		-	15	25		
Turn-off delay time	$t_{d(off)}$		-	30	45		
Fall time	t_f		-	10	15		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	-3.5		A
Pulse diode forward current ^a	I_{SM}		-	-	-25		
Body diode voltage	V_{SD}	$I_S = -4.9\text{ A}$	-	-0.8	-1.2	V	
Body diode reverse recovery time	t_{rr}	$I_F = -4.9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	-	25	50	ns	
Body diode reverse recovery charge	Q_{rr}		-	17	35	nC	
Reverse recovery fall time	t_a		-	14	-	ns	
Reverse recovery rise time	t_b		-	11	-		

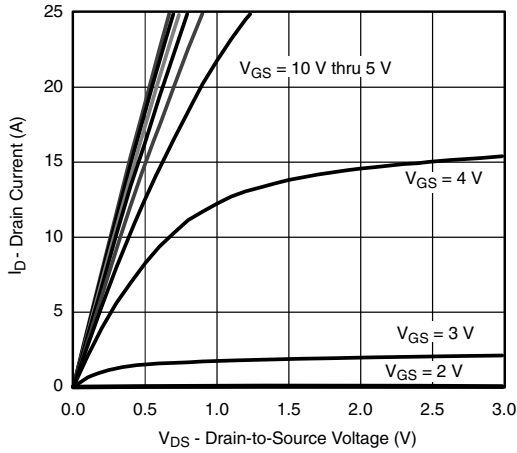
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

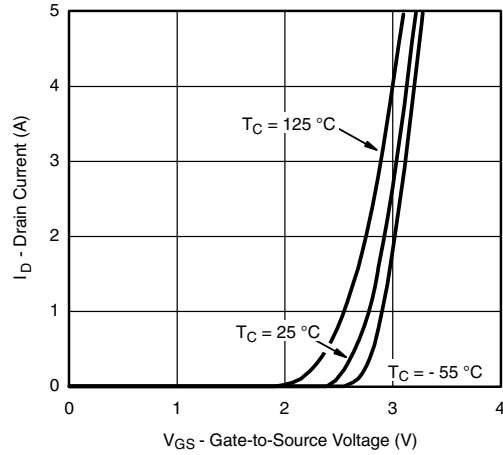
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



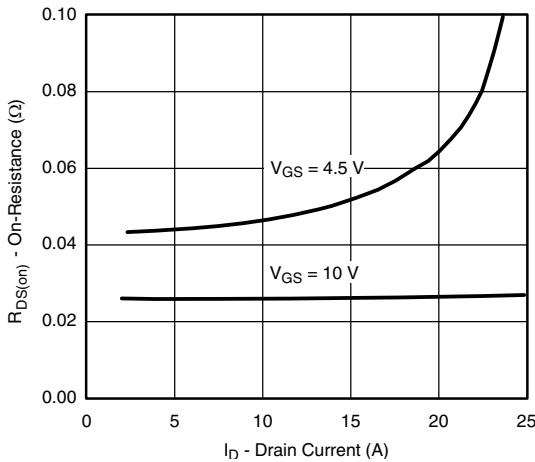
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



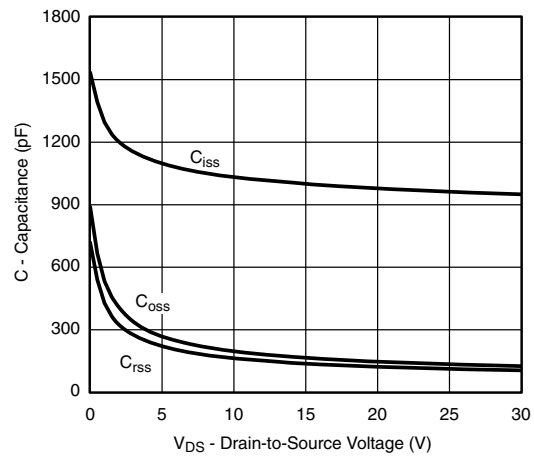
Output Characteristics



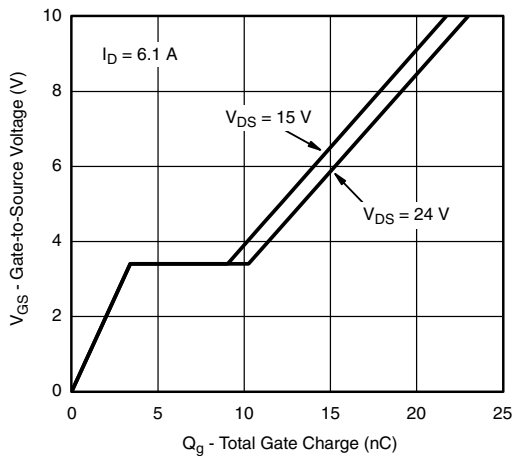
Transfer Characteristics



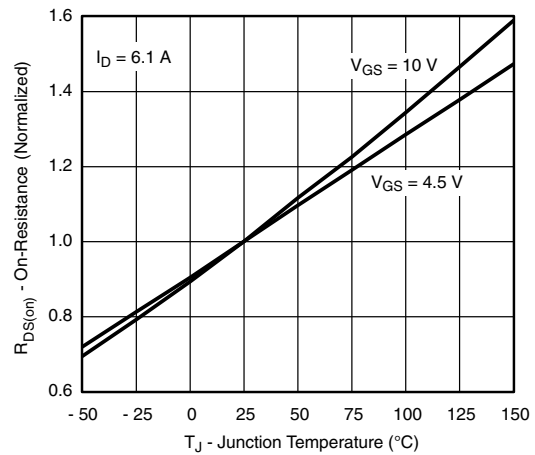
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



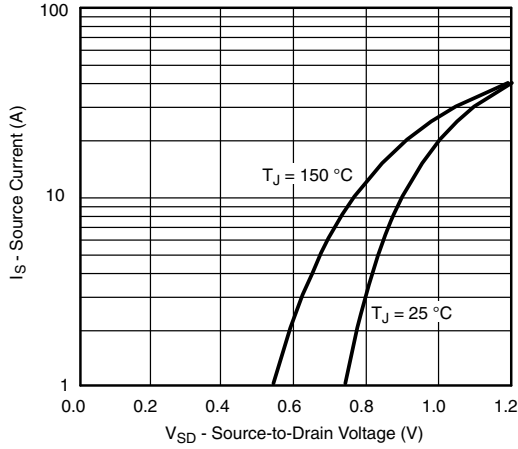
Gate Charge



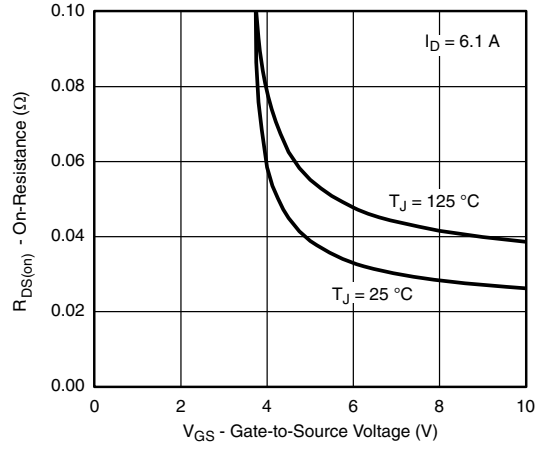
On-Resistance vs. Junction Temperature



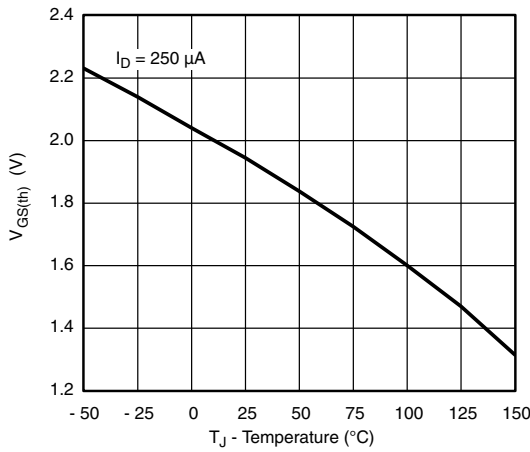
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



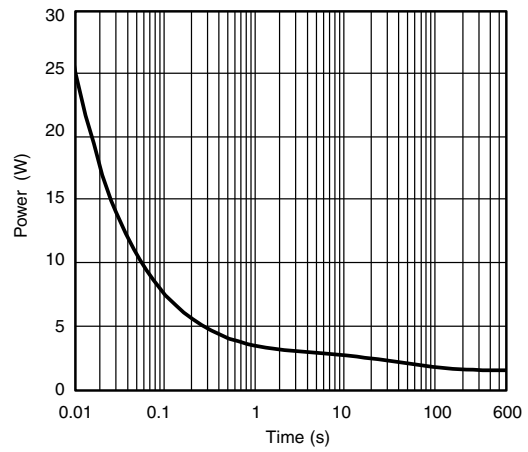
Source-Drain Diode Forward Voltage



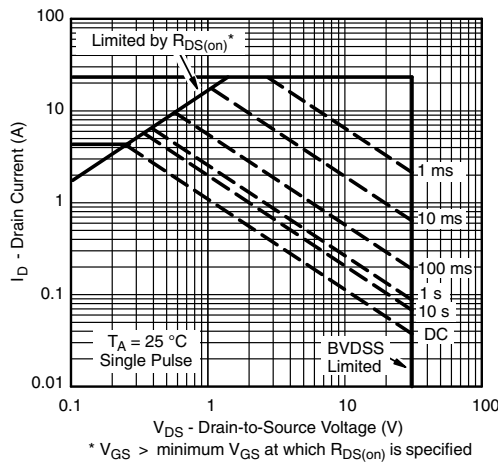
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



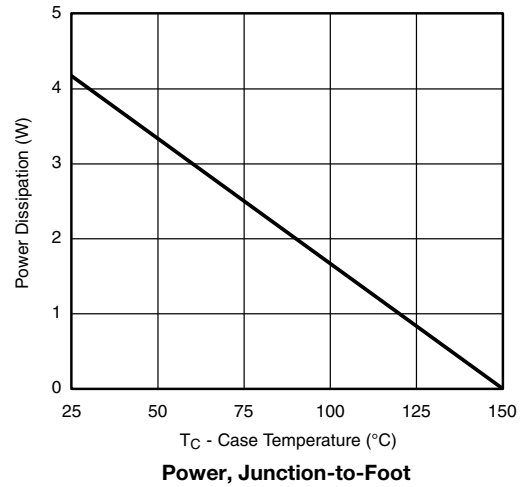
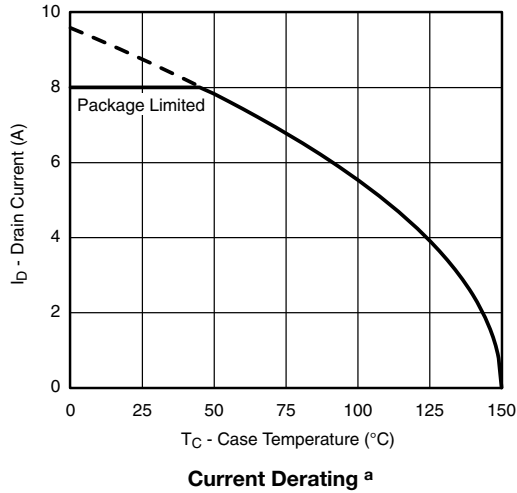
Single Pulse Power



Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

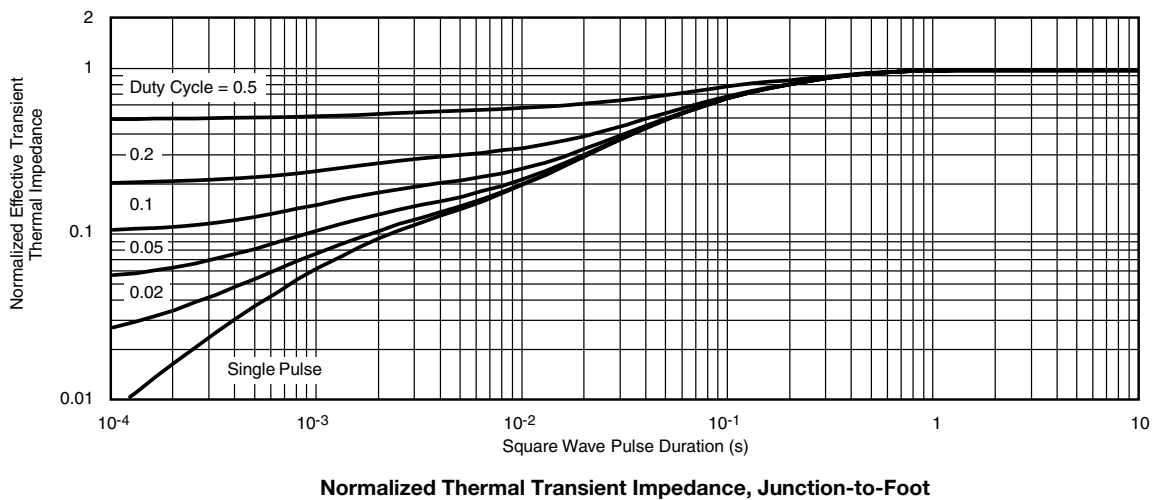
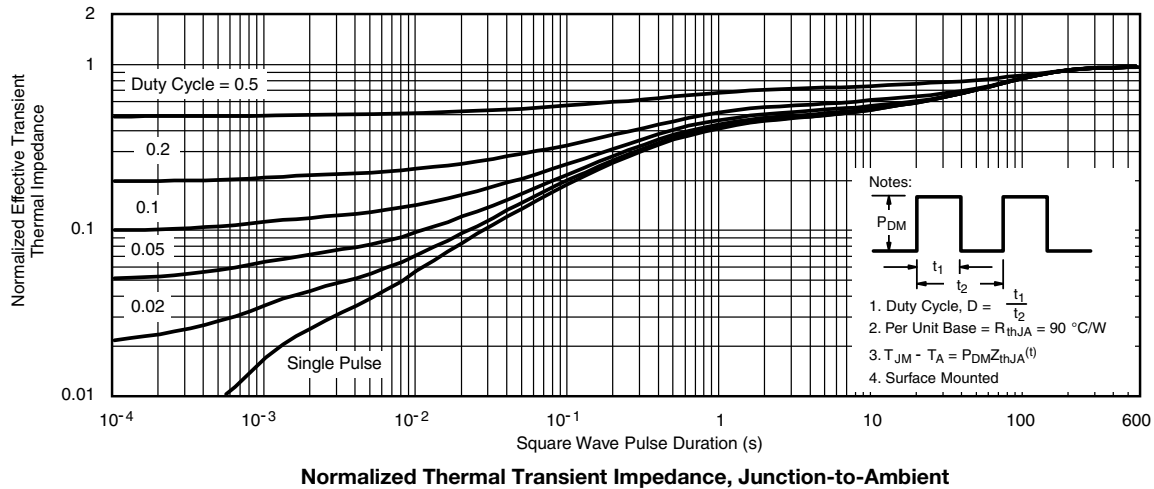


Notes

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68603.

TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C



5-LEAD TSOP



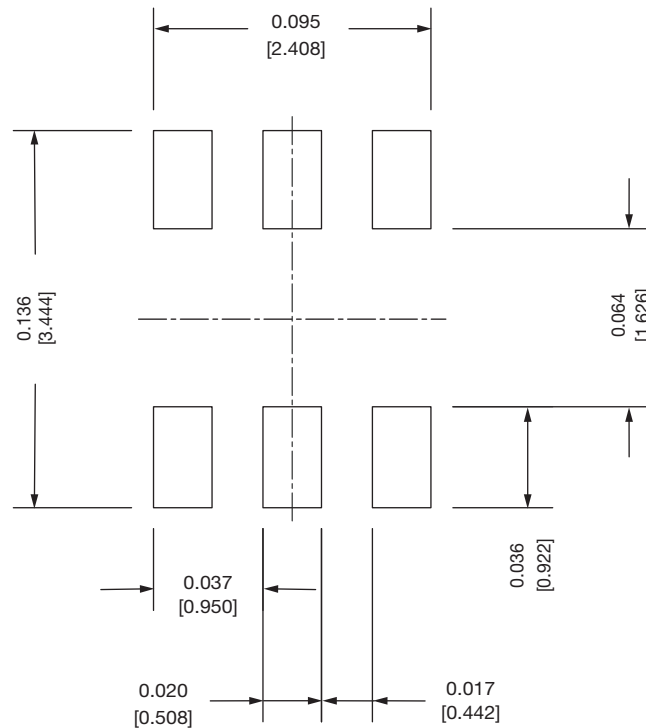
6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A₁	0.01	-	0.10	0.0004	-	0.004
A₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L₁	0.60 Ref			0.024 Ref		
L₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
 DWG: 3010



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