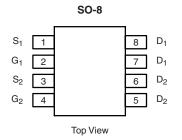


Vishay Siliconix

COMPLIANT

Dual P-Channel 30-V (D-S) MOSFET

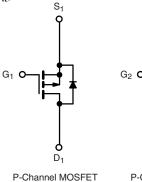
PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{d, e}	Q _g (Typ.)		
- 30	0.029 at V _{GS} = - 10 V	- 8	15 nC		
	0.041 at V _{GS} = - 4.5 V	- 8	13110		



Ordering Information: Si4925DDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested
- APPLICATIONS
- Load Switches
 - Notebook PCs
 - Desktop PCs
 - Game Stations



D₂ P-Channel MOSFET

 S_2

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted Parameter Symbol Limit Unit V_{DS} - 30 **Drain-Source Voltage** ٧ Gate-Source Voltage V_{GS} ± 20 T_C = 25 °C - 8.0^e T_C = 70 °C - 8.0^e Continuous Drain Current (T_J = 150 °C) I_D - 7.3^{a, b} T_A = 25 °C $T_A = 70 \ ^{\circ}C$ - 5.9^{a, b} A - 32^e Pulsed Drain Current I_{DM} T_C = 25 °C - 4.1 Continuous Source-Drain Diode Current I_S T_A = 25 °C - 2.0^{a, b} Avalanche Current I_{AS} - 20 L = 0.1 mHSingle-Pulse Avalanche Energy E_{AS} 20 mJ T_C = 25 °C 5.0 T_C = 70 °C 3.2 P_D Maximum Power Dissipation W T_A = 25 °C 2.5^{a, b} 1.6^{a, b} T_A = 70 °C Operating Junction and Storage Temperature Range T_J, T_{sta} - 55 to 150 °C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot	Steady State	R _{thJF}	20	25	C/W	

Notes:

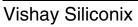
a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under Steady State conditions is 85 $^{\circ}\text{C/W}.$

d. Based on T_C = 25 °C.

e. Limited by package.





Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					1	1	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 31		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 1.0		- 3.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
	1	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1	μΑ	
Zero Gate Voltage Drain Current	IDSS	V_{DS} = - 30 V, V_{GS} = 0 V, T_{J} = 55 °C			- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge$ - 10 V, V_{GS} = - 10 V	- 30			Α	
	_	V _{GS} = - 10 V, I _D = - 7.3 A		0.024	0.029	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 6.2 A		0.033	0.041		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 9.1 A		23		S	
Dynamic ^b	•						
Input Capacitance	C _{iss}			1350			
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		215		pF	
Reverse Transfer Capacitance	C _{rss}			185			
Total Gate Charge	Q_{g} $V_{DS} = -15 V, V_{GS} = -10 V, I_{D} =$	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 9.1 A		32	50		
				15	25		
Gate-Source Charge	Q _{gs}	V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_{D} = - 9.1 A		4		nC	
Gate-Drain Charge	Q _{gd}			7.5			
Gate Resistance	R _g	f = 1 MHz		5.8		Ω	
Turn-On Delay Time	t _{d(on)}			10	15		
Rise Time	t _r	V_{DD} = - 15 V, R_L = 15 Ω		8	15		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 1 Ω		45	70		
Fall Time	t _f			12	25		
Turn-On Delay Time	t _{d(on)}			42	70	ns	
Rise Time	t _r	V_{DD} = - 15 V, R_L = 15 Ω		35	60	-	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		40	70		
Fall Time	t _f			16	30		
Drain-Source Body Diode Characterist	tics						
Continous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 4.1	A	
Pulse Diode Forward Current	I _{SM}				- 32	A	
Body Diode Voltage	V _{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.75	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			34	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 2 A, dl/dt = 100 A/μs, T _J = 25 °C		22	40	nC	
Reverse Recovery Fall Time	t _a			11			
Reverse Recovery Rise Time	t _b			23		ns	

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

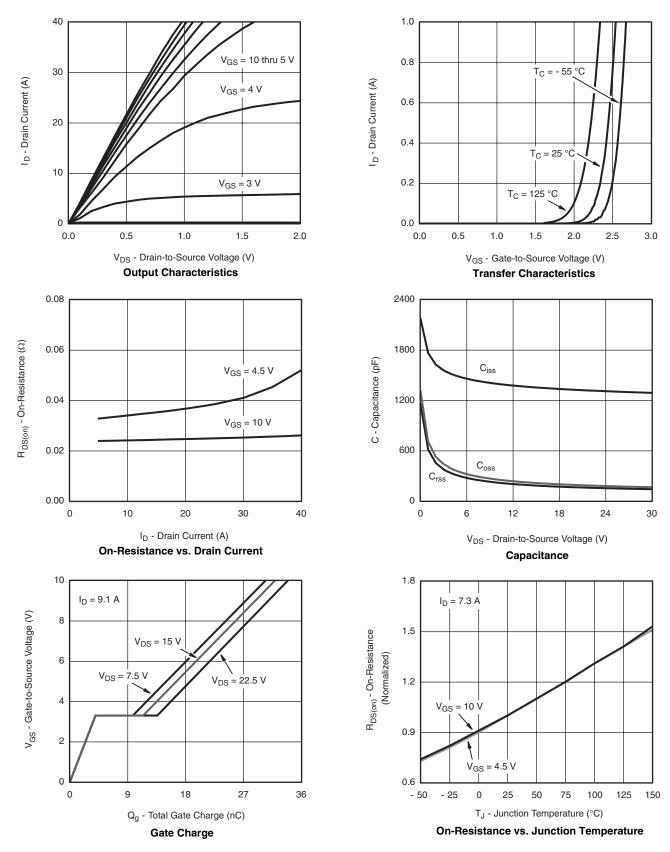
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





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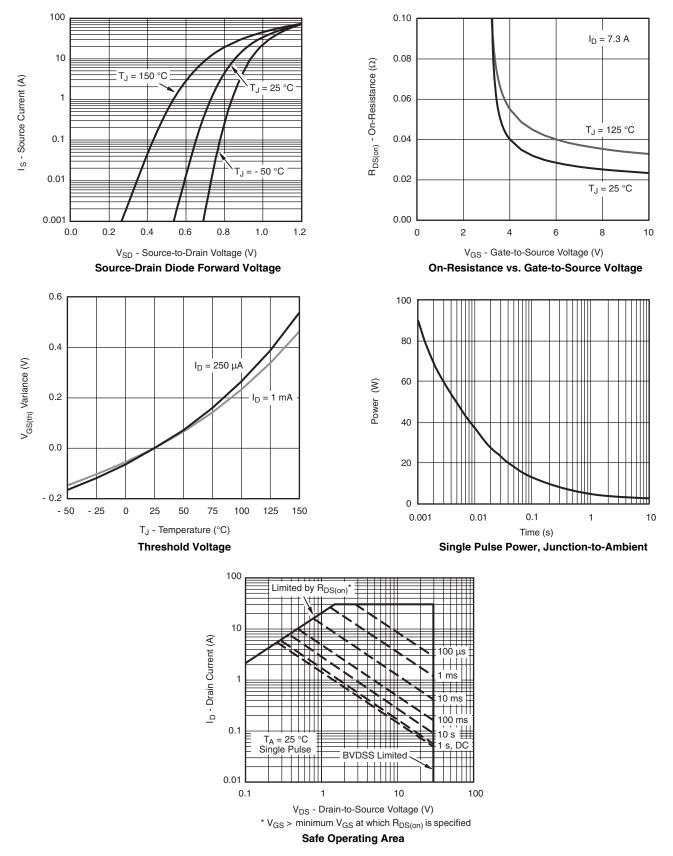


Document Number: 68969 S-82574-Rev. A, 27-Oct-08

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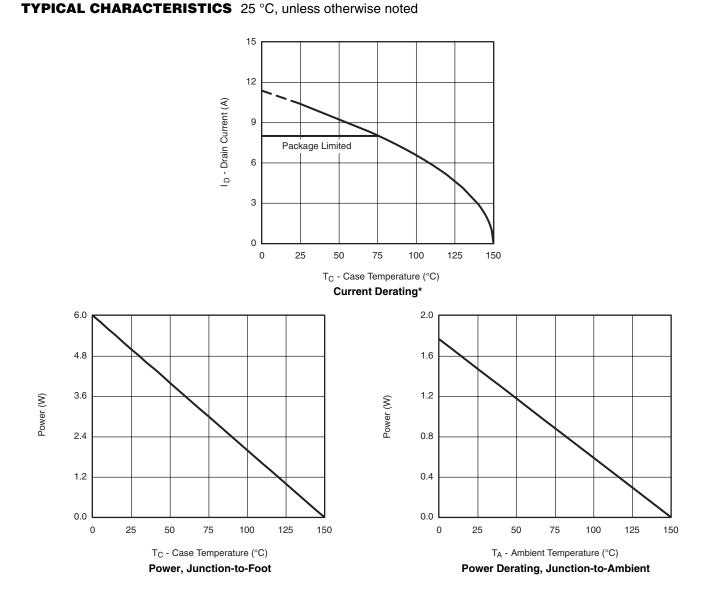


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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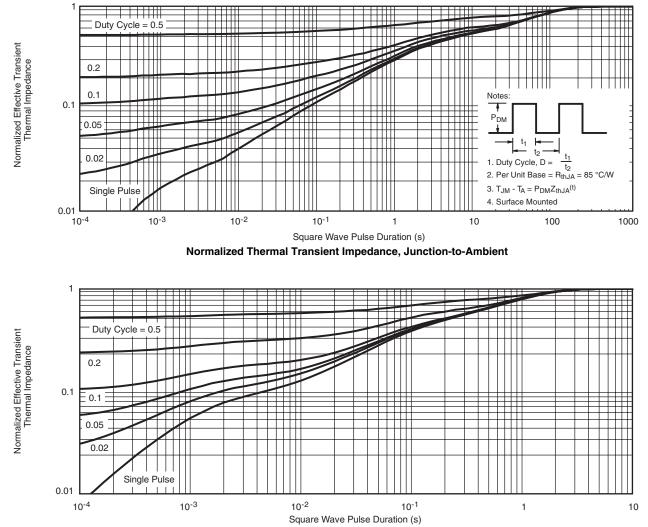


* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68969.



Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIMETERS		INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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1