Power MOSFET Failures in Automotive Applications

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There is no more demanding environment for power MOSFETs than automotive systems. As the components controlling the power for on-board electronics, MOSFETs in automotive systems are frequently used close to their electrical and thermal absolute maximum ratings in an effort to maximize power-to-weight ratios, i.e. to minimize material usage and minimize the physical volume of circuitry, in addition to cutting costs.

Design engineers have at their disposal sophisticated analysis tools to verify the adequacy of each component. Failure rates are extremely low, on the order of a few per million. The rarity of failure makes it extremely difficult to identify the cause of those failures that do occur. Collaborative efforts from both power MOSFET manufacturers and automotive design and manufacturing houses are required to reach successful solutions, and in many cases, proving the effectiveness of these solutions is extremely difficult due to the low failure rates involved.

Battery connect/disconnect switches implemented with power MOSFETs as a high-side switch (figure 1) are an example of circuits that experience a failure rate of a few parts per million. In this application, the drain of the MOSFET is permanently connected to the vehicle battery; the floating gate drive comes from a custom ASIC chip. The output voltage of the ASIC tracks the source potential and maintains the required gate drive voltage. However, the ASIC often has limited current sourcing capabilities. The source feeds into the other circuit controls; it also powers MOSFETs connected in parallel. In many cases, this load is inductive, with or without recirculation of its stored energy.

An understanding of the susceptibility of the MOSFET in this application requires studying the prime suspects, such as load dumping from a bad connection on the battery, the gate drive capabilities of the ASIC, and inductive surges from parallel connected loads on the source (the lower leg). Invariably, the results from circuit analysis are negative, with no clear root cause of device failure. This is not surprising since failures are so rare and measured in the low parts-per-million.

Failure analysis performed at MOSFET manufacturing facilities can provide further insights into the actual device failure mechanisms. Basic electrical tests can indicate gate-to-source, gate-to-drain, and drain-to-source leakages with low resistance values. Examples of systematic decapsulation of failed devices are shown in figures 2 to 7. It can be observed that failures occur in two areas of the MOSFET structure. One failure is from gate metal to drain poly and the other failure is from source metal to gate poly. The conclusion from the analysis is that some voltage transient occurs on the gate and leads to the failure.

Excluding the cases of obvious processing anomalies, investigations into the manufacturing processes have shown that these items are unlikely to be the cause of failure. The reasoning behind this conclusion takes into account the very low failure rates seen and fact that individual failures tend to occur across multiple wafer and assembly lots. Process investigation into the history of failed devices invariably shows that all critical parameters were well within the normal distribution, and corresponding final production test data were free from any objectionable deviations. At this point, every device is like every other device in all measurable ways.

For the root cause analysis, the key question is what kind of electrical transient could lead to such a failure? The failure is clearly caused after the device has completed the manufacturer's production testing, which significantly limits the possible causes of inducing failure. Device failure after this operation could be a result of handling or an actual application issue.

ESD testing to evaluate handling problems, followed by failure analysis, has not produced identical failure signatures. Similarly, application analysis and assembly level testing has yielded no clue to the definition of a critical electrical condition which reproduces the identical failure signature. In both of these cases (ESD and application evaluation), failures can be generated which involve similar structures as actual field failures, but the damage level seen in the in-house overstressing is higher than that generated from the field.

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ESD Investigation

Figures 8 to 11 are photos of device failures generated from high-voltage ESD pulses. These failures are generated from human body model and machine model stressing. (Charged device model stressing was tried, but device failure could not be achieved at the limits of our testing.) The machine model failures seem to more closely resemble the failures we have seen from the field, indicating that perhaps some type of exposure to this model may be a pre-requisite to the field returns.

Applications Investigation

Extensive bench testing at device level, within datasheet specifications, does not cause device failure. It helps confirm the fact that some voltage transient leads to such failures. However, the source and definition of the transient are unknown.

Different test setups used in attempts to duplicate the failure signature are:

(1) V_{GS} transient with drain-source shorted

(2) V_{DG} transient with gate-source shorted

(3) V_{GS} transient with drain open

The transient test pulse definition and the corresponding failure analysis are shown in figures 8 to 13. The transient with open drain, VGS = 100 V, and 150 µs duration produces a failure signature close to field failure. Compare figures 17 and 7.

Four more samples were tested to establish repeatability. Results are shown in figure 18 to 25. We can observe that repeatability can be established to the extent that the failure signature is similar. However, the failure location varies.

Conclusions

While in actual application tests it seems almost impossible to realize a VGS = 100 V, 150 µs pulse, the comparability of the signature confirms that a similar high-voltage transient does appear to create the failure. Although there is not a definite solution to the problem of these low-ppm failures, there are actions which can be taken to further reduce the potential for failure:

(1) The MOSFET manufacturer can increase the design margins while implementing improved techniques and new-generation materials. The attempt is to design and manufacture a more rugged part that can sustain such transients. These are long term solutions, requiring extensive evaluation and qualification.

(2) The application system design can increase the electrical design margins to decrease the probability of device-damaging transients reaching the power MOSFETs.

(3) The handling environments for devices can be re-evaluated to eliminate the potential for ESD damage (from equipment or humans).

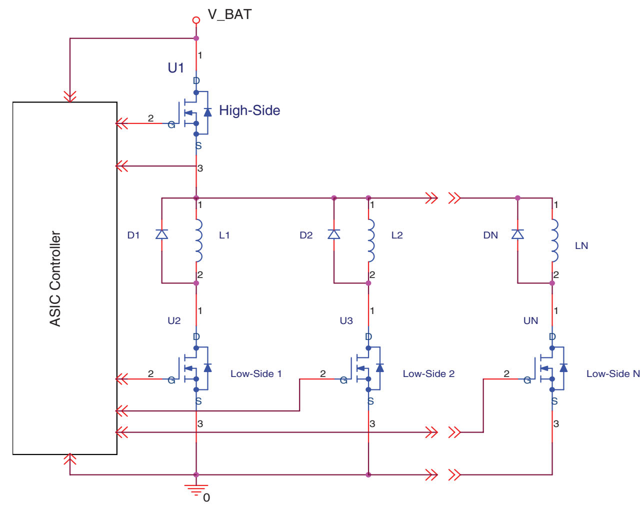

Fig. 1 - Power MOSFET in a Typical Battery Connect/Disconnect Application

Fig. 2 - Typical Failure Locations gate Metal to Drain Poly Short are located on the Periphery of the Device

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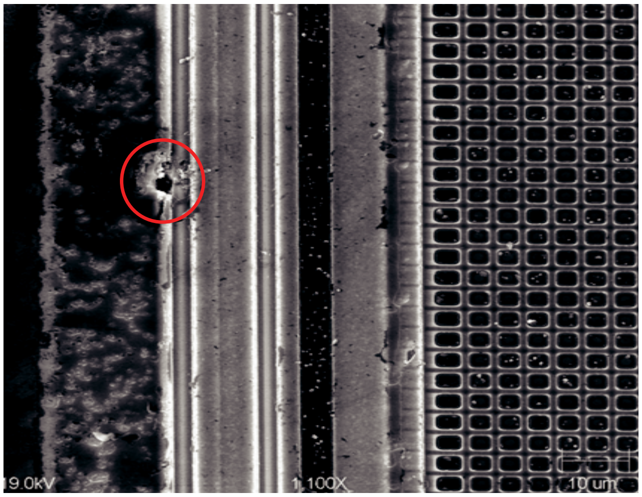

Fig. 3 - An Example of a Field return: Gate Metal to Drain Poly Short - Top View

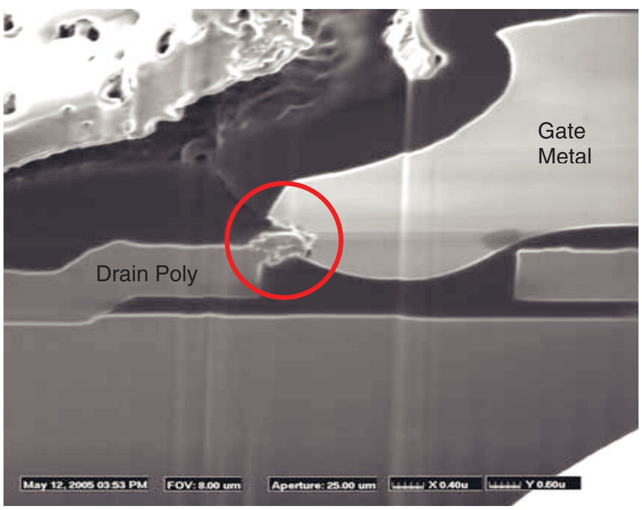

Fig. 4 - An Example of a Field return: Gate Metal to Drain Poly Short - X Section Short - Top View

Fig. 5 - Possible Failure Locations of Source Metal to Gate Poly Short

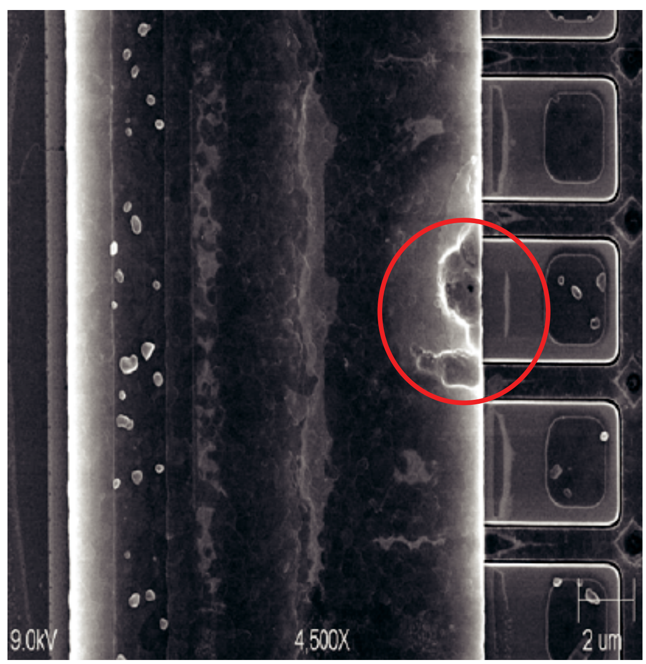

Fig. 6 - An Example of a Field return: Source Metal to Gate Poly Short - Top View

APPLICATION NOTE

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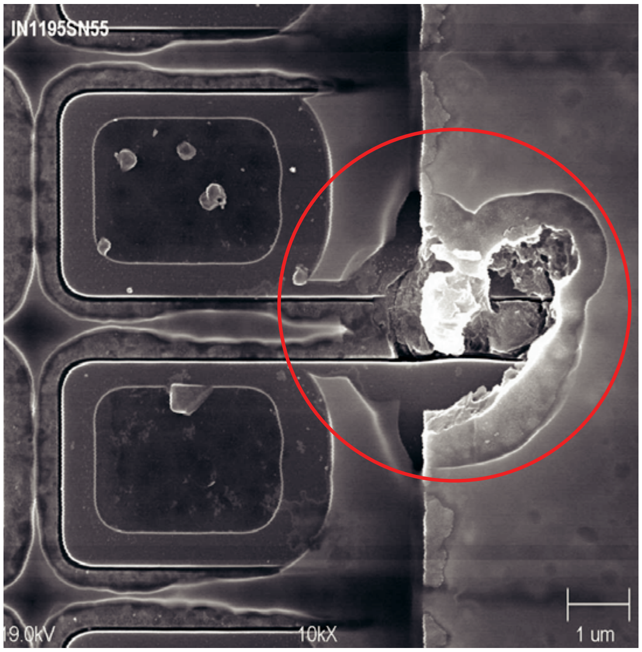

Fig. 7 - Another Example of a Field return: Source Metal to Gate Poly Short - Top View

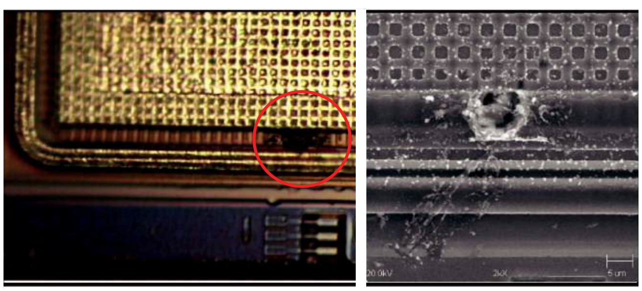

Fig. 8 - ESD Failure to Human Body Model. Gate/Drain/Source Short

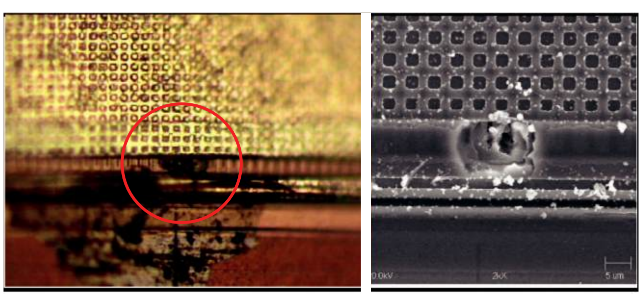

Fig. 9 - ESD Failure to Machine Model. Gate/Drain/Source Short

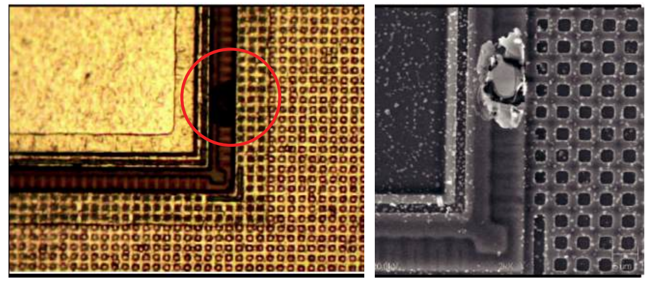

Fig. 10 - ESD Failure to Machine Model. Gate/Drain/Source Short

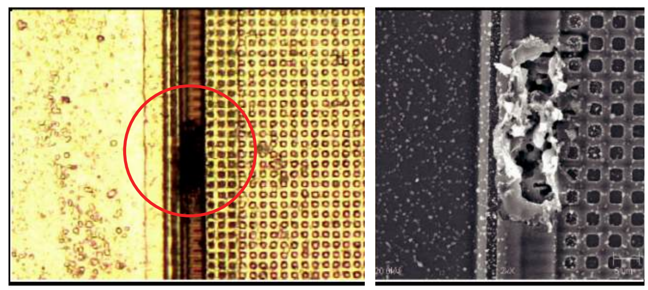

Fig. 11 - ESD Failure to Machine Model. Gate/Source Short

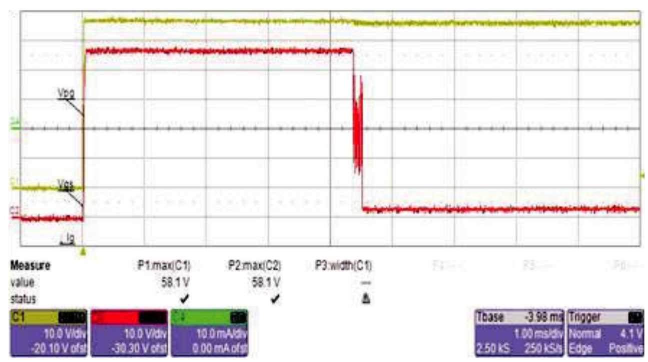

Fig. 12 - V_{GS} = 60 V, 4.5 ms

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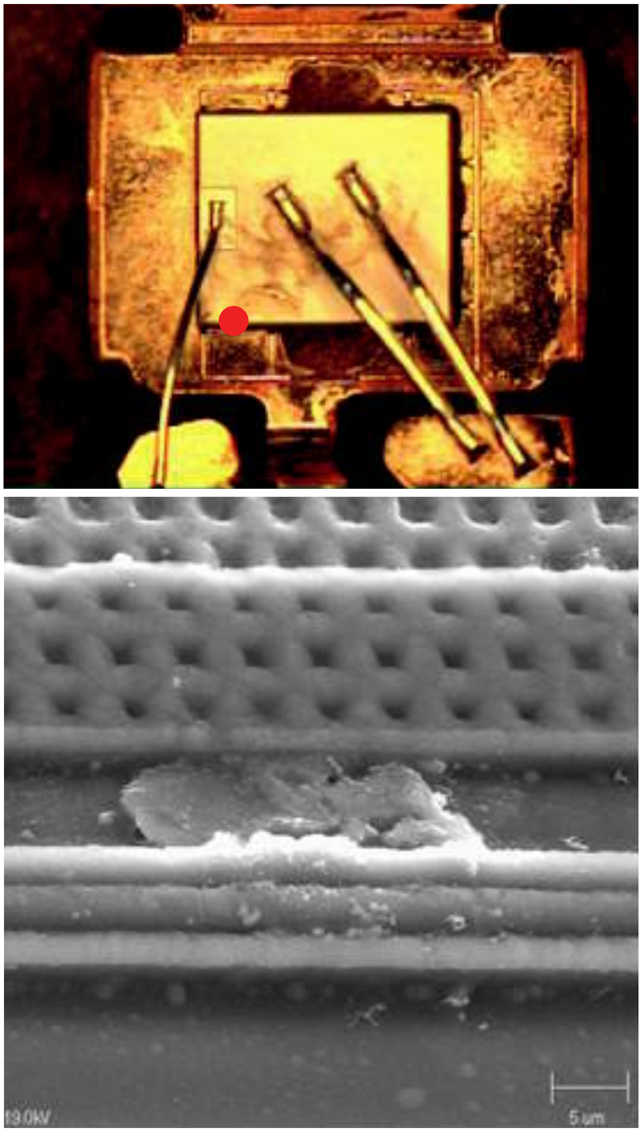

Fig. 13 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

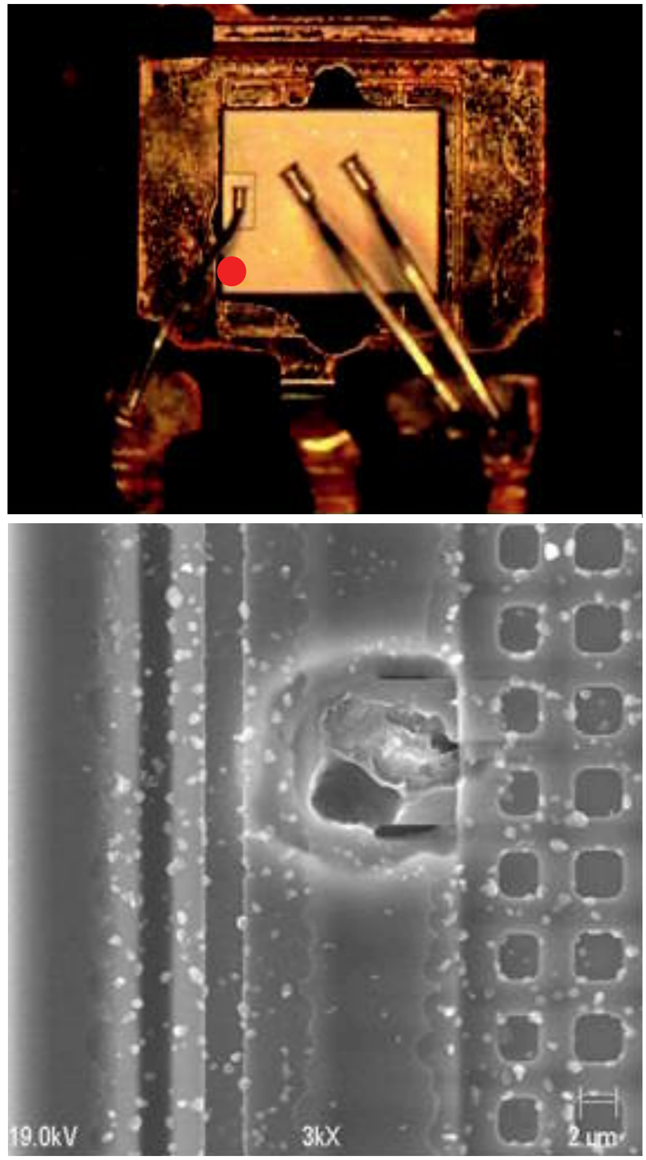

Fig. 15 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

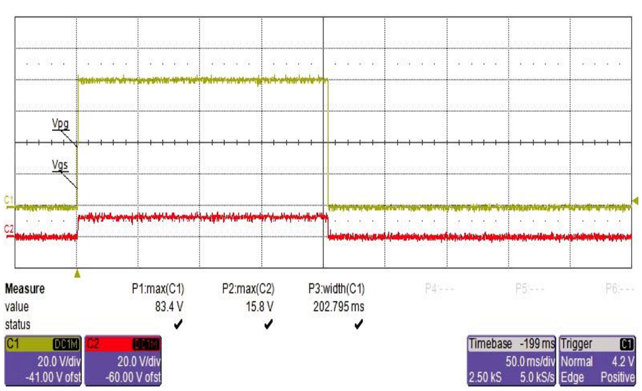

Fig. 14 - V_{DG} = 80 V, 200 ms

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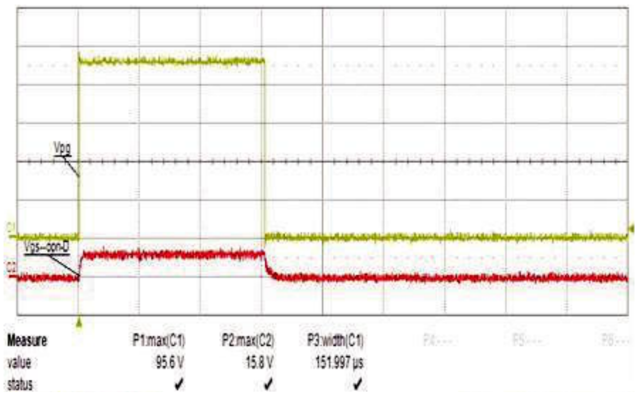

Fig. 16 - Open Drain, V_{GS} = 100 V, 150 µs

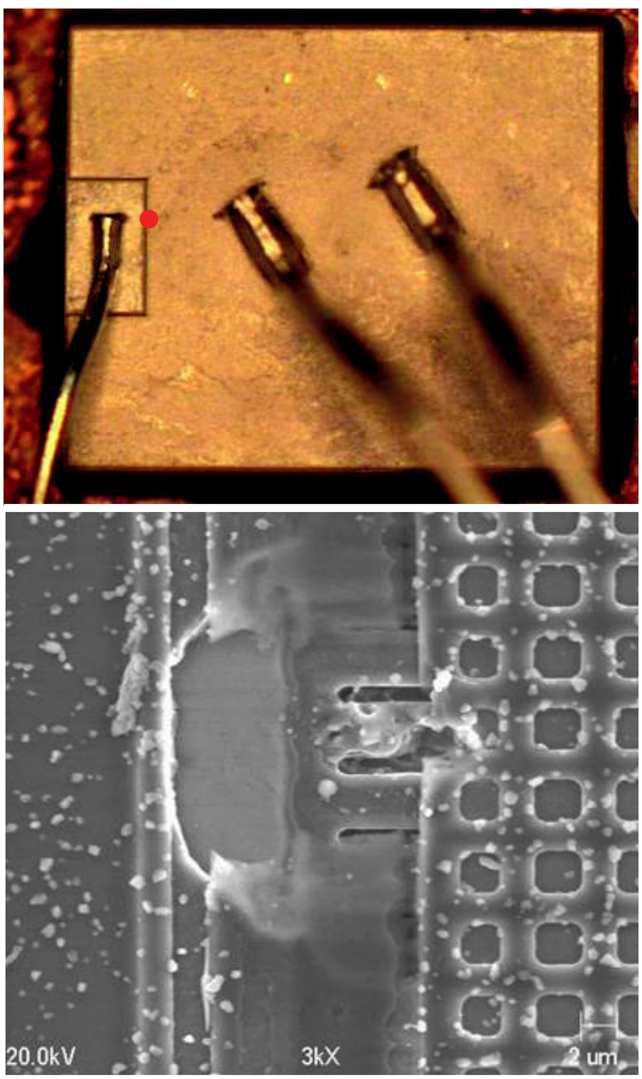

Fig. 17 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

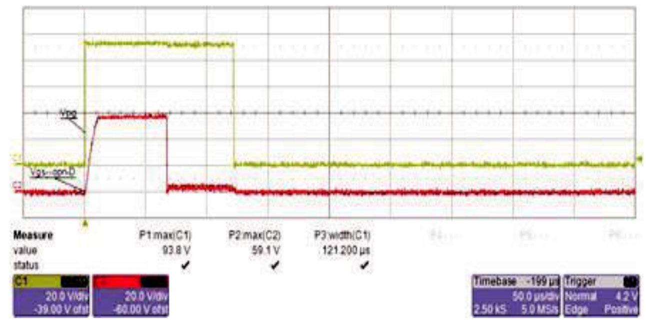

Fig. 18 - Open Drain, V_{GS} = 100 V, 120 µs

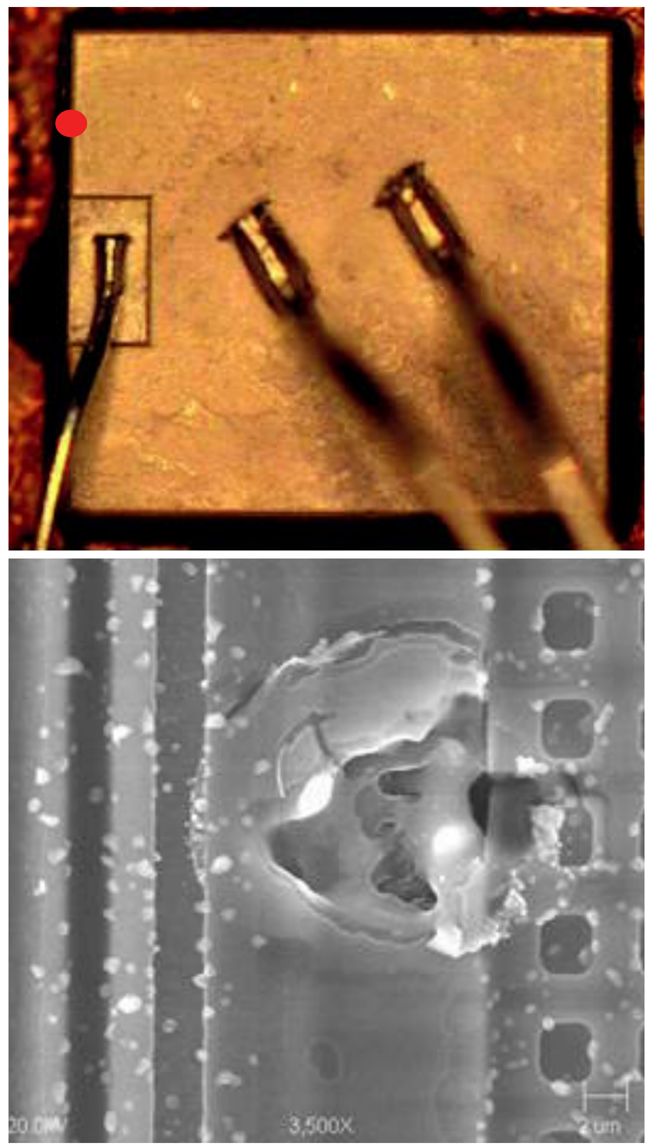

Fig. 19 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

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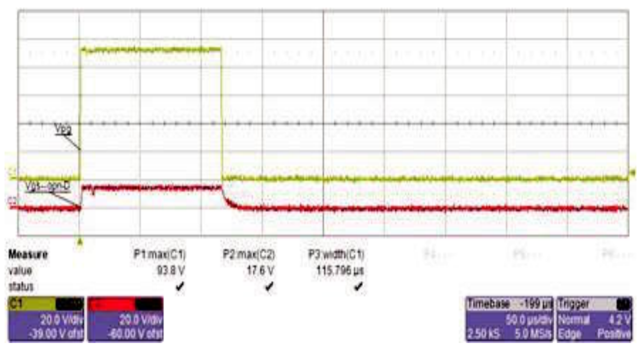

Fig. 20 - Open Drain, V_{GS} = 100 V, 115 µs

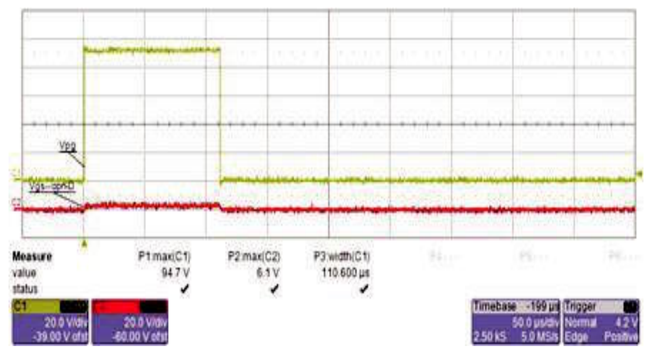

Fig. 22 - Open Drain, V_{GS} = 100 V, 110 µs

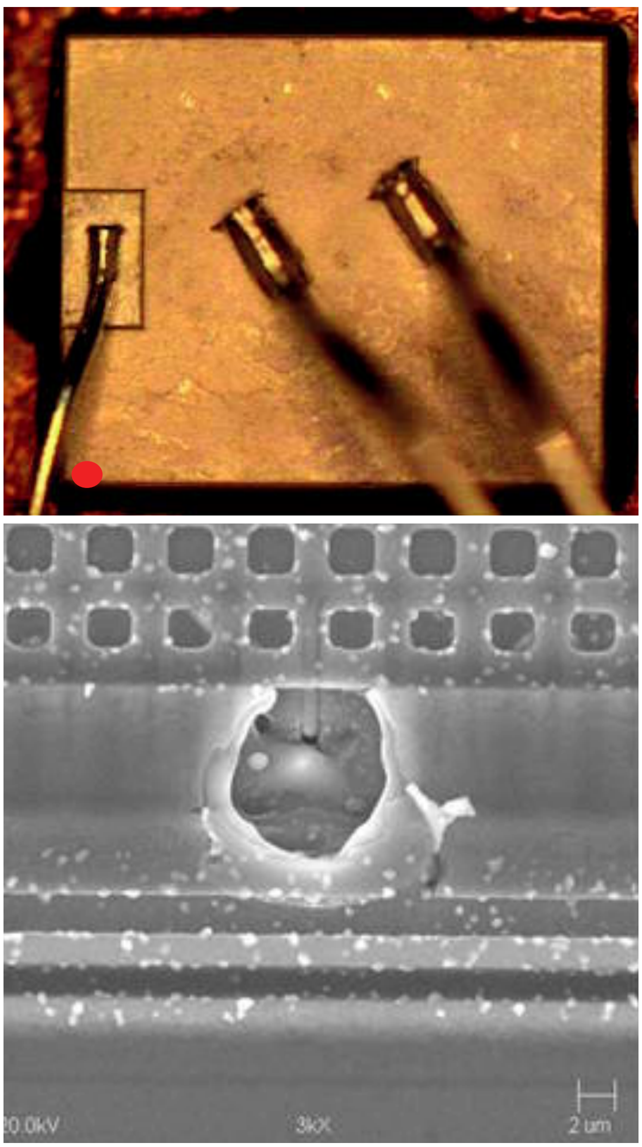

Fig. 21 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

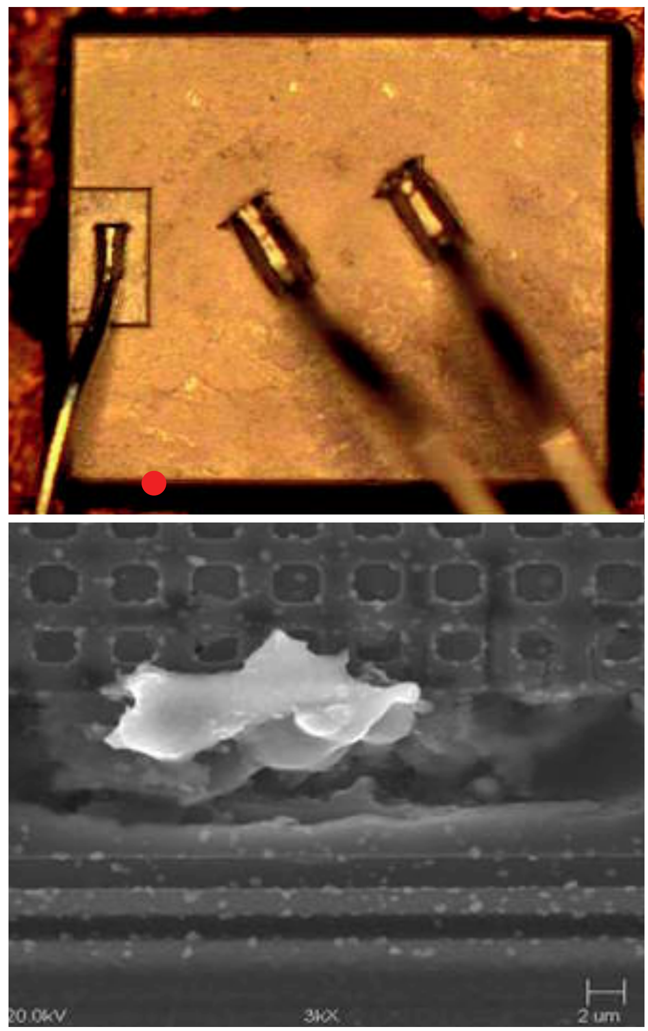

Fig. 23 - Severe burn mark caused by gate oxide rupture at trench poly to poly bus intercept

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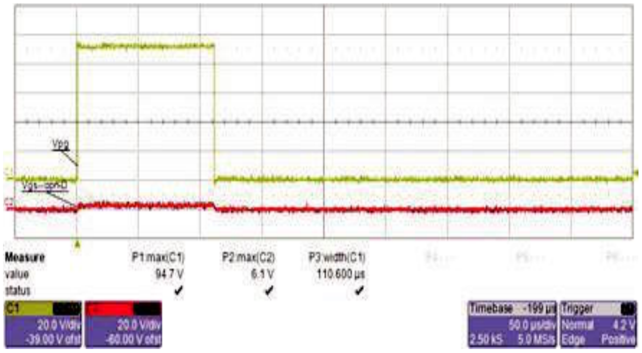

Fig. 24 - Open Drain, V_{GS} = 100 V, 110 µs

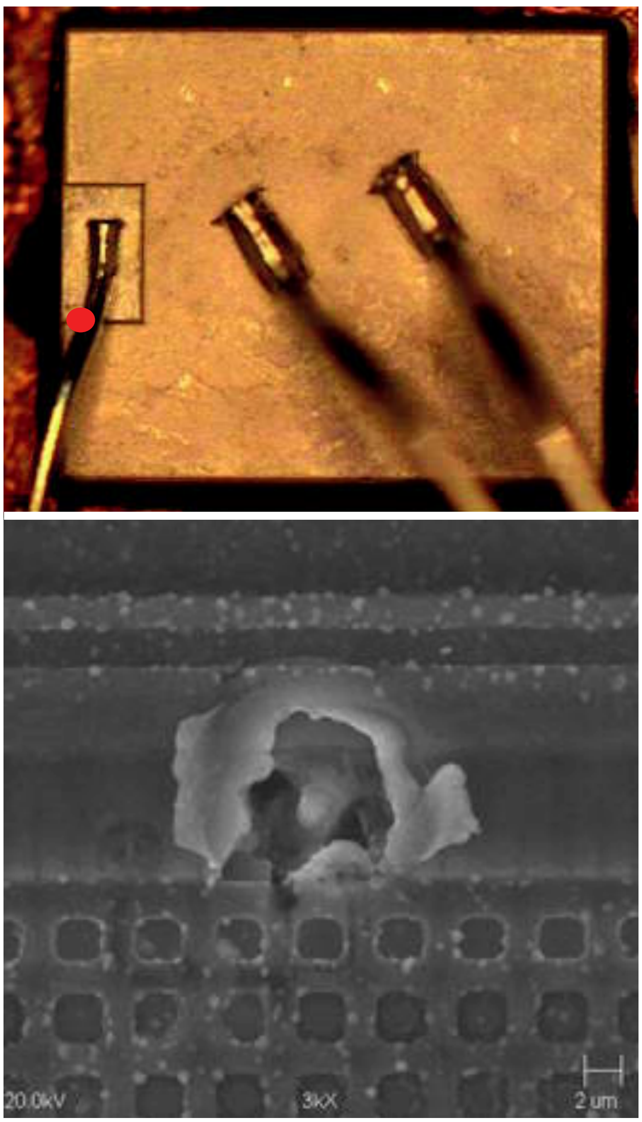

Fig. 25 - Severe burn Mark caused by Gate Oxide Rupture at Trench Poly to Poly Bus Intercept

APPLICATION NOTE