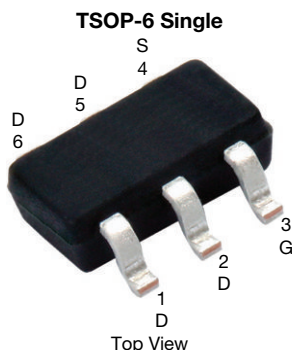


# N-Channel 60-V (D-S) MOSFET



Marking code: AN

PRODUCT SUMMARY	
$V_{DS}$ (V)	60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.100
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.128
$Q_g$ typ. (nC)	3.5
$I_D$ (A)	4.1
Configuration	Single

## FEATURES

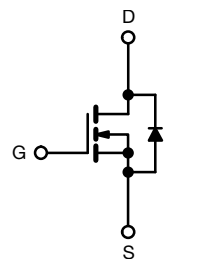
- TrenchFET® power MOSFET
- 100 %  $R_g$  tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## APPLICATIONS

- Load switch for portable applications
- LED backlight switch
- DC/DC converter



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



N-Channel MOSFET

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3458BDV-T1-E3
Lead (Pb)-free and halogen-free	Si3458BDV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	60	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	4.1	A
	$T_C = 70$ °C		3.2	
	$T_A = 25$ °C		3.2 a, b	
	$T_A = 70$ °C		2.5 a, b	
Pulsed drain current		$I_{DM}$	10	A
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	2.9	
	$T_A = 25$ °C		1.7 a, b	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	3.3	W
	$T_C = 70$ °C		2.1	
	$T_A = 25$ °C		2 a, b	
	$T_A = 70$ °C		1.3 a, b	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature)			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, c	$t \leq 5$ s	$R_{thJA}$	53	62.5	°C/W
Maximum junction-to-foot (drain)	Steady state	$R_{thJF}$	32	38	

## Notes

- Surface Mounted on 1" x 1" FR4 board
- $t = 5$  s
- Maximum under steady state conditions is 110 °C/W
- Based on  $T_C = 25$  °C



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	-	60	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	-6	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	-	3	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	10	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	10	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A	-	0.082	0.100	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.8 A	-	0.105	0.128	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.2 A	-	12	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	350	-	pF
Output capacitance	C <sub>oss</sub>		-	40	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	20	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A	-	7.1	11	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.2 A	-	3.5	5.5	
Gate-drain charge	Q <sub>gd</sub>		-	1.1	-	
			-	0.95	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	-	2.3	3.5	Ω
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 12 Ω I <sub>D</sub> ≅ 2.5 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	-	16	25	ns
Rise Ttime	t <sub>r</sub>		-	17	30	
Turn-off delay time	t <sub>d(off)</sub>		-	12	20	
Fall time	t <sub>f</sub>		-	10	15	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 12 Ω I <sub>D</sub> ≅ 2.5 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	5	10	
Rise time	t <sub>r</sub>		-	12	20	
Turn-off delay time	t <sub>d(off)</sub>		-	18	30	
Fall time	t <sub>f</sub>		-	10	15	
Drain-source body diode characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	2.9	A
Pulse diode forward current	I <sub>SM</sub>		-	-	10	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.5 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 2.5 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	25	50	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	40	80	nC
Reverse recovery fall time	t <sub>a</sub>		-	22	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	3	-	

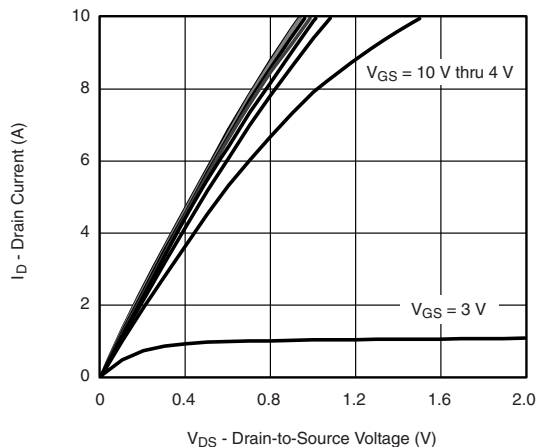
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

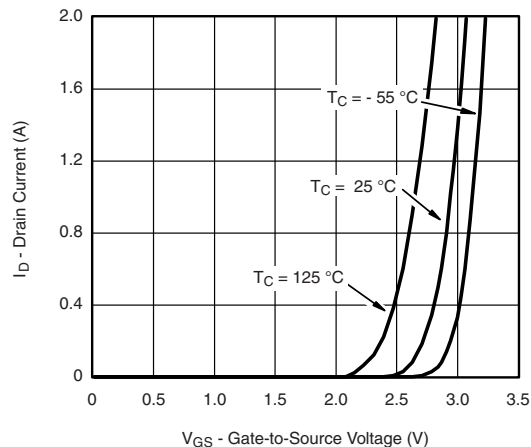
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



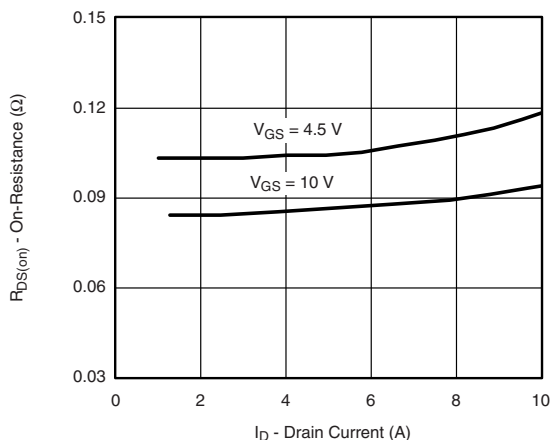
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



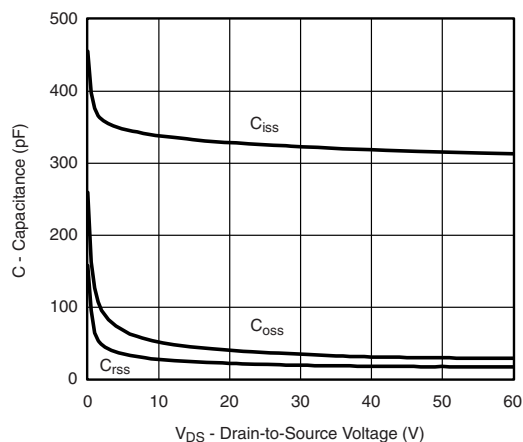
**Output Characteristics**



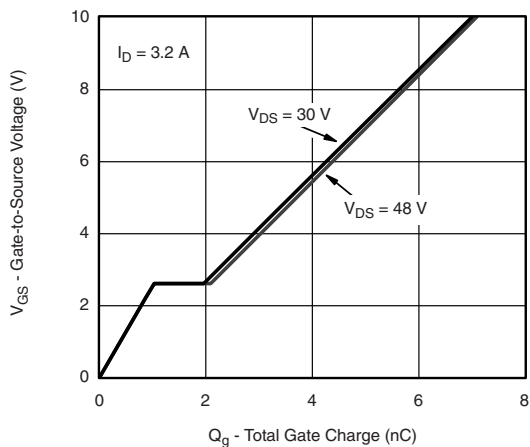
**Transfer Characteristics**



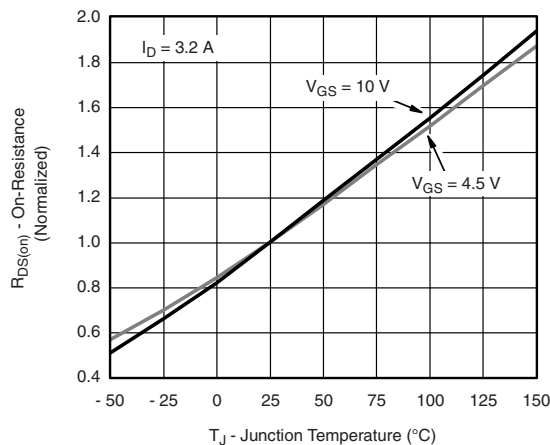
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



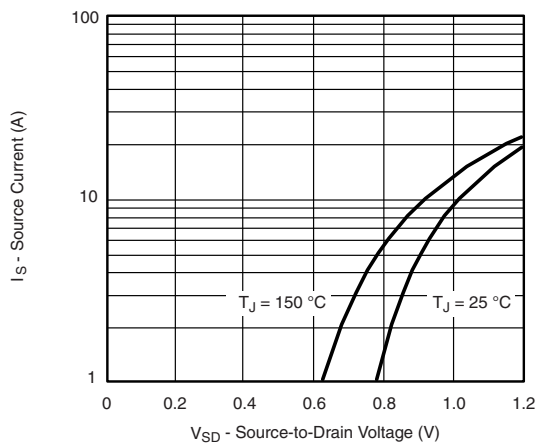
**Gate Charge**



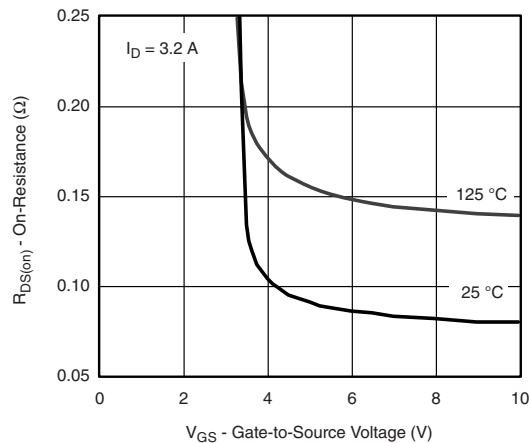
**On-Resistance vs. Junction Temperature**



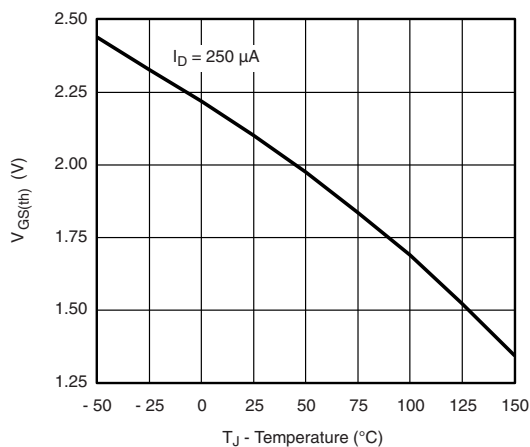
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



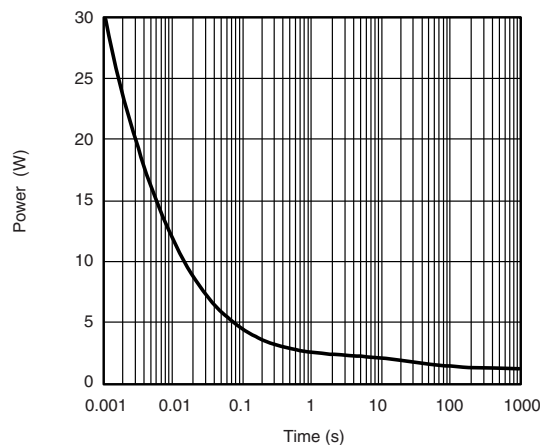
**Source-Drain Diode Forward Voltage**



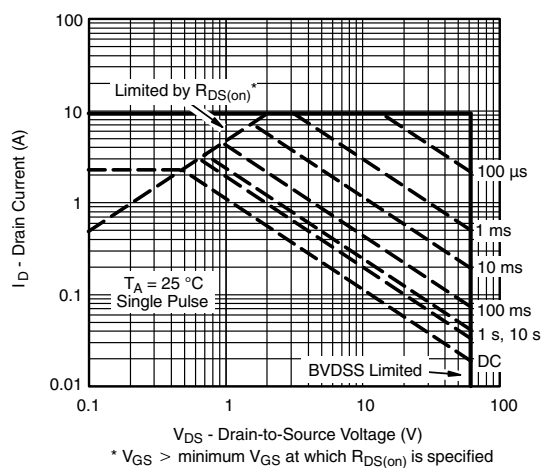
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



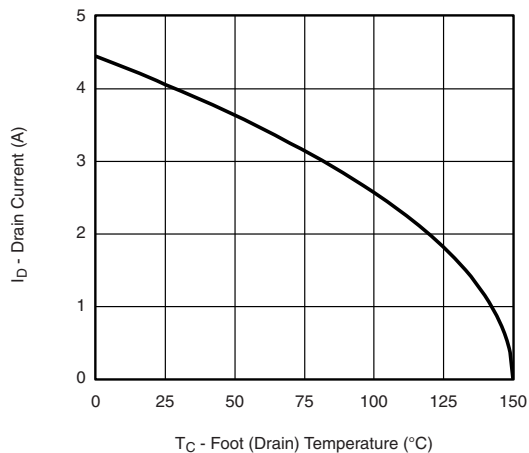
**Single Pulse Power (Junction-to-Ambient)**



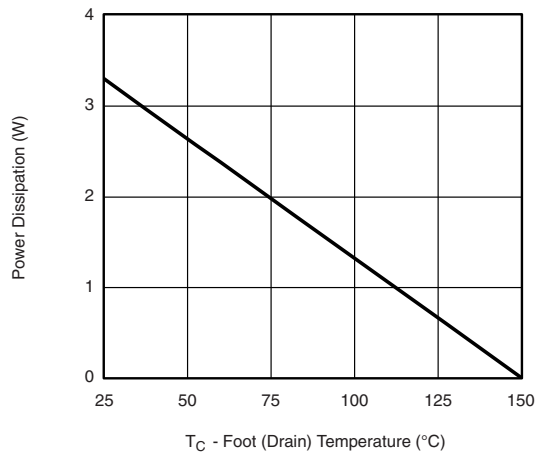
**Safe Operating Area, Junction-to-Ambient**



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



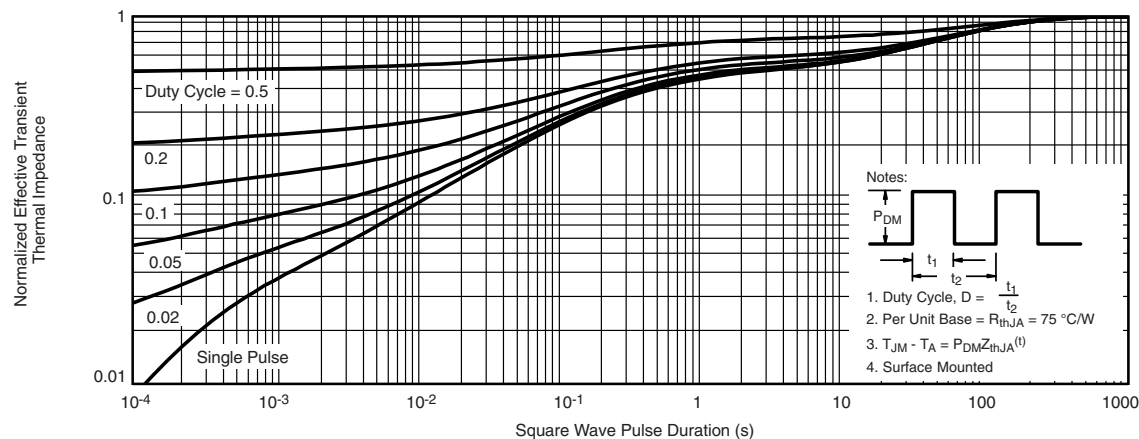
**Power Derating**

**Note**

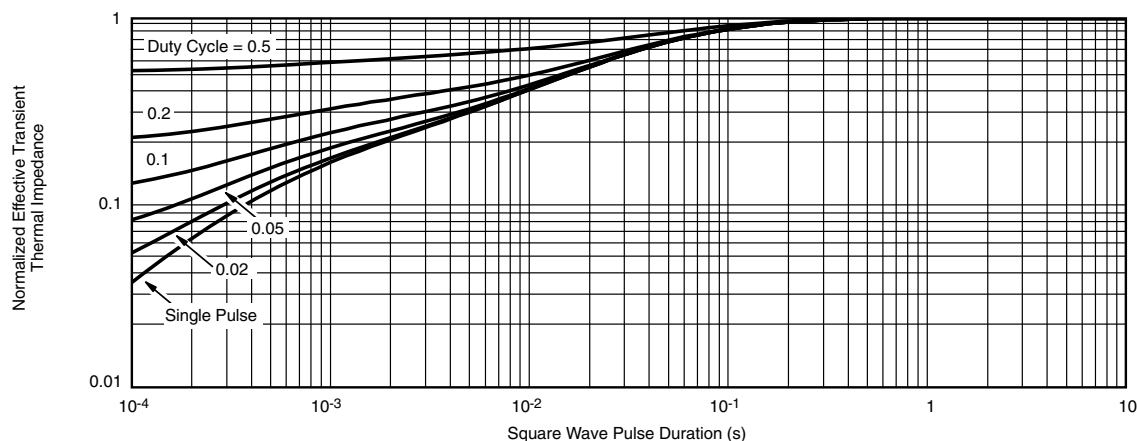
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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## TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C



5-LEAD TSOP



6-LEAD TSOP



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A <sub>1</sub>	0.01	-	0.10	0.0004	-	0.004
A <sub>2</sub>	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e <sub>1</sub>	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L <sub>1</sub>	0.60 Ref			0.024 Ref		
L <sub>2</sub>	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ <sub>1</sub>	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

## Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


**Note**

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022  
DWG: 3010





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