0.5 pC Charge Injection, 100 pA Leakage, Dual SPDT Analog Switch

DESCRIPTION

The DG636 is an analog CMOS, dual SPDT switch, designed to operate from a +2.7 V to +12 V single supply or from ± 2.7 V to ± 5 V, dual supplies. The DG636 is fully specified at +3 V, +5 V and ± 5 V. All control logic inputs have guaranteed 2 V logic high limits when operating from +5 V or ± 5 V supplies and 1.4 V when operating from a 3 V supply.

The DG636 switches conduct equally well in both directions and offer rail to rail analog signal handling. < 1 pC low charge injection, coupled with very low switch capacitance and leakage current makes this product ideal for use in precision instrumentation applications. Operating temperature range is specified from -40 °C to +125 °C. The DG636 is available in 14 lead TSSOP and the space saving 1.8 mm x 2.6 mm miniQFN package.

FEATURES

- Ultra low charge injection (± 0.5 pC, typ. over the full analog signal range)
- Leakage current < 0.5 nA max. at 85 °C (for DG636EQ-T1-E3)
- Low switch capacitance (C_{soff}, 2 pF typ.)
- Low $R_{DS(on)}$ - 115 Ω max.
- Fully specified with single supply operation at 3 V, 5 V and dual supplies at ± 5 V
- Low voltage, 2.5 V CMOS/TTL compatible
- 600 MHz, - 3 dB bandwidth
- Excellent isolation and crosstalk performance (typ. > -60 dB at 10 MHz)
- Fully specified from -40 °C to +85 °C and -40 °C to +125 °C
- 14 pin TSSOP and 16 pin miniQFN package (1.8 mm x 2.6 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

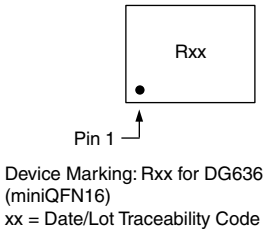
Pb-free

RoHS COMPLIANT

APPLICATIONS

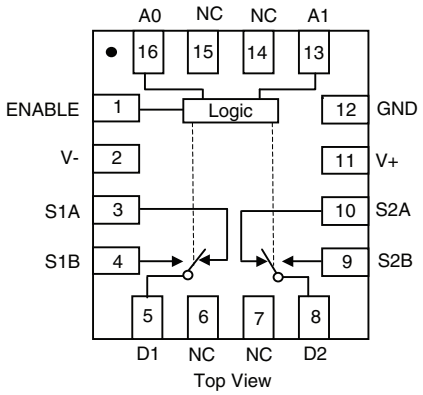
- High-end data acquisition
- Medical instruments
- Precision instruments
- High speed communications applications
- Automated test equipment
- Sample and hold applications

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



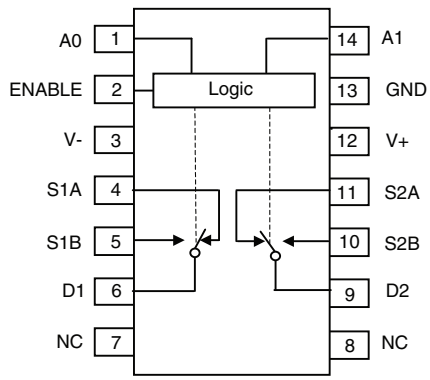
Device Marking: Rxx for DG636 (miniQFN16)
xx = Date/Lot Traceability Code

DG636 mQFN-16



Top View

DG636 TSSOP14



Top View

ENABLE = Hi, all switches are controlled by addr pins. ENABLE = Lo, all switches are off.

TRUTH TABLE

ENABLE INPUT	SELECTED INPUT		ON SWITCHES
	A1	A0	DG636
L	X	X	All Switches Open
H	L	L	D1 to S1A, D2 to S2A
H	L	H	D1 to S1B, D2 to S2A
H	H	L	D1 to S1A, D2 to S2B
H	H	H	D1 to S1B, D2 to S2B

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +125 °C [a]	14 pin TSSOP	DG636EQ-T1-E3
	16 pin miniQFN	DG636EN-T1-E4

Note

a. -40 °C to +85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+ to V-		14	V
GND to V-		7	
Digital Inputs [a], V_S, V_D		(V-) -0.3 to (V+) +0.3 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)		30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % Duty Cycle)		100	
Storage Temperature		-65 to +150	°C
Power Dissipation (Package) [b]	14 pin TSSOP [c]	450	mW
	16 pin miniQFN [d, e]	525	
Thermal Resistance (Package) [b]	14 pin TSSOP	178	°C/W
	16 pin miniQFN	152	

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 5.6 mW/°C above 70 °C.
d. Derate 6.6 mW/°C above 70 °C.
e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS FOR DUAL SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = -5 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	-5	5	-5	5	V
On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	70	-	115	-	115	Ω
			Full	-	-	160	-	140	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = ± 3 V	Room	1	-	5	-	5	
			Full	-	-	6.5	-	6.5	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	10	-	20	-	20	
			Full	-	-	33	-	22	
Analog Signal Range [e]	V_{ANALOG}		Full	-	-5	5	-5	5	V
On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	70	-	115	-	115	Ω
			Full	-	-	160	-	140	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = ± 3 V	Room	1	-	5	-	5	
			Full	-	-	6.5	-	6.5	
On-Resistance Flatness	$R_{FLATNESS}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	10	-	20	-	20	
			Full	-	-	33	-	22	
Switch Off Leakage Current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = ± 4.5 V, V_S = ∓ 4.5 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Channel On Leakage Current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_S = V_D = ± 4.5 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = ± 4.5 V, V_S = ∓ 4.5 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Channel On Leakage Current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_S = V_D = ± 4.5 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 0.8 V	Full	0.005	-0.1	0.1	-0.1	0.1	µA
Input Current, V_{IN} High	I_{IH}	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 2 V	Full	0.005	-0.1	0.1	-0.1	0.1	
Input Capacitance [e]	C_{IN}	f = 1 MHz	Room	3.4	-	-	-	-	pF

SPECIFICATIONS FOR DUAL SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = -5 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP.[b]	TYP.[c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN.[d]	MAX.[d]	MIN.[d]	MAX.[d]	
Dynamic Characteristics									
Transition Time	t_{trans}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	20	-	70	-	70	ns
			Full	-	-	105	-	80	
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 3 V	Room	16	-	60	-	60	
			Full	-	-	90	-	65	
Turn-Off Time	t_{OFF}		Room	15	-	52	-	52	
			Full	-	-	76	-	56	
Break-Before-Make Time Delay	t_D	V_S = 3 V R_L = 300 Ω, C_L = 35 pF	Room	15	-	-	-	-	
			Full	-	5	-	5	-	
Charge Injection [e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	0.1	-	-	-	-	pC
Off Isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-58	-	-	-	-	dB
Bandwidth [e]	BW	R_L = 50 Ω	Room	610	-	-	-	-	MHz
Channel-to-Channel Crosstalk [e]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-88	-	-	-	-	dB
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	2.1	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	4.2	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	11.3	-	-	-	-	
Total Harmonic Distortion [e]	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω	Room	0.01	-	-	-	-	%
Power Supplies									
Power Supply Current	I+	V_{IN} = 0 V, or V+	Room	0.001	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative Supply Current	I-		Room	-0.001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	
Ground Current	I_{GND}		Room	-0.001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

SPECIFICATIONS FOR SINGLE SUPPLY

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = 0 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP.[b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	-	5	-	5	V
On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = +3.5 V	Room	120	-	170	-	170	Ω
			Full	-	-	250	-	200	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = +3.5 V	Room	3	-	5	-	5	
			Full	-	-	12	-	10	
Switch Off Leakage Current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 1 V/4.5 V, V_S = 4.5 V/1 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Channel On Leakage Current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V V_S = V_D = 1 V/4.5 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 1 V/4.5 V, V_S = 4.5 V/1 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Channel On Leakage Current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V, V_S = V_D = 1 V/4.5 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input Current, V_{IN} Low	I_L	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 0.8 V	Full	0.005	-0.1	0.1	-0.1	0.1	µA
Input Current, V_{IN} High	I_H	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 2 V	Full	0.005	-0.1	0.1	-0.1	0.1	
Input Capacitance	C_{IN}	f = 1 MHz	Room	4.3	-	-	-	-	pF
Dynamic Characteristics									
Transition Time	t_{TRANS}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	36	-	75	-	75	ns
			Full	-	-	120	-	95	
Enable Turn-On Time	$t_{ON(EN)}$		Room	30	-	70	-	70	
			Full	-	-	102	-	80	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	17	-	47	-	47	
			Full	-	-	88	-	63	
Break-Before-Make-Time	t_{BMM}		Room	23	-	-	-	-	
			Full	-	5	-	5	-	
Charge Injection	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	0.1	-	-	-	-	pC
Off-Isolation [e]	OIRR	f = 10 MHz, R_L = 50 Ω, C_L = 5 pF	Room	-58	-	-	-	-	dB
Crosstalk [e]	X_{TALK}		Room	-81	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω	Room	520	-	-	-	-	MHz
Total Harmonic Distortion	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω	Room	0.009	-	-	-	-	%
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	2.5	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$			6.4	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$			11.3	-	-	-	-	

SPECIFICATIONS FOR SINGLE SUPPLY

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, V- = 0 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 2 V, 0.8 V [a]	TEMP.[b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Power Supplies									
Power Supply Current	I+	V_{IN} = 0 V, or V+	Room	0.001	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative Supply Current	I-		Room	-0.001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	
Ground Current	I_{GND}		Room	-0.001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

SPECIFICATIONS FOR SINGLE SUPPLY

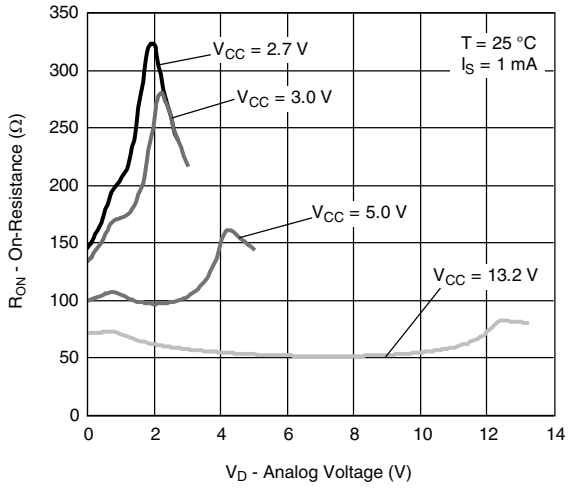
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V- = 0 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 1.4 V, 0.6 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	-	3	-	3	V
On-Resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = +1.5 V	Room	200	-	245	-	245	Ω
			Full	-	-	325	-	290	
On-Resistance Match	ΔR_{ON}	I_S = 1 mA, V_D = +1.5 V	Room	5	-	6	-	11	
			Full	-	-	13	-	6	
Switch Off Leakage Current (for 14 pin TSSOP)	$I_{S(off)}$	V+ = 3 V, V- = 0 V V_D = 1 V/3 V, V_S = 3 V/1 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	nA
			Full	-	-18	18	-0.5	0.5	
	$I_{D(off)}$		Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Channel On Leakage Current (for 14 pin TSSOP)	$I_{D(on)}$	V+ = 3 V, V- = 0 V V_S = V_D = 1 V/3 V	Room	± 0.01	-0.1	0.1	-0.1	0.1	
			Full	-	-18	18	-0.5	0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 1 V/3 V, V_S = 3 V/1 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
	$I_{D(off)}$		Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Channel On Leakage Current (for 16 pin miniQFN)	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V, V_S = V_D = 1 V/3 V	Room	± 0.01	-1	1	-1	1	
			Full	-	-18	18	-2	2	
Digital Control									
Input Current, V_{IN} Low	I_L	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 0.6 V	Full	0.005	-1	1	-1	1	µA
Input Current, V_{IN} High	I_H	$V_{IN\ A0,\ A1\ and\ ENABLE}$ Under test = 1.4 V	Full	0.005	-1	1	-1	1	
Input Capacitance	C_{IN}	f = 1 MHz	Room	4.3	-	-	-	-	pF

SPECIFICATIONS FOR SINGLE SUPPLY

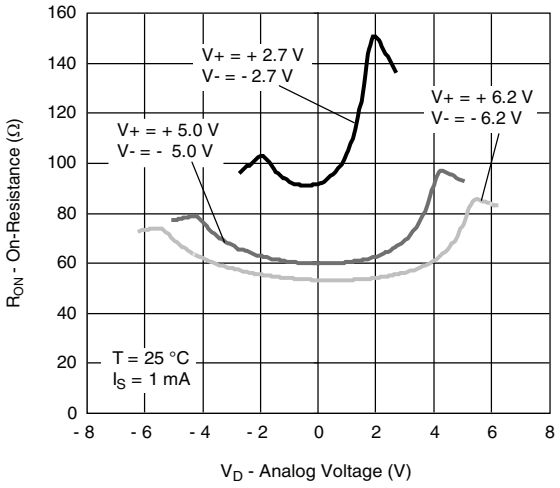
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, V- = 0 V $V_{IN\ A0,\ A1\ AND\ ENABLE}$ = 1.4 V, 0.6 V [a]	TEMP. [b]	TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Dynamic Characteristics									
Transition Time	t_{TRANS}	$V_{S(CLOSE)}$ = 3 V, $V_{S(OPEN)}$ = 0 V, R_L = 300 Ω, C_L = 35 pF	Room	95	-	130	-	130	ns
			Full	-	-	190	-	160	
Enable Turn-On Time	$t_{ON(EN)}$		Room	77	-	108	-	108	
			Full	-	-	161	-	131	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	35	-	76	-	76	
			Full	-	-	112	-	88	
Break-Before-Make-Time	t_{BMM}		Room	45	-	-	-	-	
			Full	-	5	-	5	-	
Charge Injection	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Full	0.24	-	-	-	-	pC
Off-Isolation [e]	OIRR	f = 10 MHz, R_L = 50 Ω, C_L = 5 pF	Room	-57	-	-	-	-	dB
Crosstalk [e]	X_{TALK}		Room	-93	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω	Room	442	-	-	-	-	MHz
Total Harmonic Distortion	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω	Room	0.09	-	-	-	-	%
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz	Room	2.5	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$		Room	6.4	-	-	-	-	
Channel On Capacitance [e]	$C_{D(on)}$		Room	11.7	-	-	-	-	
Power Supplies									
Power Supply Current	I+	VIN = 0 V, or V+	Room	0.001	-	0.5	-	0.5	µA
			Full	-	-	1	-	1	
Negative Supply Current	I-		Room	-0.001	-0.5		-0.5		
			Full	-	-1	-	-1	-	
Ground Current	IGND		Room	-0.001	-0.5	-	-0.5	-	
			Full	-	-1	-	-1	-	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

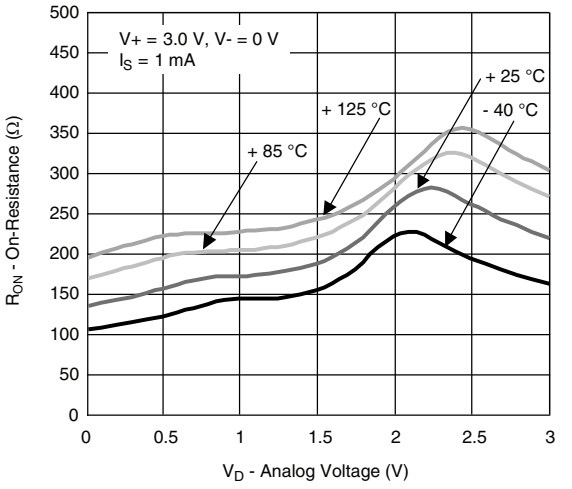
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



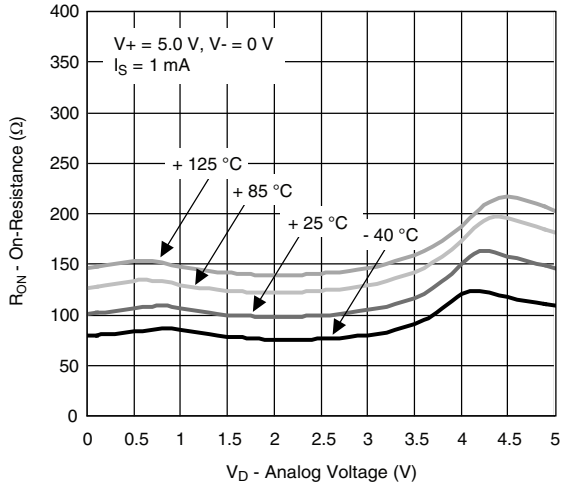
On-Resistance vs. V_D (Single Supply Voltage)



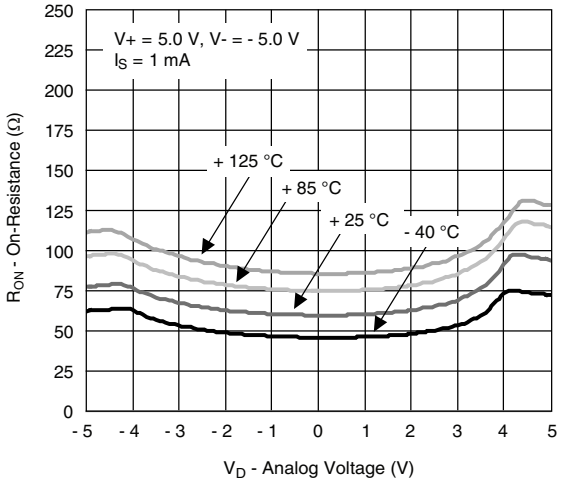
On-Resistance vs. V_D (Dual Supply Voltage)



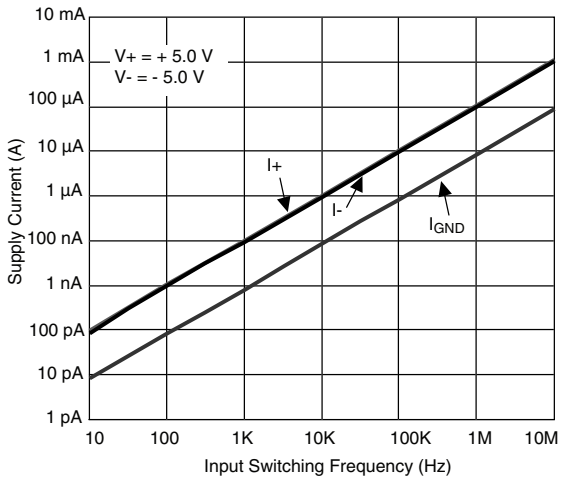
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

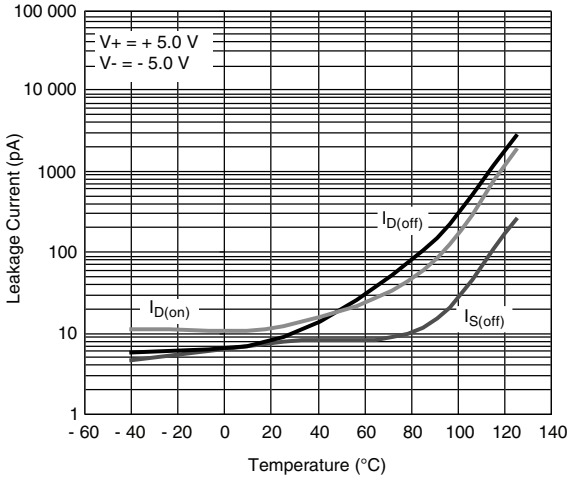


On-Resistance vs. Analog Voltage and Temperature

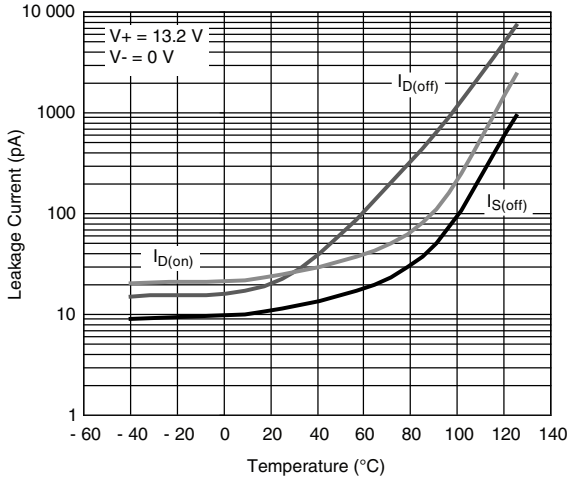


Supply Current vs. Input Switching Frequency

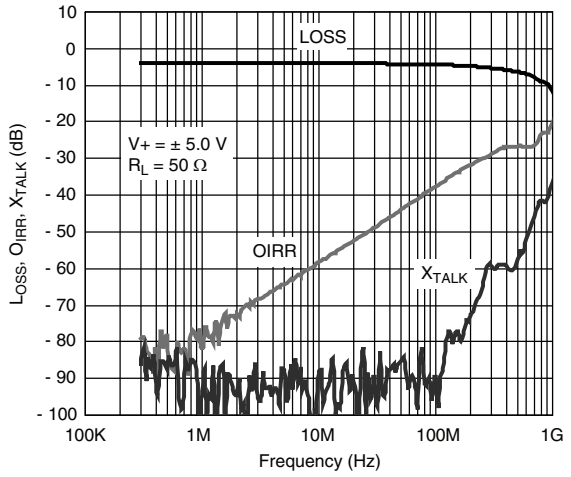
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



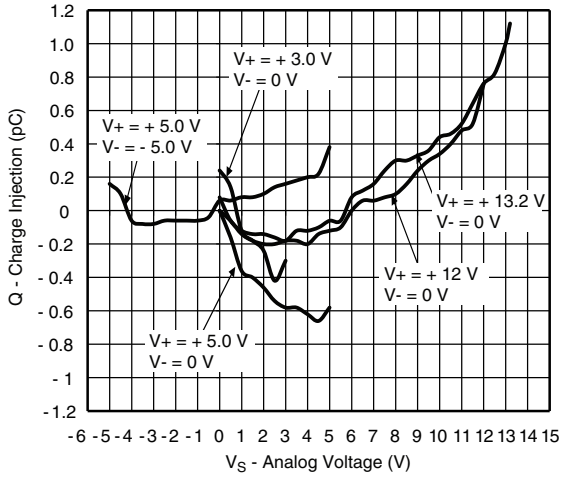
Leakage Current vs. Temperature



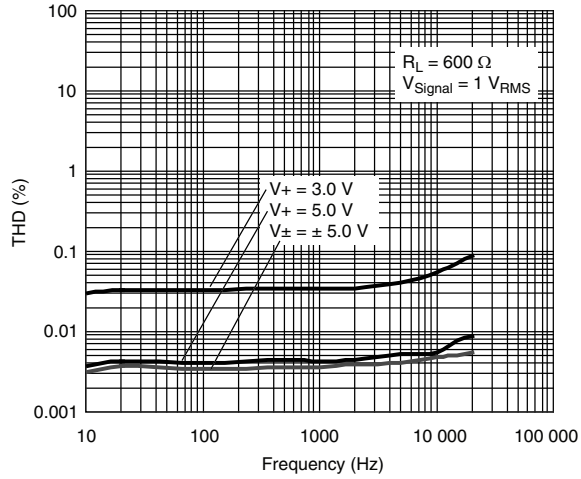
Leakage Current vs. Temperature



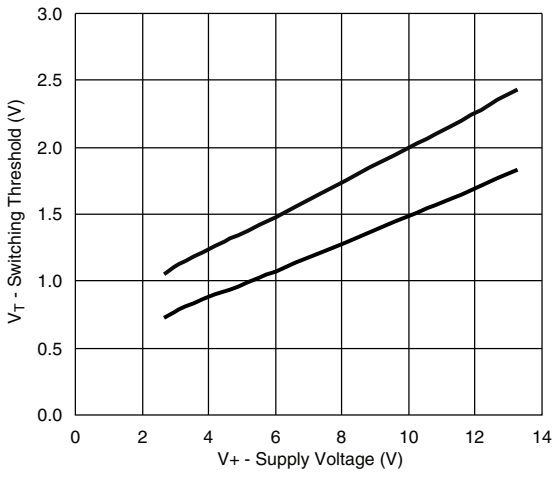
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Charge Injection vs. Analog Voltage



Total Harmonic Distortion vs. Frequency



Switching Threshold vs. Supply Voltage

TEST CIRCUITS

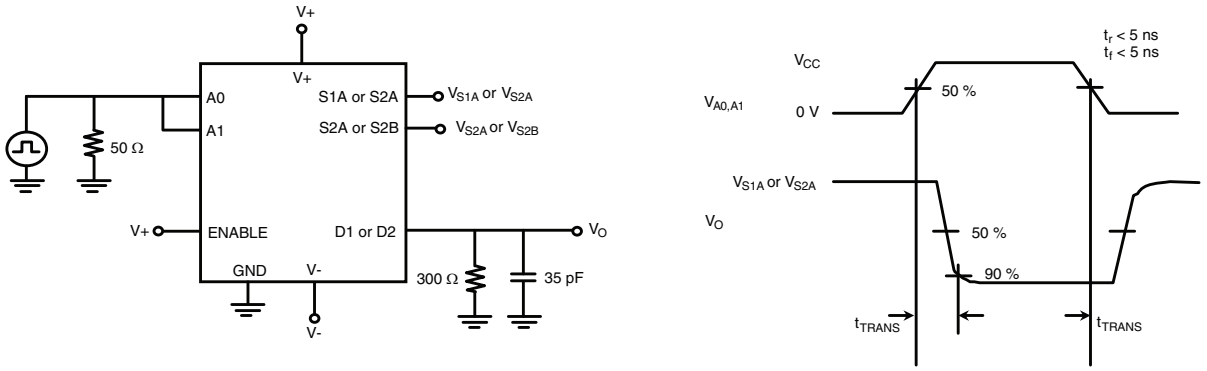


Fig. 1 - Transition Time

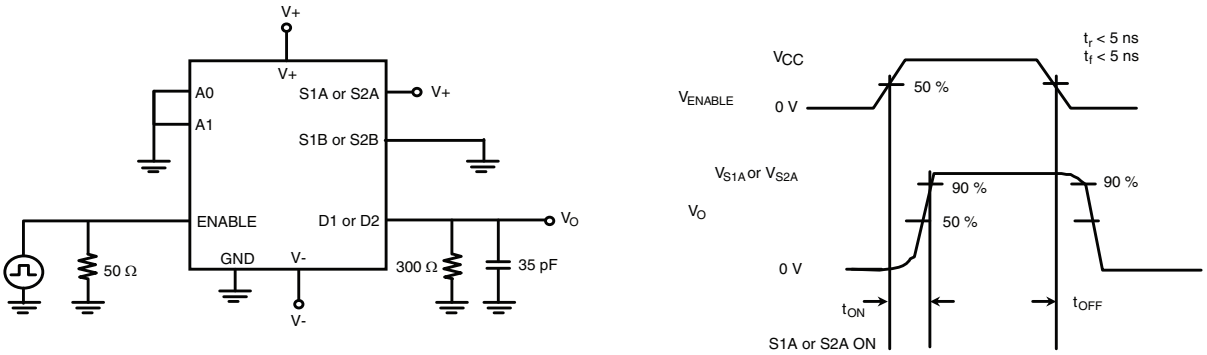


Fig. 2 - Enable Switching Time

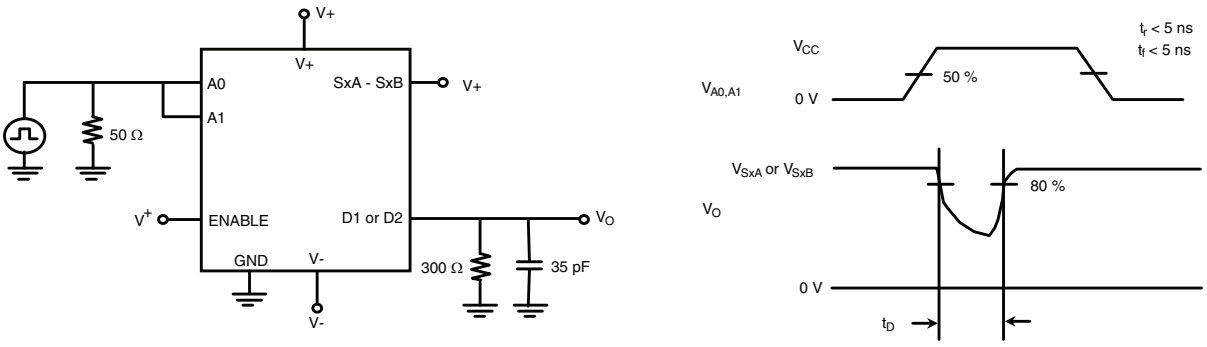


Fig. 3 - Break-Before-Make

TEST CIRCUITS

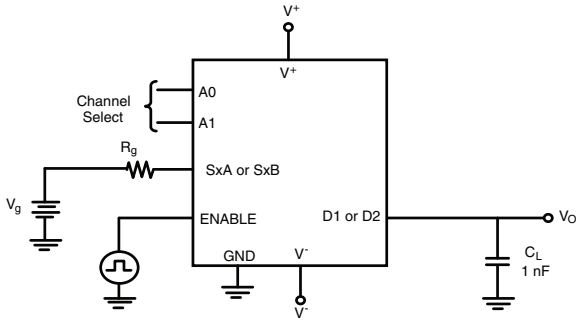


Fig. 4 - Charge Injection

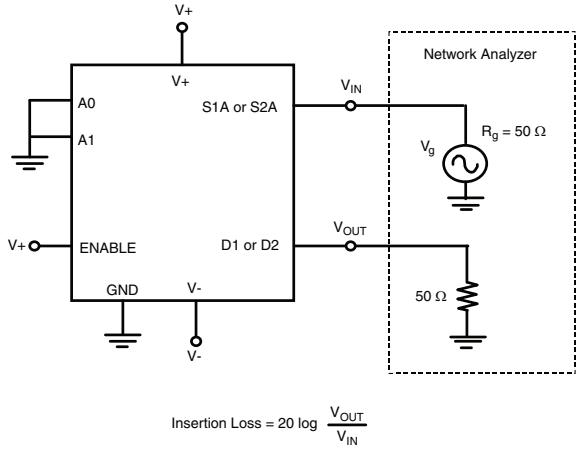


Fig. 5 - Insertion Loss

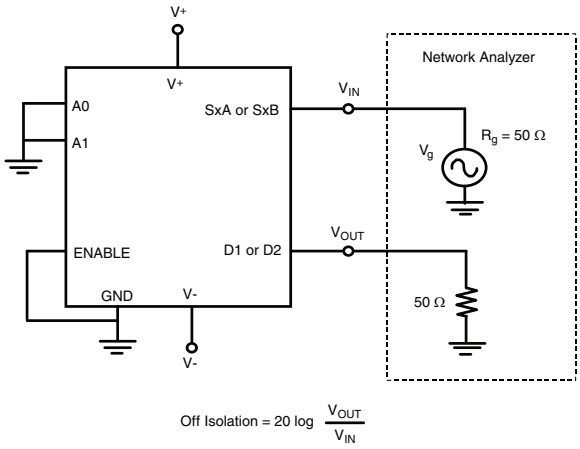


Fig. 7 - Off-Isolation

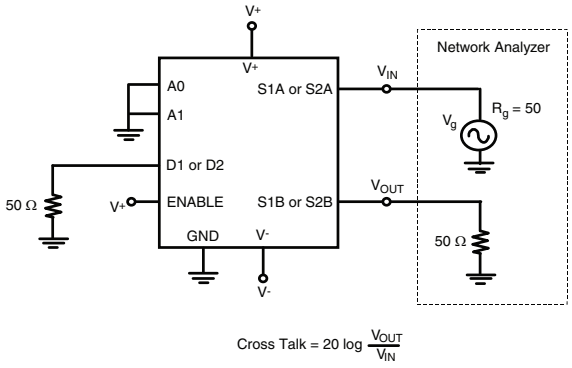


Fig. 6 - Crosstalk

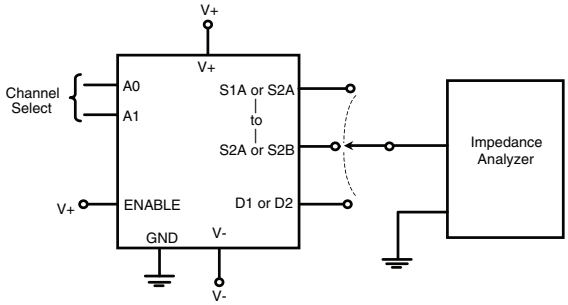
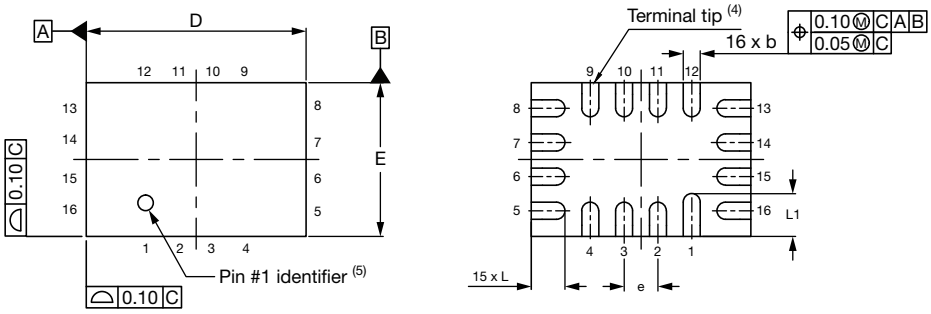


Fig. 8 - Source/Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69901.

Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

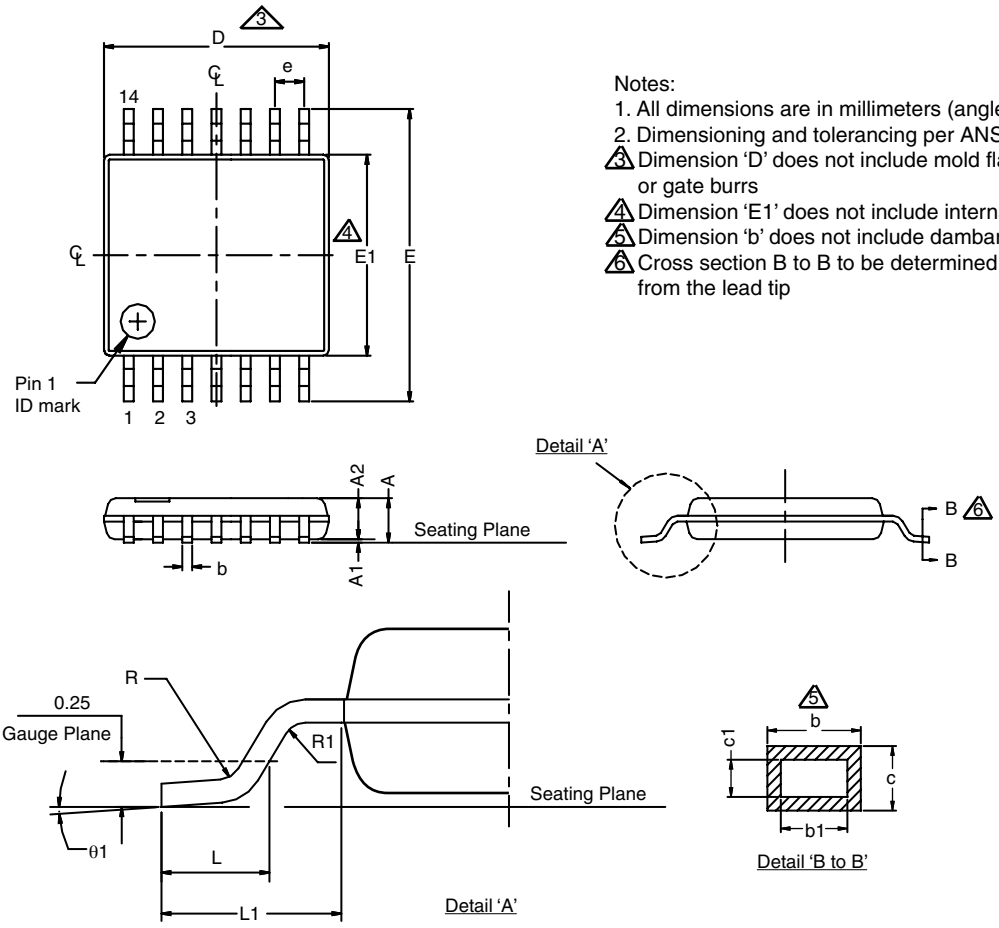
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

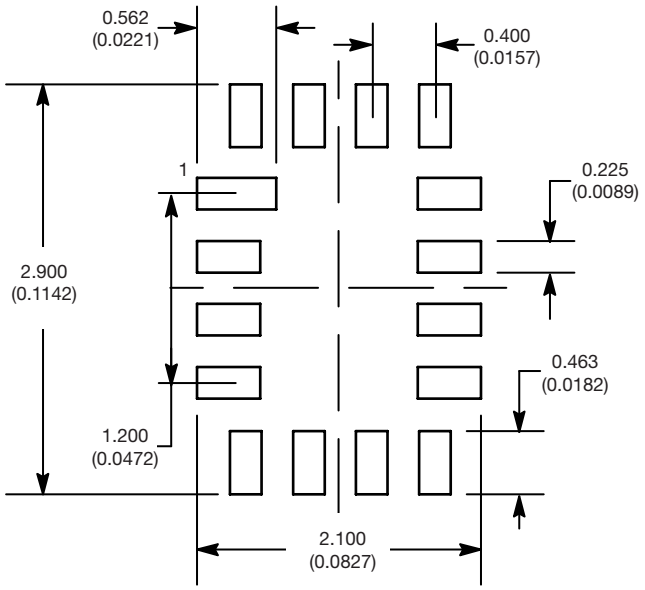
14L TSSOP



Notes:
1. All dimensions are in millimeters (angles in degrees)
2. Dimensioning and tolerancing per ANSI Y14.5M-1982
3. Dimension 'D' does not include mold flash, protrusions or gate burrs
4. Dimension 'E1' does not include internal flash or protrusion
5. Dimension 'b' does not include dambar protrusion
6. Cross section B to B to be determined at 0.10 mm to 0.25 mm from the lead tip

SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.05
D	4.9	5.0	5.1
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	-	-
R1	0.09	-	-
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
θ1	0°	-	8°
L1	1.0 ref.		
e	0.65 BSC		
ECN: T-07766-Rev. A, 14-Jan-08 DWG: 5962			

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

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