Quad SPST CMOS Analog Switch with Latches

Features

- Accepts 150-ns Write Pulse Width
- 5-V On-Chip Regulator
- Built on PLUS-40 Process
- Latches Are Transparent with $\overline{WR}$ Low
- Low On-Resistance: 60 Ω

Benefits

- Compatible with Most µP Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Consumption
- Allows Flexibility of Design

Applications

- µP Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems
- Medical Instrumentation
- Factory Automation

Description

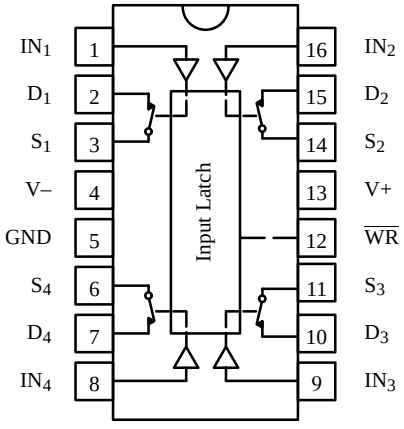
The DG221 is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common $\overline{WR}$ pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix PLUS-40 CMOS process, the DG221 combines low power and low on-resistance (60 Ω typical) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

The device features true bidirectional performance in the on condition. These switches guarantee a rail-to-rail blocking capability (44 V max), in the off condition.

Functional Block Diagram and Pin Configuration

Dual-In-Line and SOIC



Top View

Four Latchable SPST Switches per Package

Truth Table

IN_X	$\overline{WR}$	Switch
0	0	ON
1	0	OFF
X	↓	Control data latched-in, switches on or off as selected by last IN_X
X	1	Maintains previous state

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Ordering Information

Temp Range	Package	Part Number
0°C to 70°C	16-Pin Plastic DIP	DG221CJ
–40°C to 85°C	16-Pin Narrow SOIC	DG221DY
–55°C to 125°C	16-Pin CerDIP	DG221AK/883

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70041.

Absolute Maximum Ratings

Voltages Referenced to V–

V+ . . . . . 44 V

GND . . . . . 25 V

Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first

Continuous Current (Any Terminal) . . . . . 30 mA

Continuous Current, S or D . . . . . 20 mA

Peak Current, S or D (Pulsed 1 ms, 10% duty cycle) . . . . . 70 mA

Storage Temperature: (AK Suffix) . . . . . –65 to 150°C

(CJ and DY Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)[b]

16-Pin CerDIP[c] . . . . . 900 mW

16-Pin Plastic DIP[d] . . . . . 470 mW

16-Pin SOIC[e] . . . . . 600 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 12 mW/°C above 75°C

d. Derate 6.5 mW/°C above 25°C

e. Derate 7.7 mW/°C above 75°C

Schematic Diagram (Typical Channel)

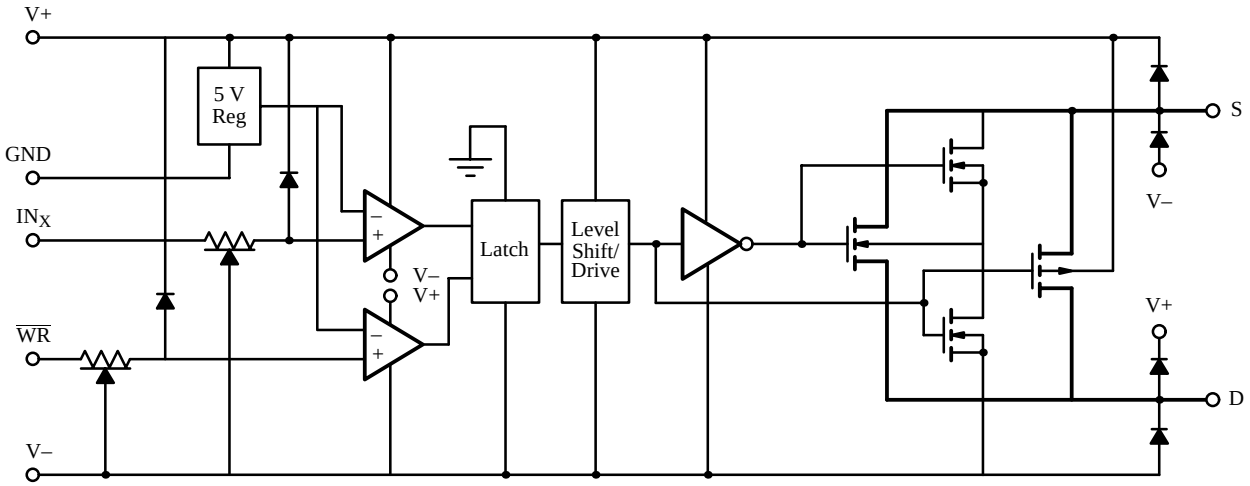


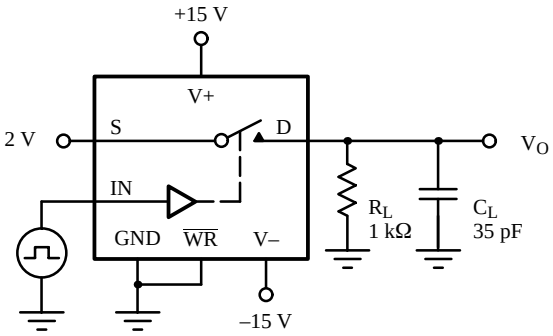
Figure 1.

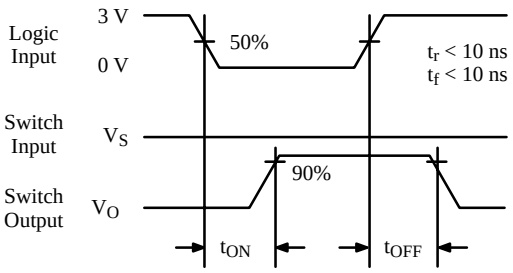
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 2.4 V, 0.8[f] V, $\overline{WR}$ = 0	Temp[b]	Typ[c]	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit
					Min[d]	Max[d]	Min[d]	Max[d]	
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ± 10 V	Room Full	60		90 135		90 135	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 14 V, V_D = ∓ 14 V	Room Full	± 0.01	–1 –100	1 100	–5 –100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$		Room Full	± 0.02	–1 –100	1 100	–5 –100	5 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 14 V	Room Full	± 0.01	–1 –200	1 200	–5 –200	5 200	
Digital Control									
Input Current	I_{INL}, I_{INH}	V_{IN} = 0 V or = 2.4 V	Room Full	–0.0004	–1 –10	1 10	–1 –10	1 10	µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room			550		550	ns
Turn-Off Time	t_{OFF}		Room			340		340	
Turn-On Time Write	t_{ON}, $\overline{WR}$	See Figure 3	Room			550		550	
Turn-Off Time Write	t_{OFF}, $\overline{WR}$		Room			340		340	
Write Pulse Width	t_W	See Figure 4	Room	120	150		150		
Input Setup Time	t_S		Room	130	180		180		
Input Hold Time	t_H		Full	0	20		20		
Charge Injection	Q	C_L = 1000 pF V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	20					pC
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S, V_D = 0 V	Room	8					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	9					
Channel-On Capacitance	$C_{D(on)}$		Room	29					
Off Isolation	OIRR	V_S = 1 V_{p-p}, f = 100 kHz C_L = 15 pF, R_L = 1 kΩ	Room	70					dB
Interchannel Crosstalk	X_{TALK}		Room	90					
Power Supplies									
Positive Supply Current	I+	All Channels On or Off V_{IN} = 0 V or 2.4 V	Full	0.8		1.5		1.5	mA
Negative Supply Current	I–		Room	–0.4	–1		–1		

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Test Circuits

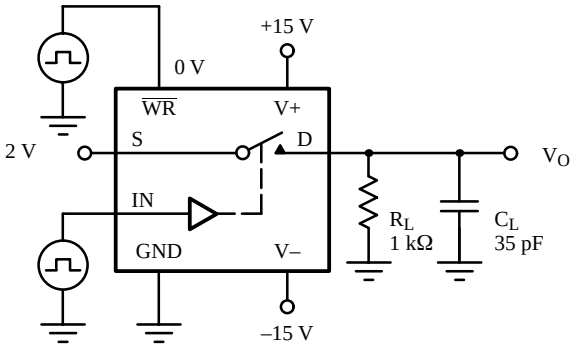


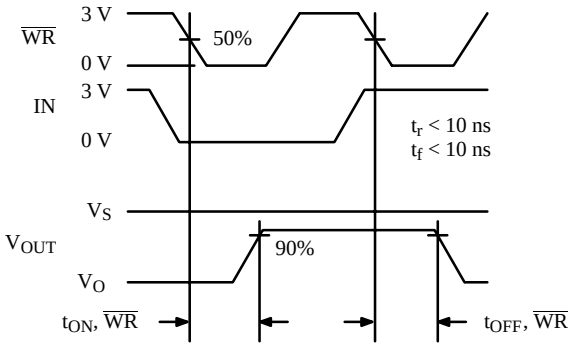


C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 2. Switching Time

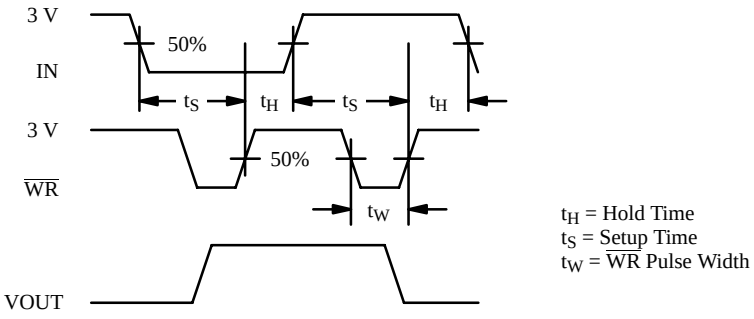




C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

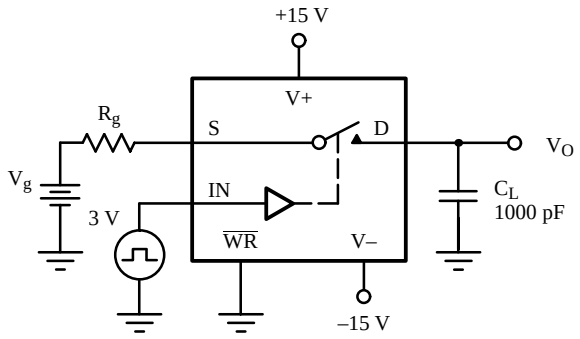
Figure 3. $\overline{WR}$ Switching Time

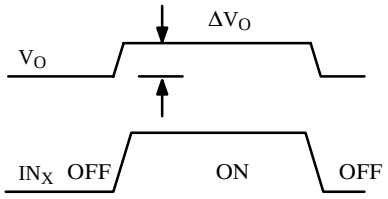


The latches are level sensitive. When $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

Figure 4. $\overline{WR}$ Setup Conditions

Test Circuits (Cont'd)





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

Figure 5. Charge Injection

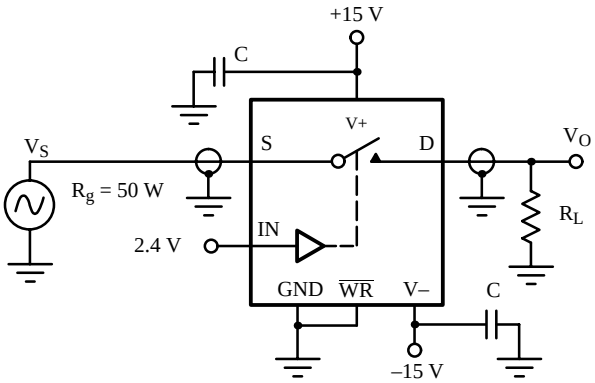


Figure 6. Off Isolation

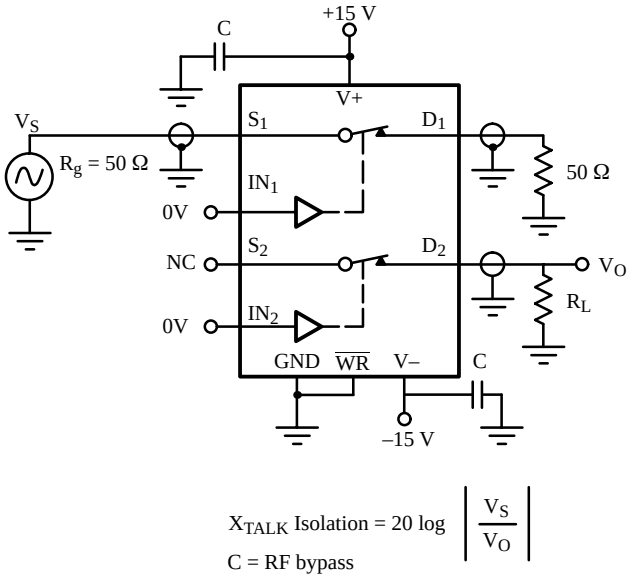


Figure 7. Channel-to-Channel Crosstalk

Application Hints[a]

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	GND (V)	$\overline{WR}$ (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	–15	0	2.4/0.8	2.4/0.8	–15 to 15
20	–20	0	2.4/0.8	2.4/0.8	–20 to 20
10	–10	0	2.4/0.8	2.4/0.8	–10 to 10
10	–5	0	2.4/0.8	2.4/0.8	–5 to 10

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

Applications

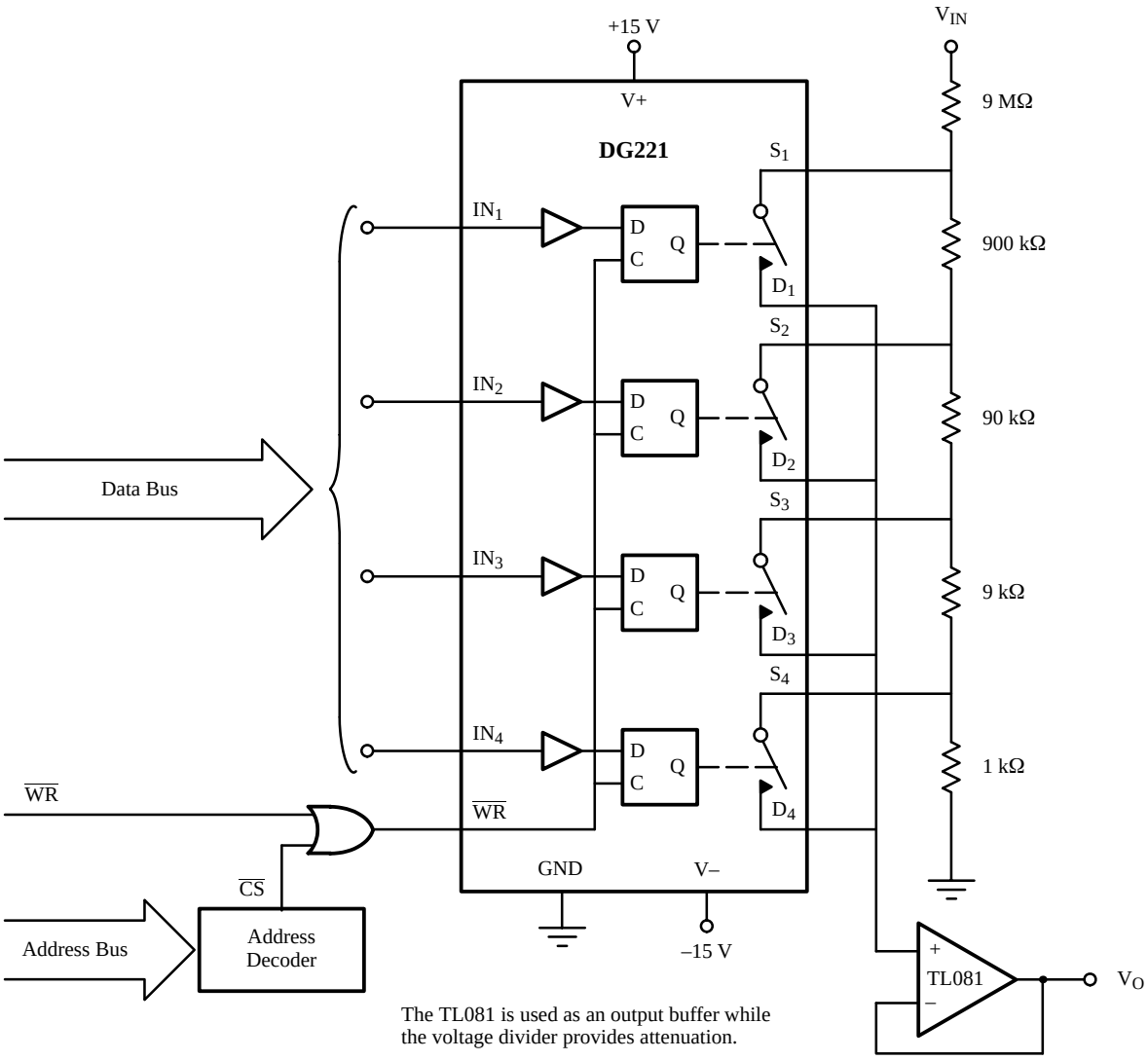


Figure 8. μP-Controlled Analog Signal Attenuator

Truth Table

IN_1	IN_2	IN_3	IN_4	$\overline{WR}$[a]	On Switch
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

Output Attenuation for Figure 8

WR	IN_1	IN_2	IN_3	IN_4	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

Notes:
a. $\overline{WR}$ may be held at “0” for temporary operation similar to DG201A/DG201B. With $\overline{WR}$ at “0” SW_1 will remain on as long as IN_1 is held at “0”.

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