

Single 8-Ch/Differential 4-Ch Latchable Analog Multiplexers

DESCRIPTION

The DG428, DG429 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary crosstalk of adjacent input signals.

The DG428 selects one of eight single-ended inputs to a common output, while the DG429 selects one of four differential inputs to a common differential output.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

The silicon-gate CMOS process enables operation over a wide range of supply voltages. The absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed and an epitaxial layer prevents latchup.

On-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- Low $R_{DS(on)}$: 55 Ω
- Low Charge Injection: 1 pC
- On-Board TTL Compatible Address Latches
- High Speed - t_{TRANS} : 160 ns
- Break-Before-Make
- Low Power Consumption: 0.3 mW
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

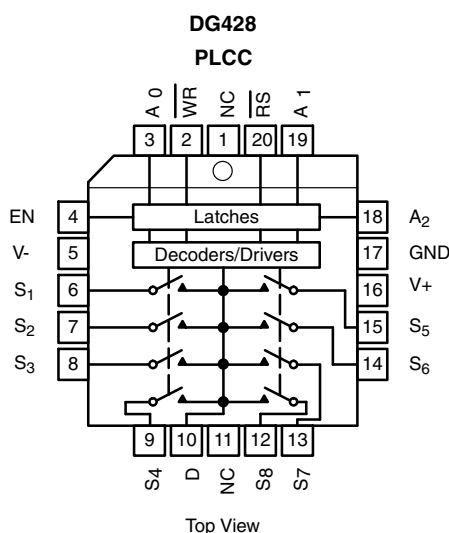
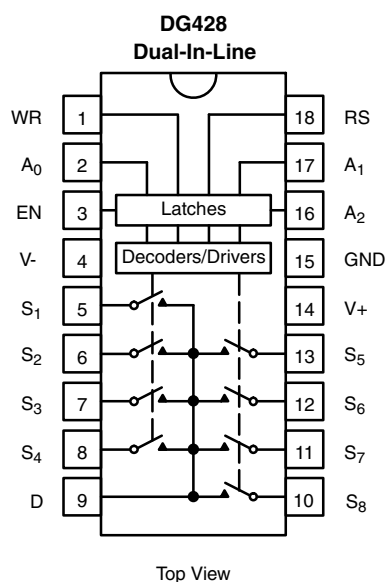
BENEFITS

- Improved System Accuracy
- Microprocessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk
- High Throughput
- Improved Reliability

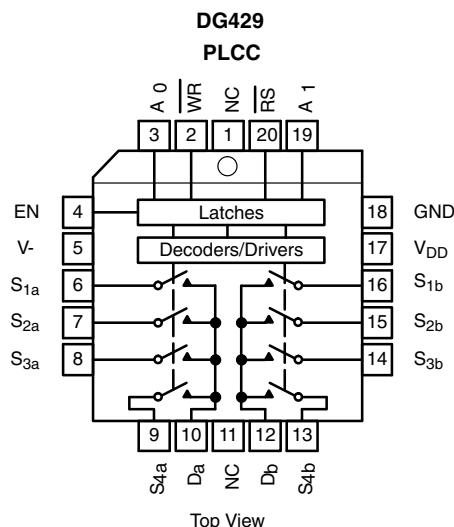
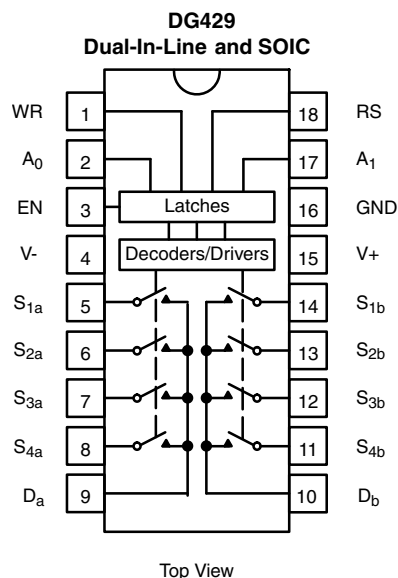
APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor-Controlled Analog Systems
- Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE - DG428						
8-Channel Single-Ended Multiplexer						
A ₂	A ₁	A ₀	EN	WR	RS	On Switch
Latching						
X	X	X	X		1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE - DG429					
Differential 4-Channel Multiplexer					
A ₁	A ₀	EN	WR	RS	On Switch
Latching					
X	X	X		1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8 \text{ V}$

Logic "1" = $V_{AH} \geq 2.4 \text{ V}$

X = Don't Care

ORDERING INFORMATION - DG428		
Temp Range	Package	Part Number
- 40 °C to 85 °C	18-pin Plastic DIP	DG428DJ
		DG428DJ-E3
	20-pin PLCC	DG428DN
		DG428DN-E3

ORDERING INFORMATION - DG429		
Temp Range	Package	Part Number
- 40 °C to 85 °C	18-pin Plastic DIP	DG429DJ
		DG429DJ-E3
	20-pin PLCC	DG429DN
		DG429DN-E3
	18-pin Widebody SOIC	DG429DW
		DG429DW-E3



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Voltages Referenced to V-	V+		44	V
	GND		25	
Digital Inputs ^a , V_S , V_D			(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first	
Current (Any Terminal)			30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max)			100	
Storage Temperature	(AK Suffix)		- 65 to 150	$^{\circ}\text{C}$
	(DJ, DN Suffix)		- 65 to 125	
Power Dissipation (Package) ^b	18-pin Plastic DIP ^c		470	mW
	18-pin CerDIP ^d		900	
	20-pin PLCC ^e		800	
	28-Pin Widebody SOIC ^f		450	

Notes:

- a. Signals on S_X , D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 6.3 mW/ $^{\circ}\text{C}$ above 75 $^{\circ}\text{C}$.
- d. Derate 12 mW/ $^{\circ}\text{C}$ above 75 $^{\circ}\text{C}$.
- e. Derate 10 mW/ $^{\circ}\text{C}$ above 75 $^{\circ}\text{C}$.
- f. Derate 6 mW/ $^{\circ}\text{C}$ above 75 $^{\circ}\text{C}$.

SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V, \overline{WR} = 0, \overline{RS} = 2.4 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, V _{AL} = 0.8 V I _S = - 1 mA, V _{AH} = 2.4 V		Room Full	55		100 125		100 125	Ω
Greatest Change in R _{DS(on)} Between Channels ^g	ΔR _{DS(on)}	- 10 V < V _S < 10 V I _S = - 1 mA		Room	5					%
Source Off Leakage Current	I _{S(off)}	V _S = ± 10 V, V _{EN} = 0 V, V _D = ± 10 V		Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50	nA
Drain Off Leakage Current	I _{D(off)}	V _{EN} = 0 V V _D = ± 10 V V _S = ± 10 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ± 10 V V _{EN} = 2.4 V V _{AL} = 0.8 V V _{AH} = 2.4 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	
Digital Control										
Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V		Full	0.01		1		1	μA
		V _A = 15 V		Full	0.01		1		1	
Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A = 0 V \overline{RS} = 0 V, \overline{WR} = 0 V		Full	- 0.01	- 1		- 1		
Logic Input Capacitance	C _{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t _{TRANS}	See Figure 5		Room Full	150		250 300		250 300	ns
Break-Before-Make Interval	t _{OPEN}	See Figure 4		Full	30	10		10		
Enable and Write Turn-On Time	t _{ON(EN,WR)}	See Figure 6 and 7		Room Full	90		150 225		150 225	
Enable and Reset Turn-Off Time	t _{OFF(EN,RS)}	See Figure 6 and 8		Room Full	55		150 300		150 300	
Charge Injection	Q	V _{GEN} = 0 V, R _{GEN} = 0 Ω C _L = 1 nF, See Figure 9		Room	1					pC
Off Isolation	OIRR	V _{EN} = 0 V, R _L = 300 Ω C _L = 15 pF, V _S = 7 V _{RMS} f = 100 kHz		Room	- 75					dB
Source Off Capacitance	C _{S(off)}	V _S = 0 V, V _{EN} = 0 V, f = 1 MHz		Room	11					pF
Drain Off Capacitance	C _{D(off)}	V _D = 0 V V _{EN} = 0 V f = 1 MHz	DG428	Room	40					
			DG429	Room	20					
Drain On Capacitance	C _{D(on)}		DG428	Room	54					
			DG429	Room	34					
Minimum Input Timing Requirements										
Write Pulse Width	t _W	See Figure 2		Full		100		100		ns
A _X , EN Data Set Up time	t _S			Full		100		100		
A _X , EN Data Hold Time	t _H			Full		10		10		
Reset Pulse Width	t _{RS}	V _S = 5 V, See Figure 3		Full		100		100		
Power Supplies										
Positive Supply Current	I ₊	V _{EN} = V _A = 0, \overline{RS} = 5 V		Room	20		100		100	μA
Negative Supply Current	I ₋			Room	- 0.001	- 5		- 5		



SPECIFICATIONS ^a (for single supply)										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 12 V, V ₋ = 0 V, WR = 0, RS = 2.4 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55°C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 10 V, V _{AL} = 0.8 V I _S = - 500 μA, V _{AH} = 2.4 V		Room	80		150		150	Ω
R _{DS(on)} Match ^g	ΔR _{DS(on)}	0 V < V _S < 10 V I _S = - 1 mA		Room	5					%
Source Off Leakage Current	I _{S(off)}	V _S = 0 V, 10 V, V _{EN} = 0 V, V _D = 10 V, 0 V		Room Full	± 0.03	- 0.5 - 50	0.5 50	- 0.5 - 50	0.5 50	nA
Drain Off Leakage Current	I _{D(off)}	V _D = 0 V, 10 V V _S = 10 V, 0 V V _{EN} = 0 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = 0 V, 10 V V _{EN} = 2.4 V V _{AL} = 0.8 V V _{AH} = 2.4 V	DG428	Room Full	± 0.07	- 1 - 100	1 100	- 1 - 100	1 100	
			DG429	Room Full	± 0.05	- 1 - 50	1 50	- 1 - 50	1 50	
Digital Control										
Logic Input Current Input Voltage High	I _{AH}	V _A = 2.4 V		Full			1		1	μA
		V _A = 12 V		Full			1		1	
Logic Input Current Input Voltage Low	I _{AL}	V _{EN} = 0 V, 2.4 V, V _A = 0 V RS = 0 V, WR = 0 V		Full		- 1		- 1		
Dynamic Characteristics										
Transition Time	t _{TRANS}	S ₁ = 10 V/ 2 V, S ₈ = 2 V/ 10 V See Figure 5		Room Full	160		280 350		280 350	ns
Break-Before-Make Interval	t _{OPEN}	See Figure 4		Room Full	40	25 10		25 10		
Enable and WriteTurn-On Time	t _{ON(EN,WR)}	S ₁ = 5 V See Figure 6 and 7		Room Full	110		300 400		300 400	
Enable and Reset Turn-Off Time	t _{OFF(EN,RS)}	S ₁ = 5 V See Figure 6 and 8		Room Full	70		300 400		300 400	
Charge Injection	Q	V _{GEN} = 6 V, R _{GEN} = 0 Ω C _L = 1 nF, See Figure 9		Room	4					pC
Off Isolation	OIRR	V _{EN} = 0 V, R _L = 300 Ω C _L = 15 pF, V _S = 7 V _{RMS} f = 100 kHz		Room	- 75					dB
Minimum Input Timing Requirements										
Write Pulse Width	t _W	See Figure 2		Full		100		100		ns
A _X , EN Data Set Up time	t _S			Full		100		100		
A _X , EN Data Hold Time	t _H			Full		10		10		
Reset Pulse Width	t _{RS}	V _S = 5 V, See Figure 3		Full		100		100		
Power Supplies										
Positive Supply Current	I ₊	V _{EN} = 0 V, V _A = 0, RS = 5 V		Room	20		100		100	μA

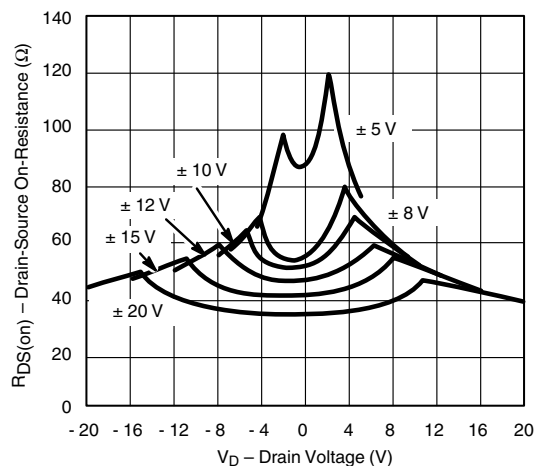
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

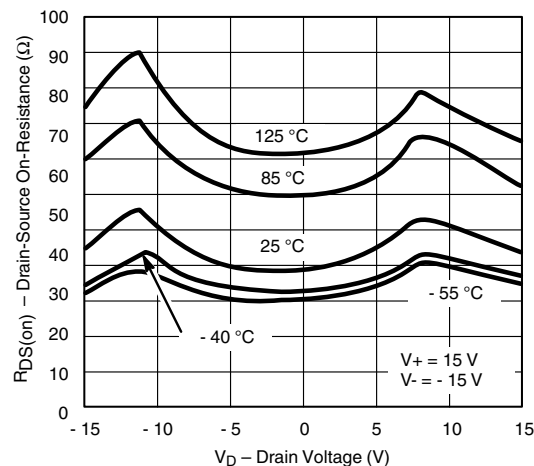
$$g. \Delta R_{DS(on)} = \left(\frac{R_{DS(on) \text{ MAX}} - R_{DS(on) \text{ MIN}}}{R_{DS(on) \text{ AVE}}} \right) \times 100 \%$$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

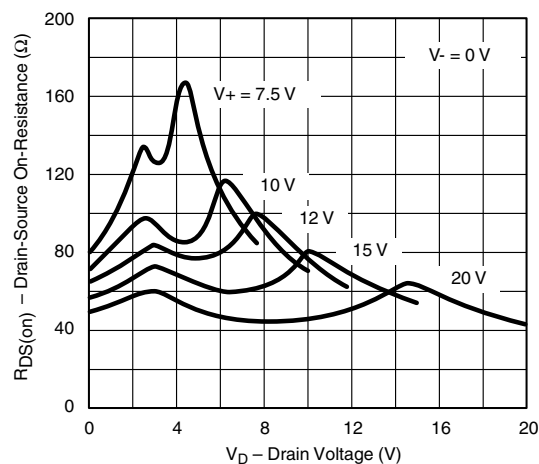
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



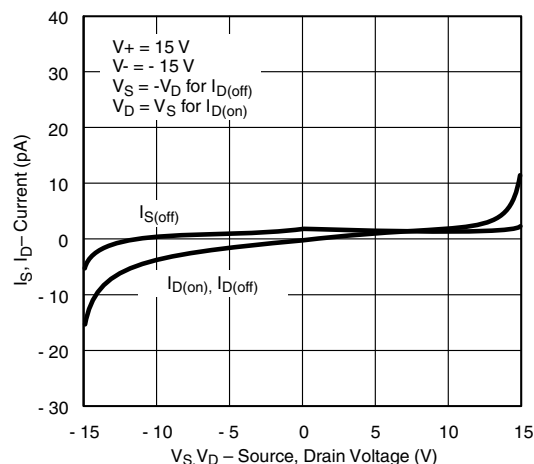
$R_{DS(on)}$ vs. V_D and Supply Voltage



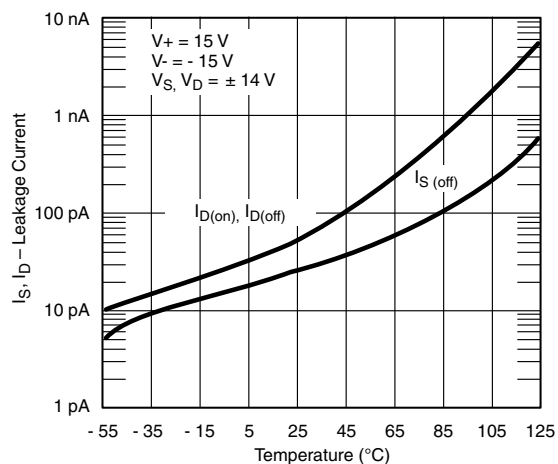
$R_{DS(on)}$ vs. V_D and Temperature



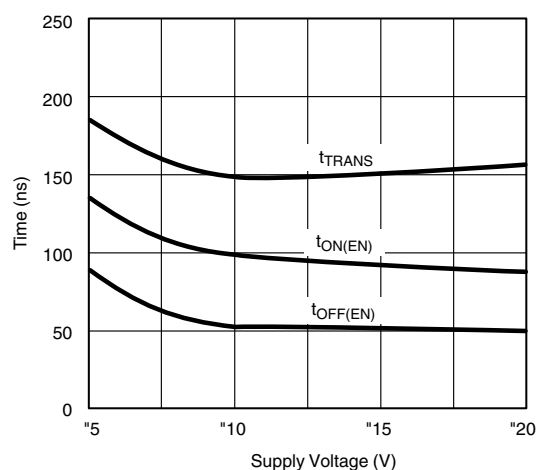
Single Supply $R_{DS(on)}$ vs. V_D and Supply



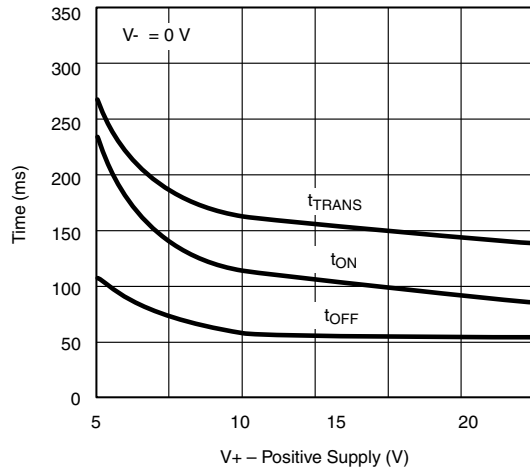
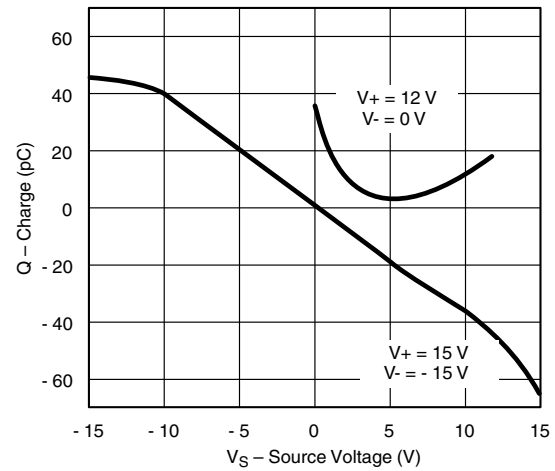
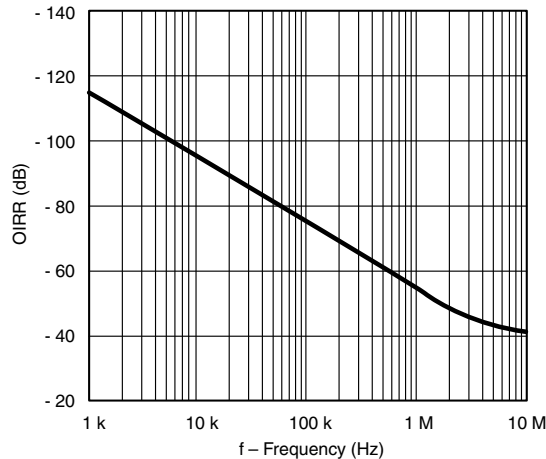
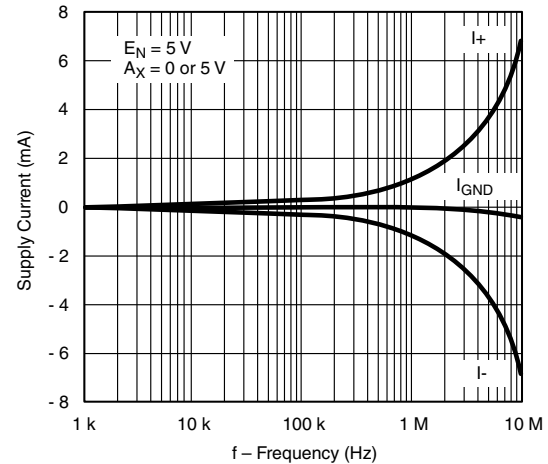
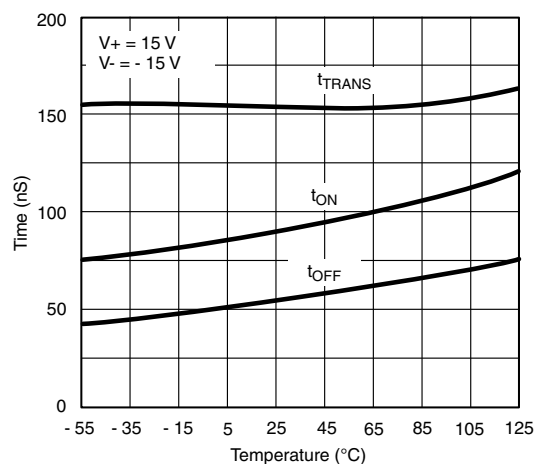
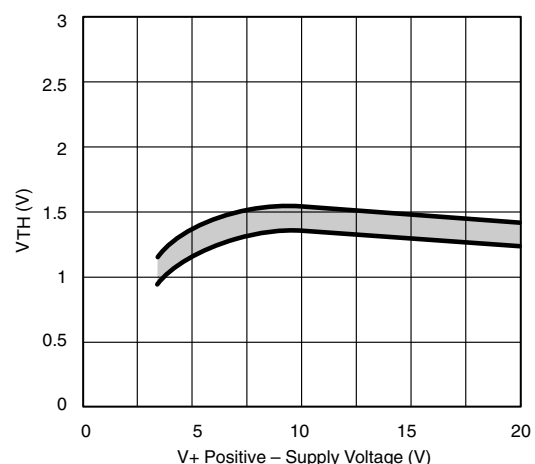
I_D , I_S Leakage Currents vs. Analog Voltage



I_D , I_S Leakes vs. Temperature



Switching Times vs. Power Supply Voltage

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Switching Times vs. Single Supply

Charge Injection vs. Analog Voltage

Off-Isolation vs. Frequency

Supply Currents vs. Switching Frequency

Switching Times vs. Temperature

Input Switching Threshold vs. Positive Supply Voltage

SCHEMATIC DIAGRAM (Typical Channel)

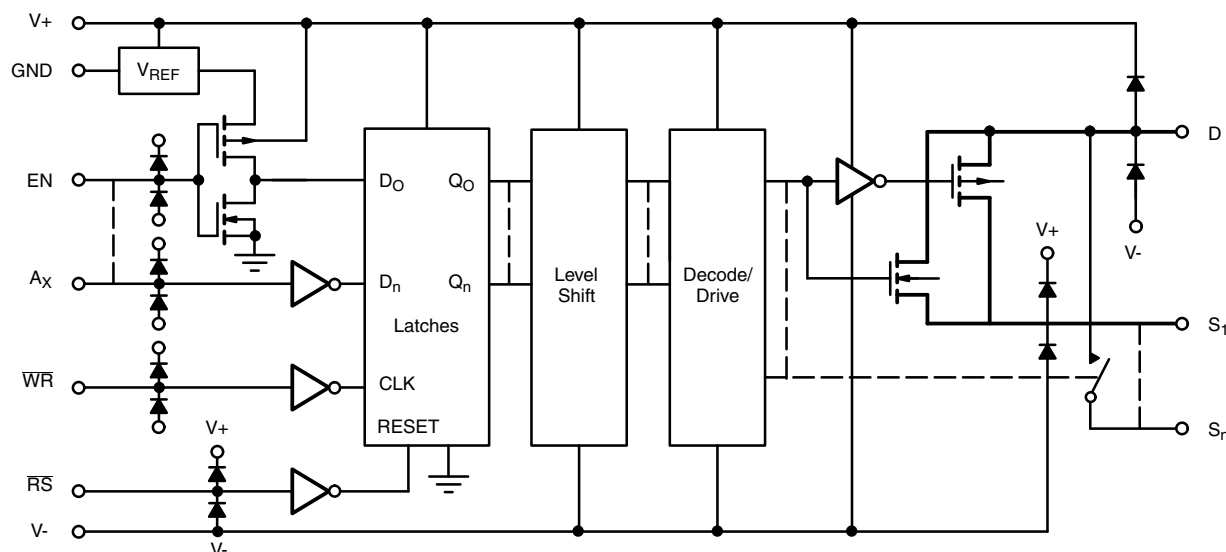


Figure 1.

TIMING DIAGRAMS

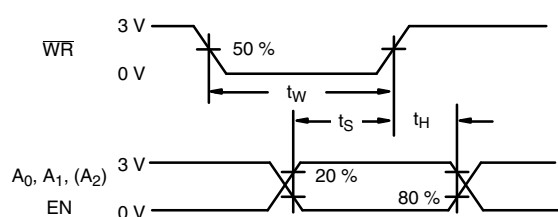


Figure 2.

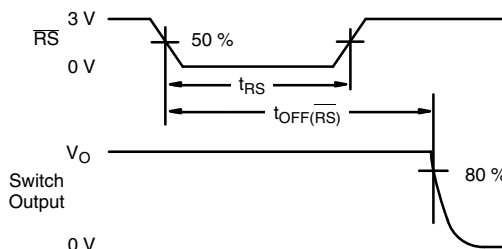


Figure 3.

TEST CIRCUITS

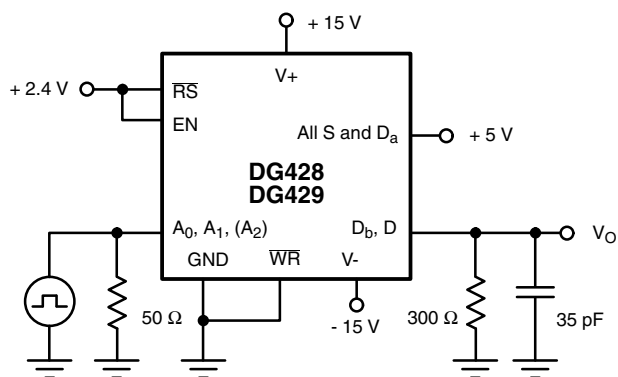
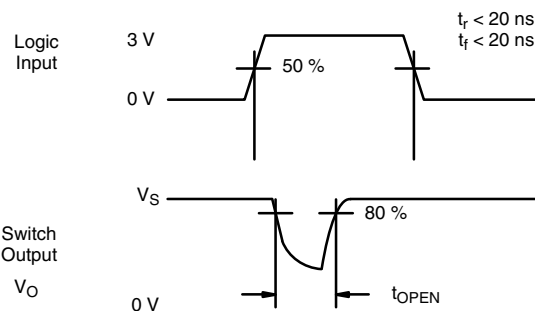
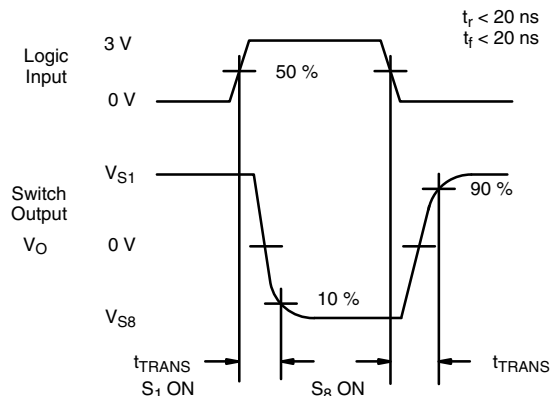
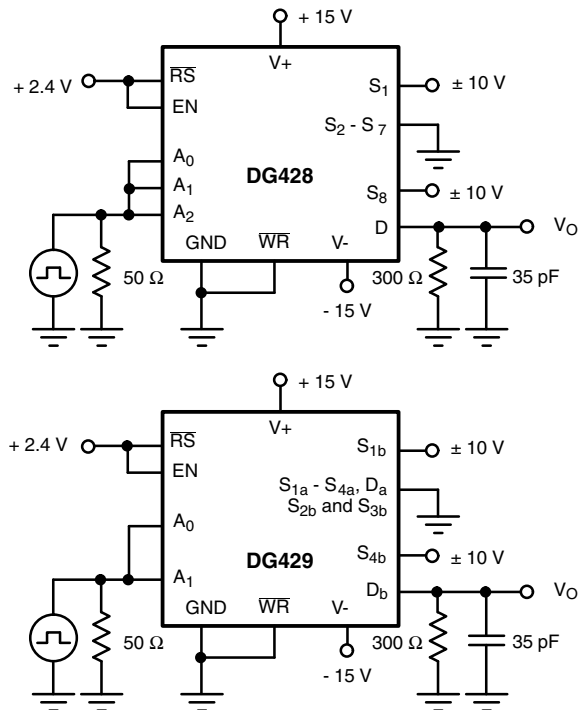
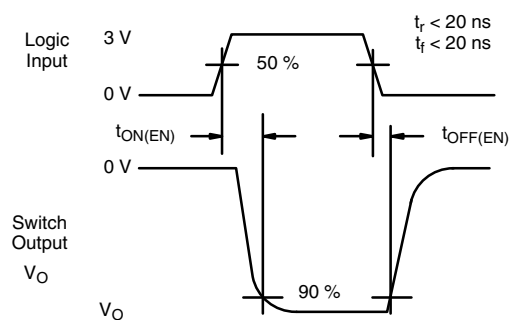
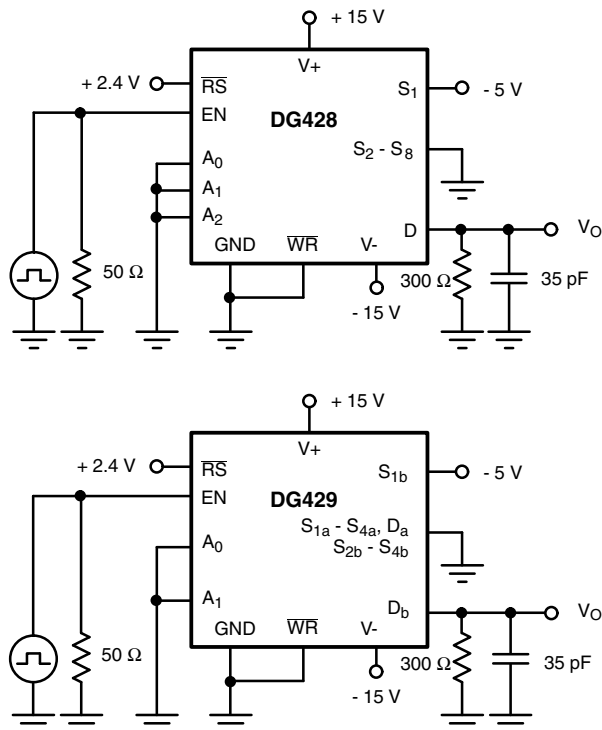


Figure 4. Break-Before-Make



TEST CIRCUITS

Figure 5. Transition Time

Figure 6. Enable $t_{\text{ON}}/t_{\text{OFF}}$ Time

TEST CIRCUITS

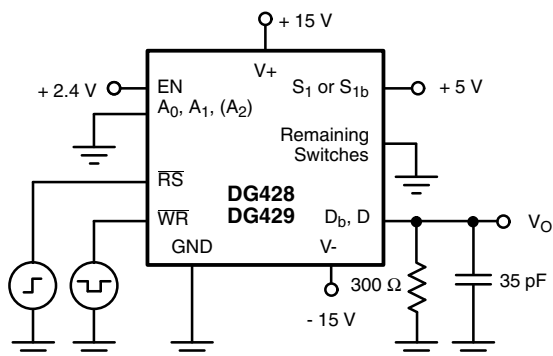


Figure 7. Write Turn-On Time $t_{ON(WR)}$

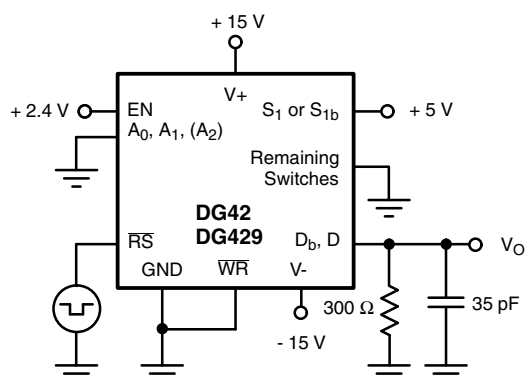
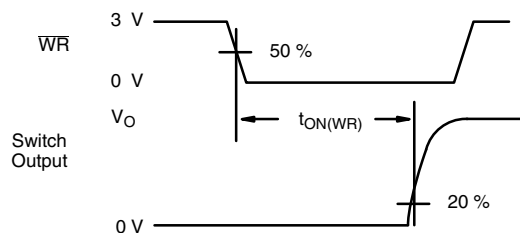


Figure 8. Reset Turn-Off Time $t_{OFF(RS)}$

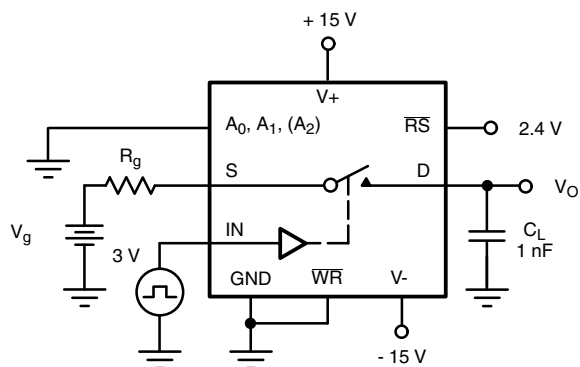
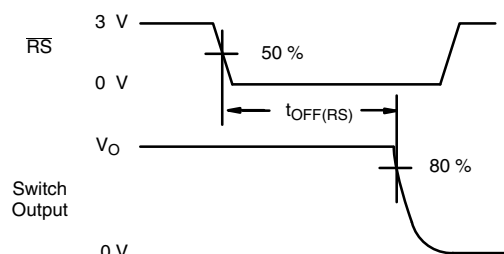
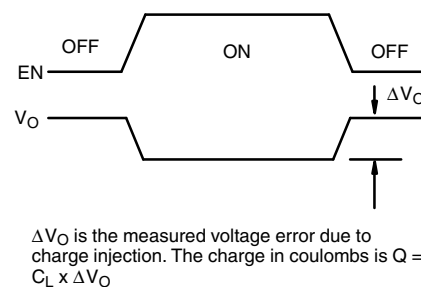


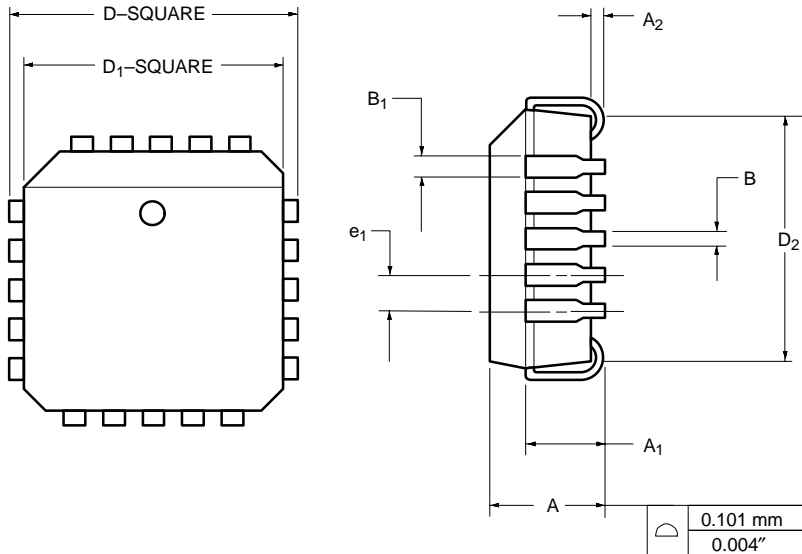
Figure 9. Charge Injection



APPLICATIONS HINTS



PLCC: 20-LEAD

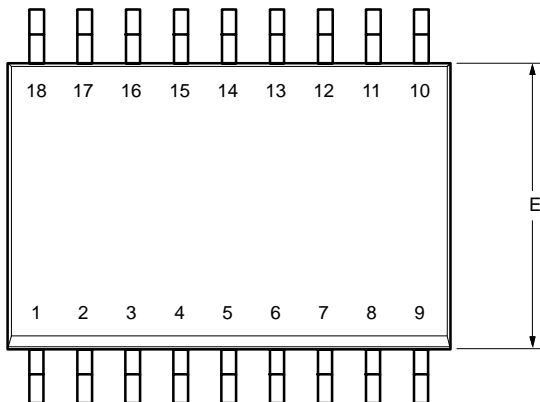


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A ₁	2.29	3.04	0.090	0.120
A ₂	0.51	—	0.020	—
B	0.331	0.553	0.013	0.021
B ₁	0.661	0.812	0.026	0.032
D	9.78	10.03	0.385	0.395
D ₁	8.890	9.042	0.350	0.356
D ₂	7.37	8.38	0.290	0.330
e ₁	1.27 BSC		0.050 BSC	

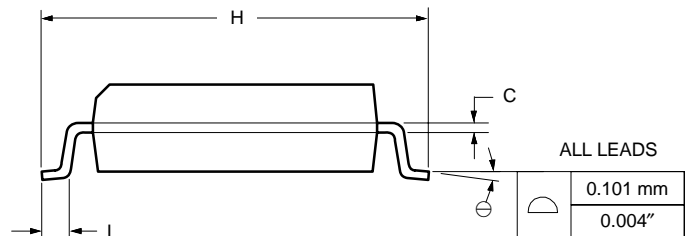
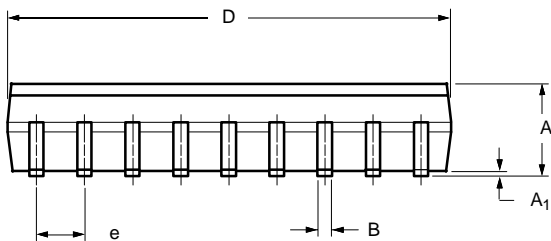
ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5306



SOIC (WIDE-BODY): 18-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A₁	0.10	0.30	0.004	0.012
B	0.35	0.45	0.014	0.018
C	0.23	0.28	0.009	0.011
D	11.25	12.45	0.443	0.490
E	7.25	8.00	0.285	0.315
e	1.27 BSC		0.050 BSC	
H	9.80	10.60	0.386	0.417
L	0.60	1.00	0.024	0.039
\ominus	0°	8°	0°	8°
ECN: S-03946—Rev. C, 09-Jul-01 DWG: 5302				





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