



### N-Channel 20-V (D-S) MOSFET

#### CHARACTERISTICS

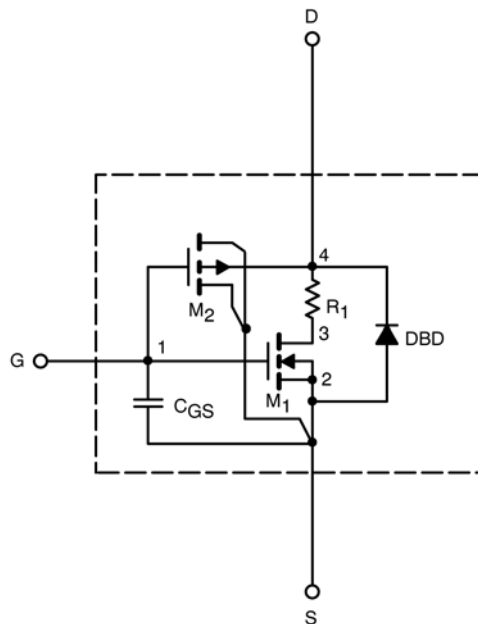
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si4408DY

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SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1.7		V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$ , $V_{GS} = 10\ \text{V}$	1056		A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$ , $I_D = 21\ \text{A}$	0.0036	0.0035	$\Omega$
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 17\ \text{A}$	0.0054	0.0054	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 6\ \text{V}$ , $I_D = 21\ \text{A}$	61	60	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.9\ \text{A}$ , $V_{GS} = 0\ \text{V}$	0.76	0.75	V
<b>Dynamic<sup>b</sup></b>					
Total Gate Charge	$Q_g$	$V_{DS} = 10\ \text{V}$ , $V_{GS} = 4.5\ \text{V}$ , $I_D = 21\ \text{A}$	22	21	nC
Gate-Source Charge	$Q_{gs}$		8.9	8.9	
Gate-Drain Charge	$Q_{gd}$		6.4	6.4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}$ , $V_{GEN} = 4.5\ \text{V}$ , $R_G = 6\ \Omega$	26	42	ns
Rise Time	$t_r$		44	42	
Turn-Off Delay Time	$t_{d(off)}$		60	60	
Fall Time	$t_f$		96	26	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.9\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$	60	55	

### Notes

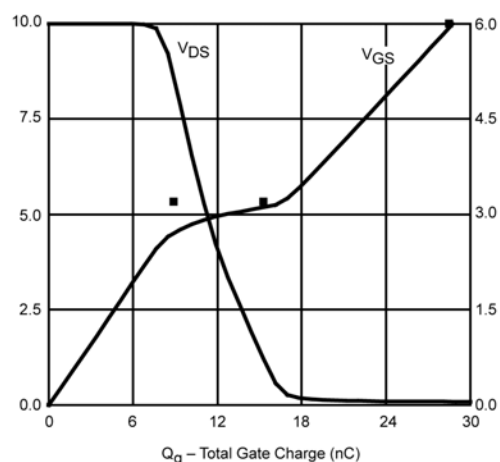
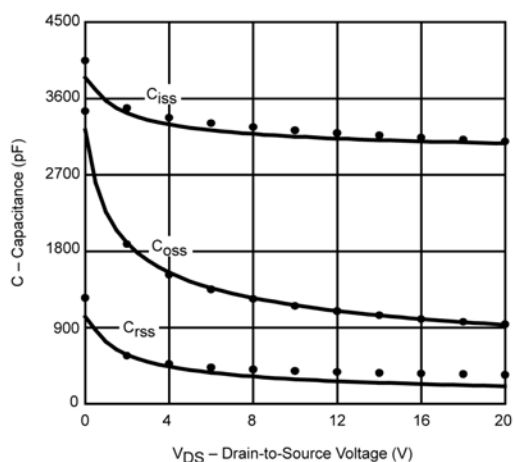
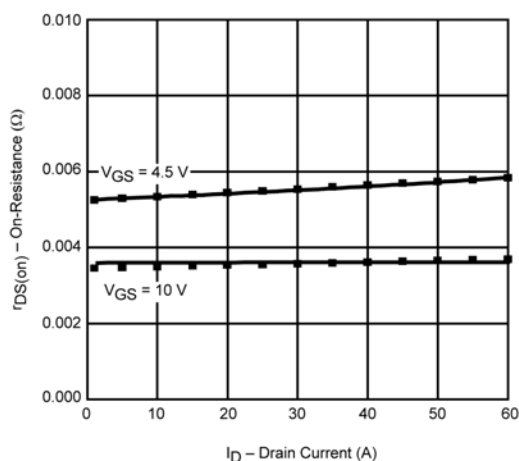
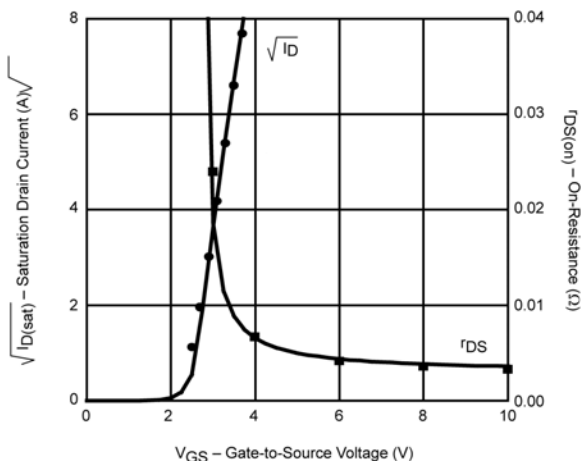
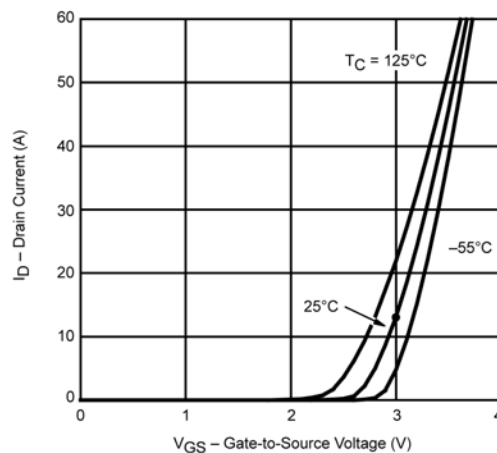
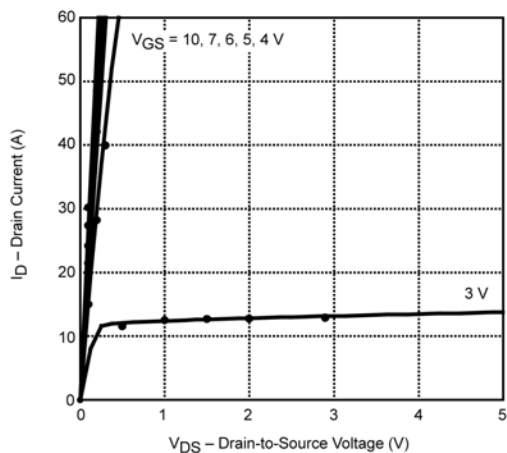
- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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