

N-Channel 80-V (D-S) MOSFET

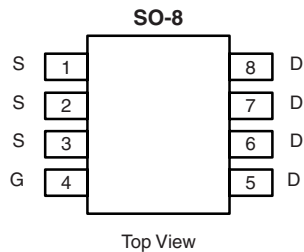
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
80	0.035 at $V_{GS} = 10$ V	6.0
	0.040 at $V_{GS} = 6.0$ V	5.5

FEATURES

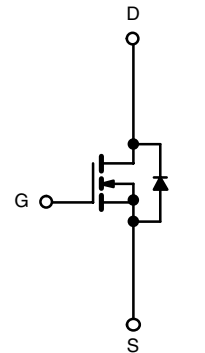
- Halogen-free According to IEC 61249-2-21 Definiton
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4480DY-T1-E3 (Lead (Pb)-free)
Si4480DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	A
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	40	
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	W
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	°C/W

Notes:

a. Surface Mounted on FR4 board, $t \leq 10$ s.

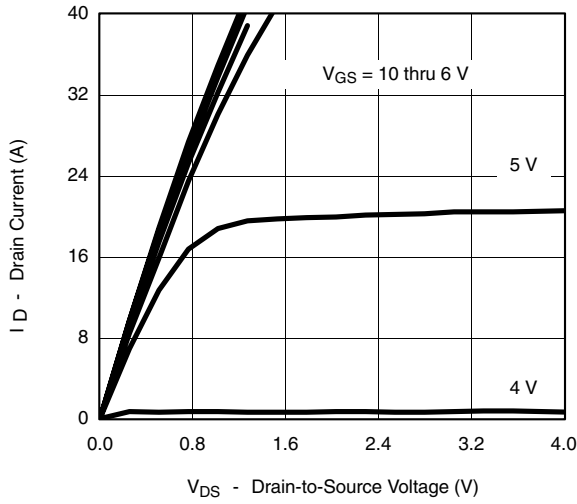
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^b	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 6.0\text{ A}$		0.026	0.035	Ω
		$V_{GS} = 6.0\text{ V}$, $I_D = 5.5\text{ A}$		0.030	0.040	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 6.0\text{ A}$		25		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.1\text{ A}$, $V_{GS} = 0\text{ V}$			1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 40\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 6.0\text{ A}$		30	50	nC
Gate-Source Charge	Q_{gs}			9		
Gate-Drain Charge	Q_{gd}			5.6		
Gate Resistance	R_g		1.5		4.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}$, $R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$		12.5	25	ns
Rise Time	t_r			12.5	25	
Turn-Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			22	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		50	80	

Notes:

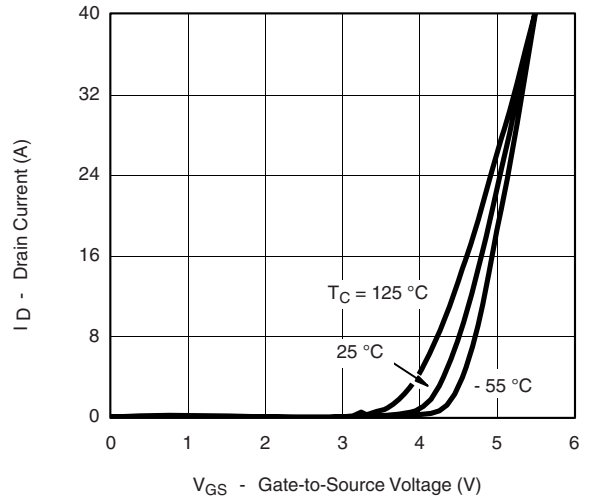
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. For design aid only; not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

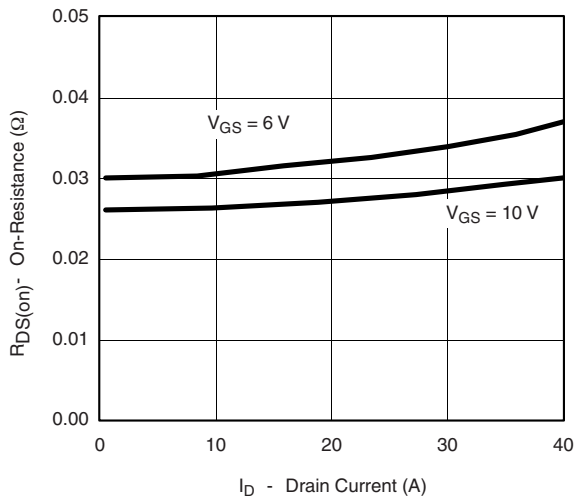
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



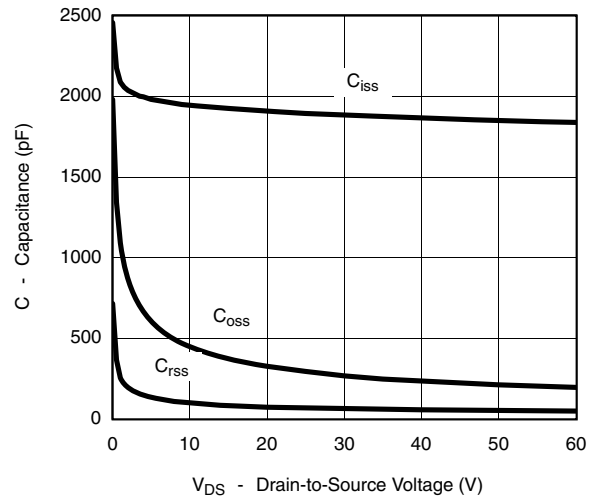
Output Characteristics



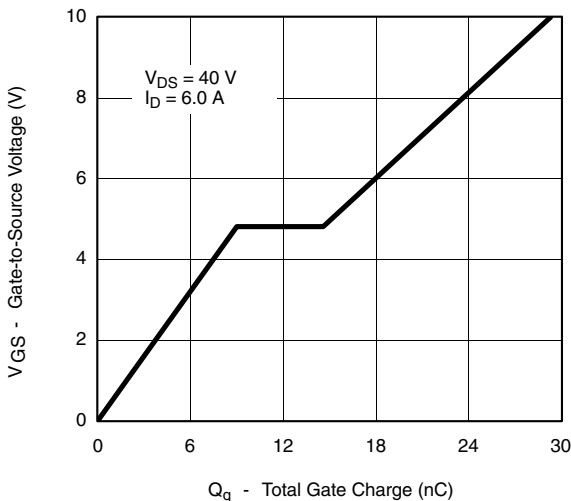
Transfer Characteristics



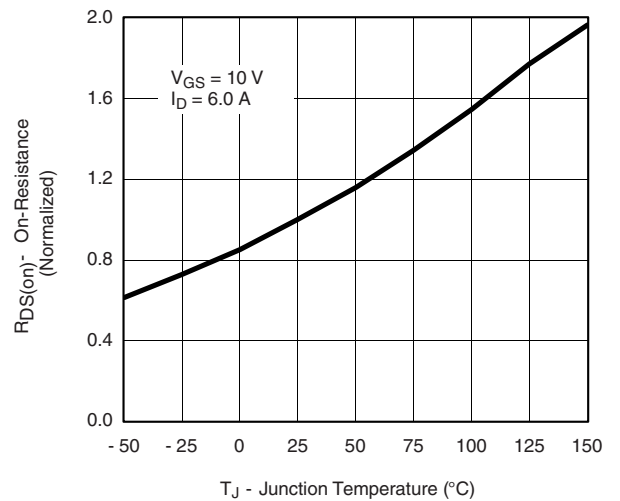
On-Resistance vs. Drain Current



Capacitance

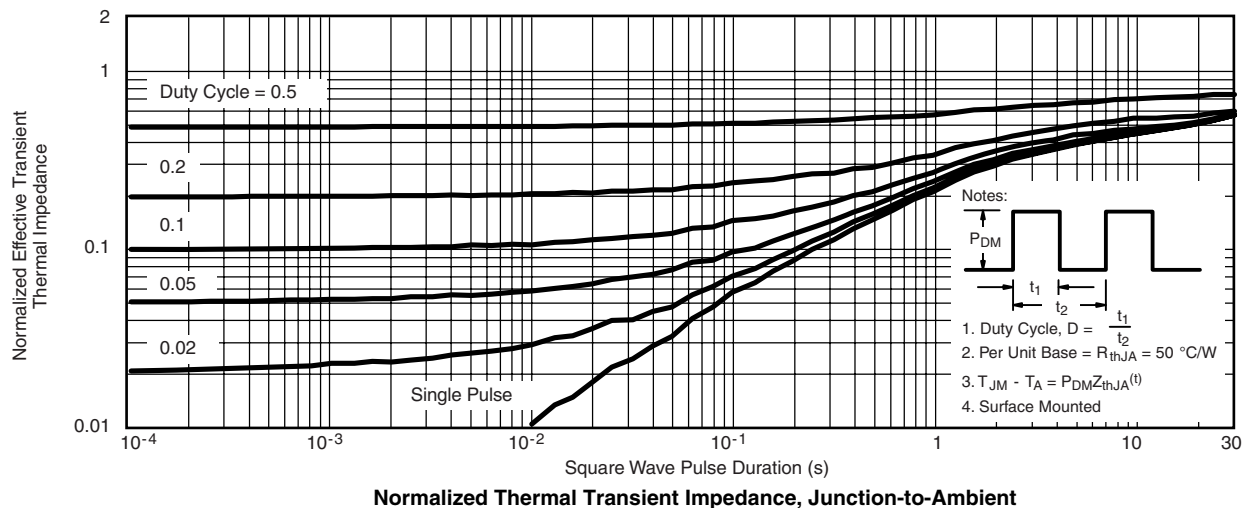
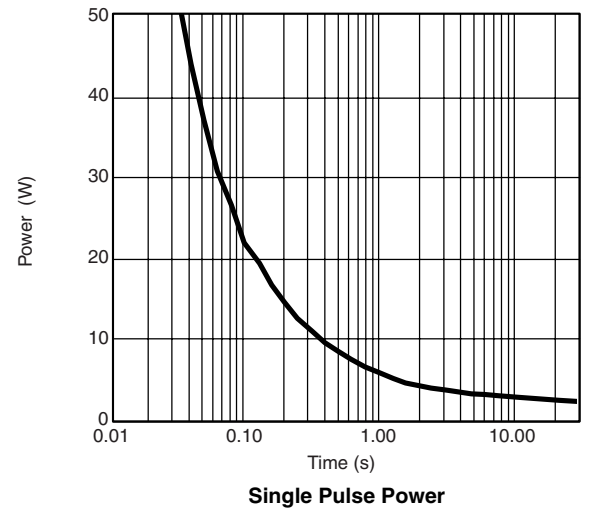
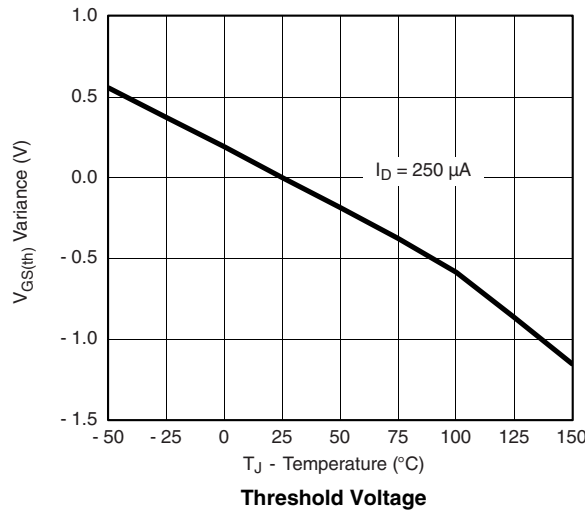
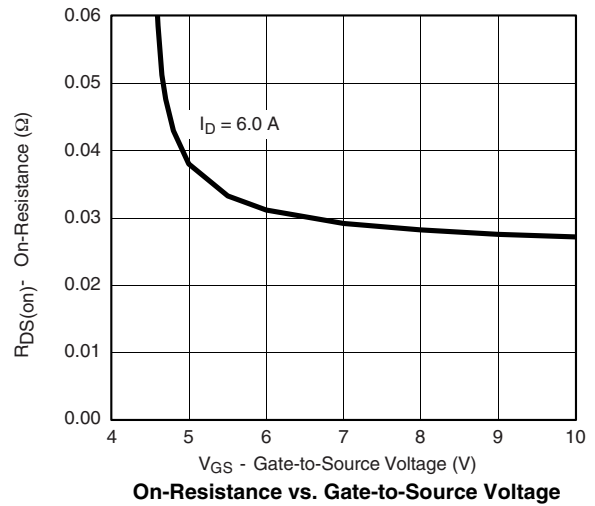
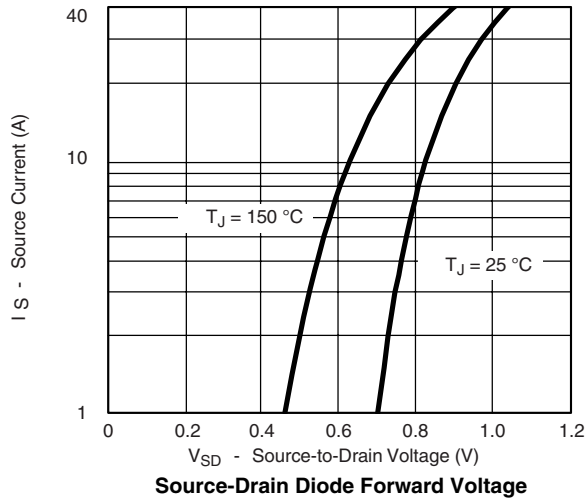


Gate Charge



On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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