HALOGEN FREE





N-Channel 20-V (D-S) MOSFET

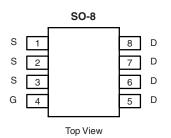
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A)		
20	0.0045 at V _{GS} = 10 V	21		
	0.0068 at V _{GS} = 4.5 V	17		

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- · PWM Optimized for Fast Switching
- Low Switching Losses
- · Low Gate Drive Losses
- 100 % R_q Tested

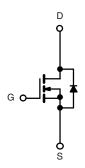


• Self-Driven Synchronous Rectification



Ordering Information: Si4408DY-T1-E3 (Lead (Pb)-free)

Si4408DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_{μ}	$_{\Lambda}$ = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current /T 150 °C\a	T _A = 25 °C	- I _D	21	14	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		17	11	^
Pulsed Drain Current (10 µs Pulse Width)		I _{DM}	60		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.3	
Marian and Demon Discipation 8	T _A = 25 °C	P _D	3.5	1.6	W
Maximum Power Dissipation ^a	T _A = 70 °C] ' ⁻ D	2.2	1	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana la Antica de Antica de	t ≤ 10 s	R _{thJA}	29	35	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	67	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	16	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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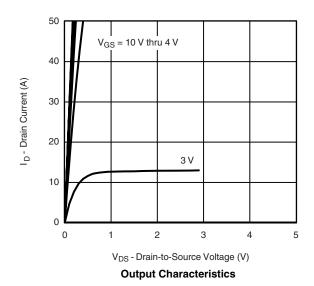
Parameter	Symbol	ymbol Test Conditions		Тур.	Max.	Unit	
Static					<u>I</u>		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zovo Coto Voltogo Dvoin Curvent	1	V _{DS} = 16 V, V _{GS} = 0 V			1	1 5 μA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
5	В	V _{GS} = 10 V, I _D = 21 A		0.0035			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$		0.0054	0.0068	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 \text{ V}, I_{D} = 21 \text{ A}$		60		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.75	1.1	V	
Dynamic ^b			•	•			
Total Gate Charge	Q_g			21	32		
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 21 \text{ A}$		8.9		nC	
Gate-Drain Charge	Q_{gd}			6.4			
Gate Resistance	R_g		0.5	1.40	2.4	Ω	
Turn-On Delay Time	t _{d(on)}			42	65		
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		42	65		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 4.5 V, R_g = 6 Ω		60	90	ns	
Fall Time	t _f			26	40		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, dI/dt = 100 A/μs		55	80		

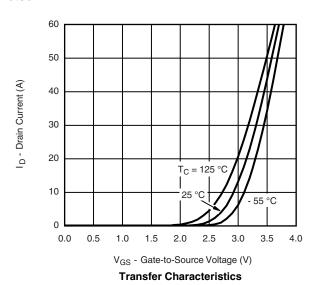
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

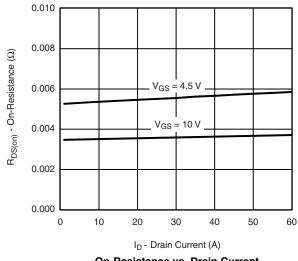




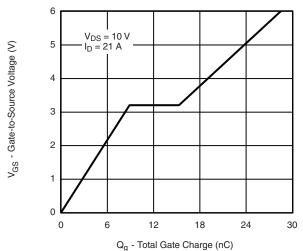




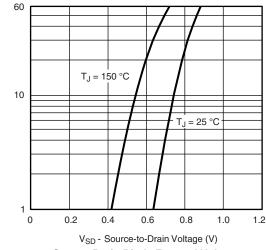
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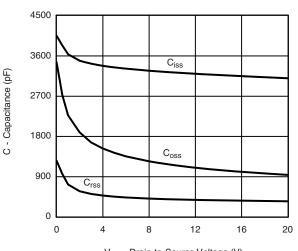
On-Resistance vs. Drain Current



Gate Charge

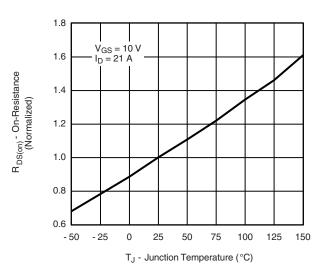


Source-Drain Diode Forward Voltage

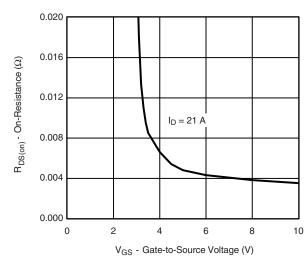


V_{DS} - Drain-to-Source Voltage (V)

Capacitance



On-Resistance vs. Junction Temperature



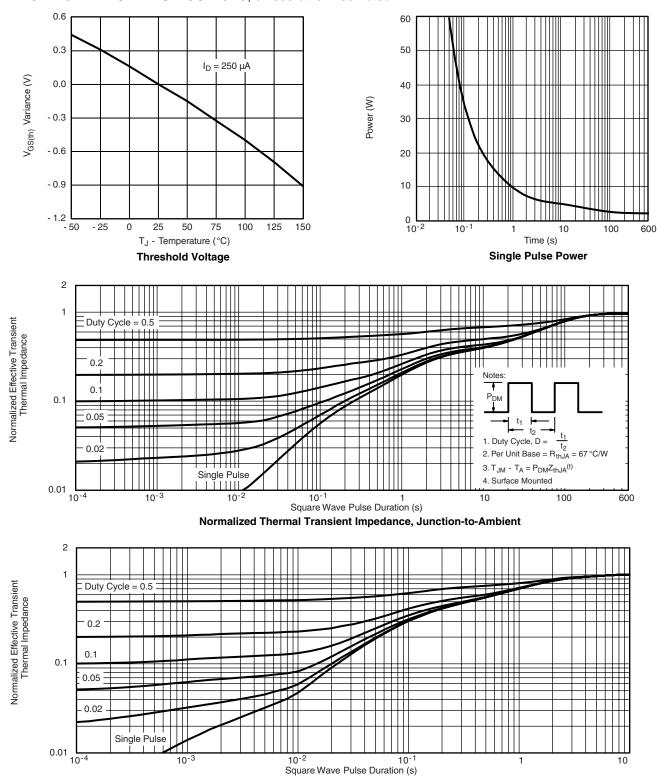
On-Resistance vs. Gate-to-Source Voltage

Is - Source Current (A)

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70687.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	MILLIMETERS INCHES				
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050) BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Bey 11-Sen-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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