N-Channel 80 V (D-S) MOSFET

DESCRIPTION

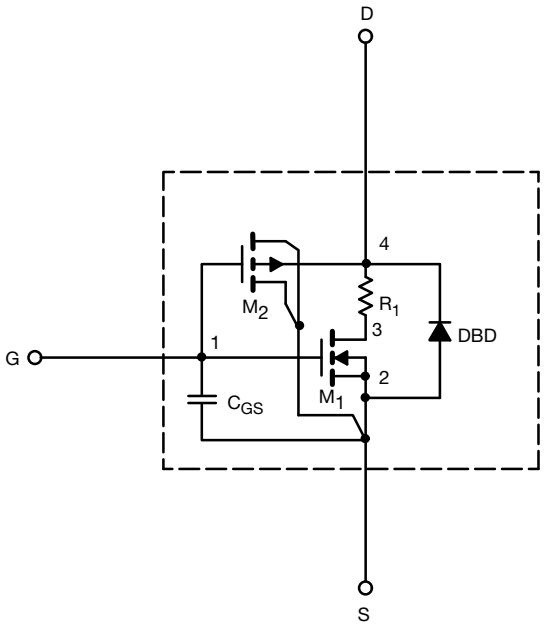
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

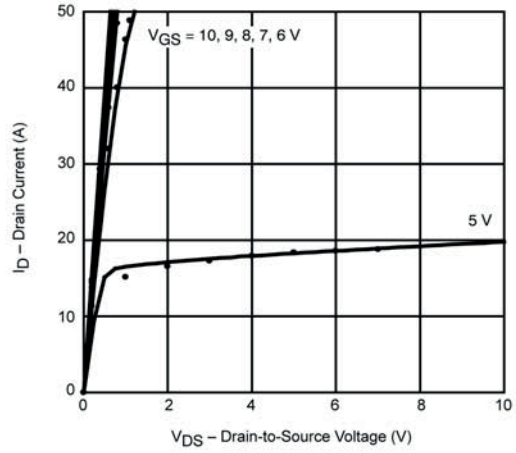
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.6	-	V
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \geq 5$ V, V_{GS} = 10 V	319	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	0.0127	0.0135	Ω
		V_{GS} = 6 V, I_D = 8 A	0.0175	0.0175	
Forward Transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	24	25	S
Diode Forward Voltage [a]	V_{SD}	I_S = 2.8 A, V_{GS} = 0 V	0.83	0.75	V
Dynamic [b]					
Total Gate Charge	Q_g	V_{DS} = 40 V, V_{GS} = 10 V, I_D = 10 A	37	34	nC
Gate-Source Charge	Q_{gs}		7.5	7.5	
Gate-Drain Charge	Q_{gd}		11	11	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 40 V, R_L = 40 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω	18	17	ns
Rise Time	t_r		22	11	
Turn-Off Delay Time	$t_{d(off)}$		30	40	
Fall Time	t_f		45	31	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.8 A, dI/dt = 100 A/µs	40	45	

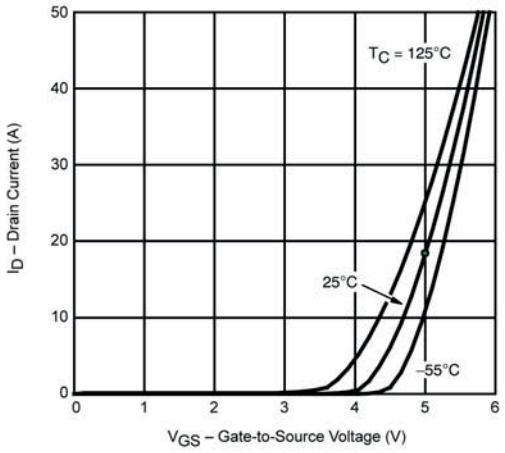
Notes

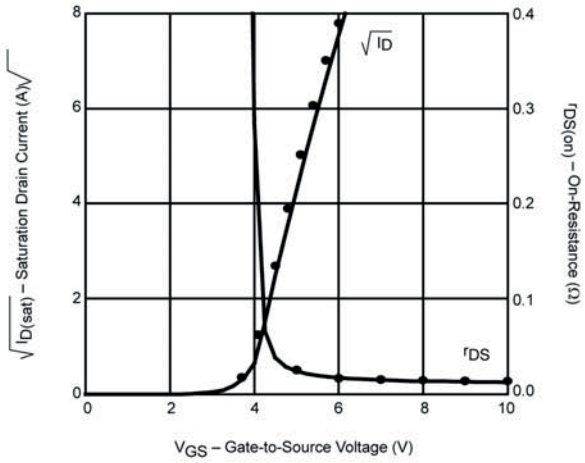
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

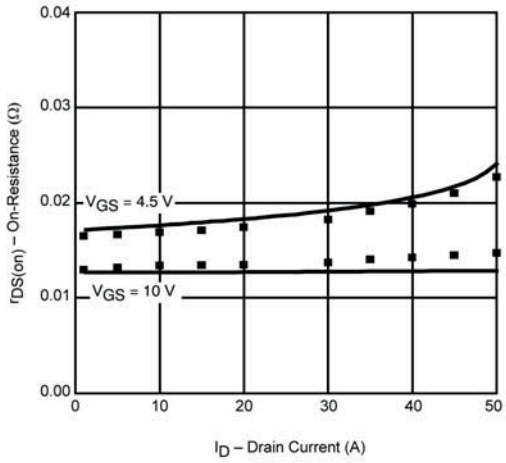
b. Guaranteed by design, not subject to production testing.

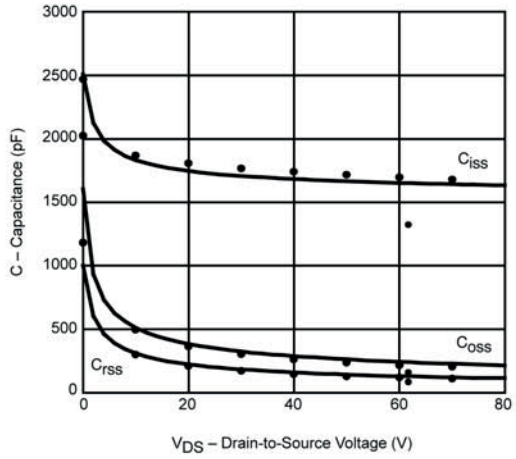
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

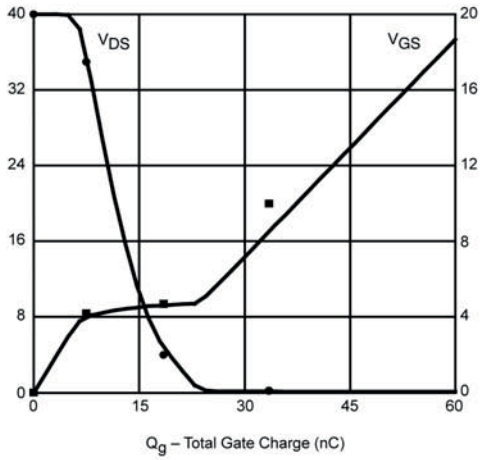












Note

- Dots and squares represent measured data.

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