# N-Channel 20-V (D-S) MOSFET

## CHARACTERISTICS

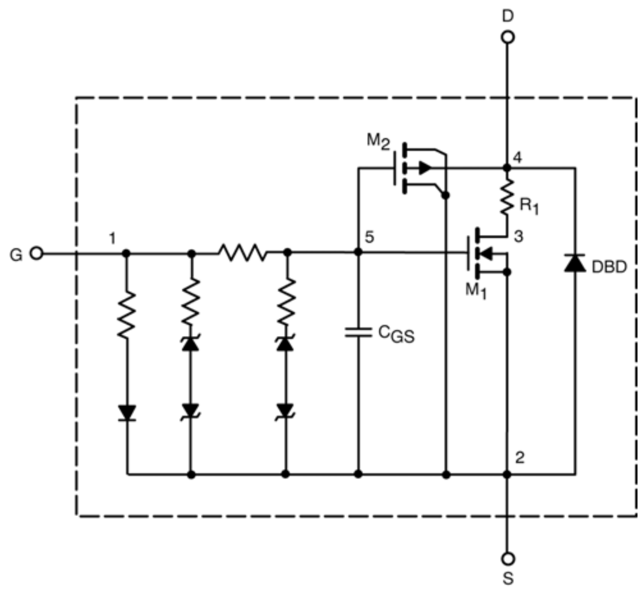
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC

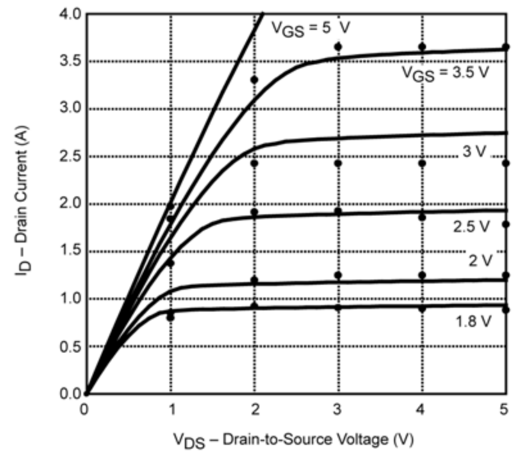


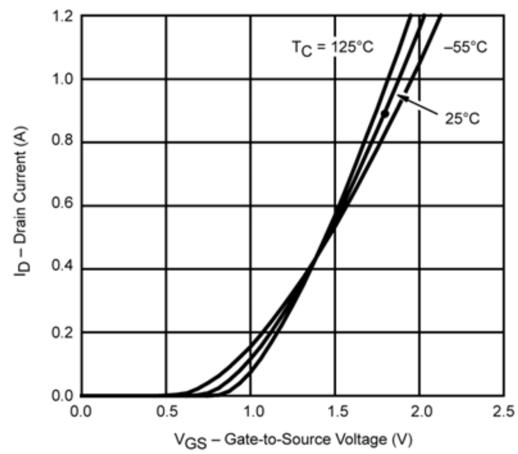

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

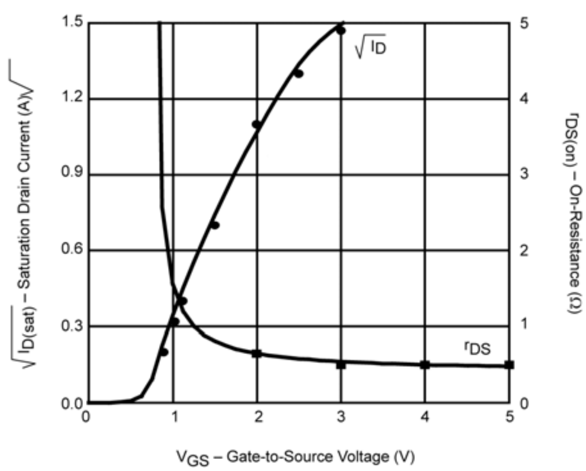
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = VGS, $I_D$ = 250 µA | 0.60 | 0.70 | V |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 4.5 V | 5.5 | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 200 mA | 0.50 | | Ω |
| | | $V_{GS}$ = 2.5 V, $I_D$ =175 mA | 0.58 | | |
| | | $V_{GS}$ = 1.8 V, $I_D$ = 150 mA | 0.70 | | |
| | | $V_{GS}$ = 1.5 V, $I_D$ = 40 mA | 0.78 | | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 200 mA | 0.80 | 0.50 | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 150 mA, $V_{GS}$ = 0 V | 0.70 | | V |
| **Dynamic[b]** | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 150 mA | 0.68 | 0.75 | nC |
| Gate-Source Charge | $Q_{gs}$ | | 0.075 | 0.075 | |
| Gate-Drain Charge | $Q_{gd}$ | | 0.225 | 0.225 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 47 Ω<br>$I_D$ ≅ 200 mA, $V_{GEN}$ = 4.5 V, $R_G$ = 10 Ω | 3 | | ns |
| Rise Time | $t_r$ | | 10 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 18 | | |
| Fall Time | $t_f$ | | 31 | | |

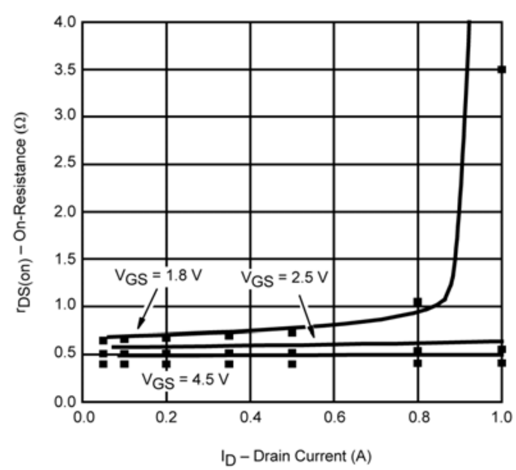
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

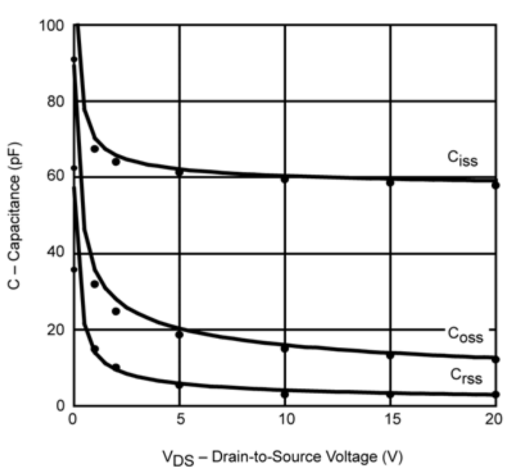
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

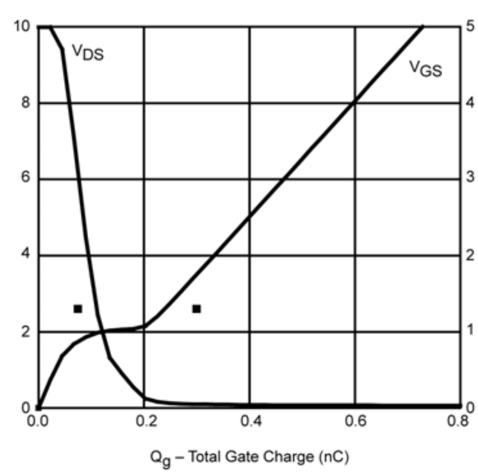



Note: Dots and squares represent measured data.

# Disclaimer

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