**Bi-Directional P-Channel MOSFET/Power Switch**

### FEATURES
- Halogen-free According to IEC 61249-2-21 Definition
- Low $R_{DS(on)}$ Symmetrical P-Channel MOSFET
- Integrated Body Bias For Bi-Directional Blocking
- 2.5 V to 5.5 V Operation
- Exceeds ± 2 kV ESD Protected
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Battery Switching in Multiple Battery Cell Phones, PDAs and PCS Products
- Low Profile, Small Footprint TSOP-6 Package
- Compliant to RoHS Directive 2002/95/EC

### PRODUCT SUMMARY

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$R_{DS(on)}$ ($\Omega$)</th>
<th>$I_D$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>± 7</td>
<td>0.170 at $V_{GS} = -4.5$ V</td>
<td>± 2.4</td>
</tr>
<tr>
<td></td>
<td>0.240 at $V_{GS} = -2.5$ V</td>
<td>± 2.0</td>
</tr>
</tbody>
</table>

### DESCRIPTION

The Si3831DV is a low on-resistance p-channel power MOSFET providing bi-directional blocking and conduction. Bi-directional blocking is facilitated by combining a 4-terminal symmetric p-channel MOSFET with a body bias selector circuit. Circuit operation automatically biases the p-channel body to the most positive source/drain potential thereby maintaining a reverse bias across the diode present between the source/drain terminals. Off-state device blocking characteristics are symmetric, facilitating bi-directional blocking for high-side battery switching in portable products. Gate drive is facilitated by negatively biasing the gate relative to the body potential. The off-state is achieved by biasing the gate to the most positive supply voltage or to the body potential. The Si3831DV is available in a 6-pin TSOP-6 package rated for the -25 °C to 85 °C commercial temperature range.

### APPLICATION CIRCUITS

**Figure 1. Charger Demultiplexing**

**Figure 2. Battery Multiplexing (High-Side Switch)**

Note:
- a. Patents pending.
**Si3831DV**

Vishay Siliconix

**FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION**

![Image of functional block diagram and pin configuration]

**Notes:**
- Bi-directional.
- Surface Mounted on FR4 board, \( t \leq 5 \) s.
- Surface Mounted on FR4 board, Steady-State.

**Ordering Information:** Si3831DV-T1-E3 (Lead (Pb)-free)
Si3831DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

### ABSOLUTE MAXIMUM RATINGS \( T_A = 25 \) °C, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage, Source-Drain Voltage(^a)</td>
<td>( V_{DS} )</td>
<td>- 7.0 to + 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>( V_{SB}, V_{DB}, V_{GB} )</td>
<td>0.3 to - 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Body-Substrate Voltage</td>
<td>( V_{BSUB} )</td>
<td>+ 7.0 to - 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Drain-to-Source Current (( T_J = 150 ) °C)(^a, b)</td>
<td>( I_D )</td>
<td>± 2.4</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>± 2.0</td>
<td>A</td>
</tr>
<tr>
<td>Pulsed Drain-to-Source Current(^a)</td>
<td>( I_{DM} )</td>
<td>± 8</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Power Dissipation(^b)</td>
<td>( P_D )</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td>Operating Junction and Storage Temperature Range</td>
<td>( T_J, T_{stg} )</td>
<td>- 55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage(^a)</td>
<td>( V_{DS} )</td>
<td>- 5.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Gate-Drain, Gate-Source Voltage</td>
<td>( V_{GD}, V_{GS} )</td>
<td>0 to - 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>( V_{SB}, V_{DB}, V_{GB} )</td>
<td>0 to - 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Drain-to-Source Current(^a, b)</td>
<td>( I_{DS} )</td>
<td>± 2.4</td>
<td>A</td>
</tr>
<tr>
<td>Body-Source Current</td>
<td>( I_{BS} )</td>
<td>0 to 10</td>
<td>µA</td>
</tr>
</tbody>
</table>

### THERMAL RESISTANCE RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction-to-Ambient(^b)</td>
<td>( R_{thJA} )</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>125</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**Notes:**
- Bi-directional.
- Surface Mounted on FR4 board, \( t \leq 5 \) s.
- Surface Mounted on FR4 board, Steady-State.
**SPECIFICATIONS**  \( V_{BS} = 0 \text{ V}, \ T_J = 25 \degree \text{C}, \text{ unless otherwise noted} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_{GS(th)} )</td>
<td>( V_{DS} = V_{GS}, \ I_D = -250 \mu A )</td>
<td>-0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gate-Body Leakage</td>
<td>( I_{GSS} )</td>
<td>( V_{DS} = 0 \text{ V}, \ V_{GS} = -5.5 \text{ V} \text{ to } +0.3 \text{ V} )</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DSS} )</td>
<td>( V_{DS} = -5.5 \text{ V}, \ V_{GS} = 0 \text{ V}, \ V_{SB} = 0 \text{ V} )</td>
<td>-1</td>
<td></td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DS} = -5.5 \text{ V}, \ V_{GS} = 0 \text{ V}, \ V_{SB} = 0 \text{ V}, \ T_J = 70 \degree \text{C} )</td>
<td>-5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-State Drain Current(^a)</td>
<td>( I_{D(on)} )</td>
<td>( V_{DS} = -3 \text{ V}, \ V_{GS} = -4.5 \text{ V} )</td>
<td>-8</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DS} = -3 \text{ V}, \ V_{GS} = -2.5 \text{ V} )</td>
<td>-3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-Source On-State Resistance(^a)</td>
<td>( R_{DS(on)} )</td>
<td>( V_{GS} = -4.5 \text{ V}, \ I_D = -2.4 \text{ A} )</td>
<td>0.130</td>
<td>0.170</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{GS} = -2.5 \text{ V}, \ I_D = -2.0 \text{ A} )</td>
<td>0.180</td>
<td>0.240</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dynamic(^b)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>( Q_g )</td>
<td>( V_{DS} = -5 \text{ V}, \ V_{GS} = -4.5 \text{ V}, \ I_D = -2.4 \text{ A} )</td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Gate-Source Charge</td>
<td>( Q_{gs} )</td>
<td></td>
<td>0.23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Drain Charge</td>
<td>( Q_{gd} )</td>
<td></td>
<td>0.14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_{(on)} )</td>
<td>( V_{DD} = -3 \text{ V}, \ R_L = 3 \Omega )</td>
<td>12</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_D \cong -1.0 \text{ A}, \ V_{GEN} = -4.5 \text{ V}, \ R_g = 6 \Omega )</td>
<td>55</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td></td>
<td>90</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_{(off)} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_f )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

a. Pulse test; pulse width \( \leq 300 \mu \text{ s}, \text{ duty cycle } \leq 2 \% \).
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**GATE BUFFER REFERENCE**

Figure 5. Gate Buffer Referenced to Most Positive Supply

Figure 6. Gate Buffer Referenced to Body Bias Pin
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

On-Resistance vs. Drain Current

V_T = 5 V thru 3 V
V_T = 2.5 V
V_T = 2 V
V_T = 1.5 V
V_T = 1 V

V_DS - Drain-to-Source Voltage (V)

Transfer Characteristics

Gate Charge

Capacitance

On-Resistance vs. Junction Temperature (Normalized)

Gate Charge

On-Resistance vs. Junction Temperature

V_GS = 5 V thru 3 V
V_GS = 2.5 V
V_GS = 2 V
V_GS = 1.5 V
V_GS = 1 V

V_DS - Drain-to-Source Voltage (V)

V_GS - Gate-to-Source Voltage (V)

C - Capacitance (pF)

R_DS(on) - On-Resistance (Ω)

ID - Drain Current (A)

Q_G - Total Gate Charge (nC)

V_GS = 4.5 V
ID = 2.4 A

TJ - Junction Temperature (°C)

R_DS(on) - On-Resistance (Normalized)

TC = -55 °C
25 °C
125 °C

ID - Drain Current (A)

V_DS - Drain-to-Source Voltage (V)

V_DS = 3 V
ID = 2.4 A

V_GS = 4.5 V
ID = 2.4 A

V_GS = 2.5 V
ID = 2.4 A

V_DS = 25 °C
V_DS = 2.5 °C
V_DS = 125 °C
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power

Normalized Thermal Transient Impedance, Junction-to-Ambient

Notes:
1. Duty Cycle, D = \( \frac{t_1}{T} \)
2. Per Unit Base = \( R_{thJA} = 80 °C/W \)
3. \( T_{JM} \cdot T_A = P_{DM}^2 C_{JA}^{(1)} \)
4. Surface Mounted
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

![Graph showing Bi-Directional Blocking Drain-Source Voltage](image)

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