**PRODUCT SUMMARY**

<table>
<thead>
<tr>
<th>$V_{DS}$ (V)</th>
<th>$R_{DS(on)}$ (Ω)</th>
<th>$I_D$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>± 7</td>
<td>0.170 at $V_{GS} = -4.5$ V</td>
<td>± 2.4</td>
</tr>
<tr>
<td></td>
<td>0.240 at $V_{GS} = -2.5$ V</td>
<td>± 2.0</td>
</tr>
</tbody>
</table>

**FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Low $R_{DS(on)}$ Symmetrical P-Channel MOSFET
- Integrated Body Bias For Bi-Directional Blocking
- 2.5 V to 5.5 V Operation
- Exceeds ± 2 kV ESD Protected
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Battery Switching in Multiple Battery Cell Phones, PDAs and PCS Products
- Low Profile, Small Footprint TSOP-6 Package
- Compliant to RoHS Directive 2002/95/EC

**DESCRIPTION**

The Si3831DV is a low on-resistance p-channel power MOSFET providing bi-directional blocking and conduction. Bi-directional blocking is facilitated by combining a 4-terminal symmetric p-channel MOSFET with a body bias selector circuit\(^a\). Circuit operation automatically biases the p-channel body to the most positive source/drain potential thereby maintaining a reverse bias across the diode present between the source/drain terminals. Off-state device blocking characteristics are symmetric, facilitating bi-directional blocking for high-side battery switching in portable products. Gate drive is facilitated by negatively biasing the gate relative to the body potential. The off-state is achieved by biasing the gate to the most positive supply voltage or to the body potential. The Si3831DV is available in a 6-pin TSOP-6 package rated for the -25 °C to 85 °C commercial temperature range.

**APPLICATION CIRCUITS**

**Note:**

\(^a\) Patents pending.
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

![Functional Block Diagram](image)

Notes:
- Bi-directional.
- Surface Mounted on FR4 board, $t \leq 5$ s.
- Surface Mounted on FR4 board, Steady-State.

Figure 3.

TSOP-6 Top View

Figure 4.

Ordering Information:
- Si3831DV-T1-E3 (Lead (Pb)-free)
- Si3831DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

### ABSOLUTE MAXIMUM RATINGS $T_A = 25 \degree C$, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage, Source-Drain Voltage$^a$</td>
<td>$V_{DS}$</td>
<td>- 7.0 to + 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>$V_{SB}, V_{DB}, V_{GB}$</td>
<td>0.3 to - 7.0</td>
<td></td>
</tr>
<tr>
<td>Body-Substrate Voltage</td>
<td>$V_{BSUB}$</td>
<td>+ 7.0 to - 0.3</td>
<td></td>
</tr>
<tr>
<td>Continuous Drain-to-Source Current ($T_J = 150 \degree C$)$^{a, b}$</td>
<td>$I_D$</td>
<td>± 2.4</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>± 2.0</td>
<td></td>
</tr>
<tr>
<td>Pulsed Drain-to-Source Current$^a$</td>
<td>$I_{DM}$</td>
<td>± 8</td>
<td></td>
</tr>
<tr>
<td>Maximum Power Dissipation$^b$</td>
<td>$P_D$</td>
<td>1.5</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>Operating Junction and Storage Temperature Range</td>
<td>$T_J, T_{stg}$</td>
<td>- 55 to 150</td>
<td>\degree C</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-Source Voltage$^a$</td>
<td>$V_{DS}$</td>
<td>- 5.5 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>Gate-Drain, Gate-Source Voltage</td>
<td>$V_{GD}, V_{GS}$</td>
<td>0 to - 5.5</td>
<td></td>
</tr>
<tr>
<td>Source-Body, Drain-Body, Gate-Body Voltage</td>
<td>$V_{SB}, V_{DB}, V_{GB}$</td>
<td>0 to - 5.5</td>
<td></td>
</tr>
<tr>
<td>Drain-to-Source Current$^b, c$</td>
<td>$I_{DS}$</td>
<td>± 2.4</td>
<td>A</td>
</tr>
<tr>
<td>Body-Source Current</td>
<td>$I_{BS}$</td>
<td>0 to 10</td>
<td>\mu A</td>
</tr>
</tbody>
</table>

### THERMAL RESISTANCE RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Junction-to-Ambient$^b$</td>
<td>$R_{JA}$</td>
<td>80</td>
<td>\degree C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>125</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- a. Bi-directional.
- b. Surface Mounted on FR4 board, $t \leq 5$ s.
- c. Surface Mounted on FR4 board, Steady-State.
Si3831DV
Vishay Siliconix

SPECIFICATIONS  $V_{BS} = 0 \text{ V}, \; T_J = 25 \degree \text{C}$, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>$V_{GS(th)}$</td>
<td>$V_{DS} = V_{GS}, ; I_D = - 250 \mu A$</td>
<td>- 0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gate-Body Leakage</td>
<td>$I_{GSS}$</td>
<td>$V_{DS} = 0 \text{ V}, ; V_{GS} = - 5.5 \text{ V} \text{ to } + 0.3 \text{ V}$</td>
<td>± 100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>$I_{DSS}$</td>
<td>$V_{DS} = - 5.5 \text{ V}, ; V_{GS} = 0 \text{ V}, ; V_{SB} = 0 \text{ V}$</td>
<td>- 1</td>
<td></td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = - 5.5 \text{ V}, ; V_{GS} = 0 \text{ V}, ; V_{SB} = 0 \text{ V}, ; T_J = 70 \degree \text{C}$</td>
<td>- 5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-State Drain Current$^a$</td>
<td>$I_D(on)$</td>
<td>$V_{DS} = - 3 \text{ V}, ; V_{GS} = - 4.5 \text{ V}$</td>
<td>- 8</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = - 3 \text{ V}, ; V_{GS} = - 2.5 \text{ V}$</td>
<td></td>
<td></td>
<td>- 3</td>
<td></td>
</tr>
<tr>
<td>Drain-Source On-State Resistance$^a$</td>
<td>$R_{DS(on)}$</td>
<td>$V_{GS} = - 4.5 \text{ V}, ; I_D = - 2.4 \text{ A}$</td>
<td>0.130</td>
<td>0.170</td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = - 2.5 \text{ V}, ; I_D = - 2.0 \text{ A}$</td>
<td>0.180</td>
<td>0.240</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic$^b$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>$Q_g$</td>
<td>$V_{DS} = - 5 \text{ V}, ; V_{GS} = - 4.5 \text{ V}, ; I_D = - 2.4 \text{ A}$</td>
<td>2.0</td>
<td>4.0</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>Gate-Source Charge</td>
<td>$Q_{gs}$</td>
<td></td>
<td>0.23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Drain Charge</td>
<td>$Q_{gd}$</td>
<td></td>
<td>0.14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>$t_{(on)}$</td>
<td></td>
<td>12</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>$t_r$</td>
<td>$V_{DD} = - 3 \text{ V}, ; R_L = 3 \Omega$</td>
<td>55</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>$t_{(off)}$</td>
<td>$I_D = - 1.0 \text{ A}, ; V_{GEN} = - 4.5 \text{ V}, ; R_g = 6 \Omega$</td>
<td>90</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>$t_f$</td>
<td></td>
<td>85</td>
<td>170</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:

a. Pulse test; pulse width $\leq 300 \mu \text{ s}$, duty cycle $\leq 2 \%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GATE BUFFER REFERENCE

Figure 5. Gate Buffer Referenced to Most Positive Supply

Figure 6. Gate Buffer Referenced to Body Bias Pin
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

- **On-Resistance vs. Drain Current**
  - $V_{DS}$ - Drain-to-Source Voltage (V)
  - $I_D$ - Drain Current (A)
  - $V_{GS} = 5 \text{ V} \text{ thru } 3 \text{ V}$
  - $1.5 \text{ V}$
  - $2 \text{ V}$
  - $2.5 \text{ V}$

**Gate Charge**

- $Q_g$ - Total Gate Charge (nC)
- $V_{GS} = 4.5 \text{ V}$
- $I_D = 2.4 \text{ A}$

**Transfer Characteristics**

- **Capacitance**
  - $V_{DS}$ - Drain-to-Source Voltage (V)
  - $C$ - Capacitance (pF)
  - $V_{GS} = 4.5 \text{ V}$
  - $I_D = 2.4 \text{ A}$

**On-Resistance vs. Junction Temperature**

- $R_{DS(on)}$ - On-Resistance (Ω)
- $T_J$ - Junction Temperature (°C)
- $V_{GS} = 4.5 \text{ V}$
- $I_D = 2.4 \text{ A}$

**Capacitance**

- $C_{GSS}$, $C_{ISS}$, $C_{RSS}$

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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Source-Drain Diode Forward Voltage**

- **Threshold Voltage**
  - $V_{SD}$: Source-to-Drain Voltage (V)
  - $I_S$: Source Current (A)
  - $T_J$: Temperature (°C)

- **Normalized Effective Transient Thermal Impedance**
  - **Normalized Thermal Transient Impedance, Junction-to-Ambient**

- **On-Resistance vs. Gate-to-Source Voltage**
  - $R_{DS(on)}$: On-Resistance (Ω)
  - $V_{GS}$: Gate-to-Source Voltage (V)

- **Single Pulse Power**
  - $P_{DM}$: Power (W)
  - $D$: Duty Cycle
  - $P_{Ja}$: Per Unit Base = $R_{thJA} = 80$ °C/W
  - $T_JM$: $T_A = P_{DM}C_JA$ (°)

Notes:
1. Surface Mounted
2. Per Unit Base = $R_{thJA} = 80$ °C/W
3. $T_JM - T_A = P_{DM}C_JA$
4. Surface Mounted
Si3831DV
Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

![Graph showing Bi-Directional Blocking Drain-Source Voltage](image-url)

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