Bi-Directional P-Channel MOSFET/Power Switch

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
± 7	0.170 at V_{GS} = - 4.5 V	± 2.4
	0.240 at V_{GS} = - 2.5 V	± 2.0

DESCRIPTION

The Si3831DV is a low on-resistance p-channel power MOSFET providing bi-directional blocking and conduction. Bi-directional blocking is facilitated by combining a 4-terminal symmetric p-channel MOSFET with a body bias selector circuit[a]. Circuit operation automatically biases the p-channel body to the most positive source/drain potential thereby maintaining a reverse bias across the diode present between the source/drain terminals. Off-state device blocking characteristics are symmetric, facilitating bi-directional blocking for high-side battery switching in portable products. Gate drive is facilitated by negatively biasing the gate relative to the body potential. The off-state is achieved by biasing the gate to the most positive supply voltage or to the body potential. The Si3831DV is available in a 6-pin TSOP-6 package rated for the - 25 °C to 85 °C commercial temperature range.

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low $R_{DS(on)}$ Symmetrical P-Channel MOSFET
- Integrated Body Bias For Bi-Directional Blocking
- 2.5 V to 5.5 V Operation
- Exceeds ± 2 kV ESD Protected
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Battery Switching in Multiple Battery Cell Phones, PDAs and PCS Products
- Low Profile, Small Footprint TSOP-6 Package
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATION CIRCUITS

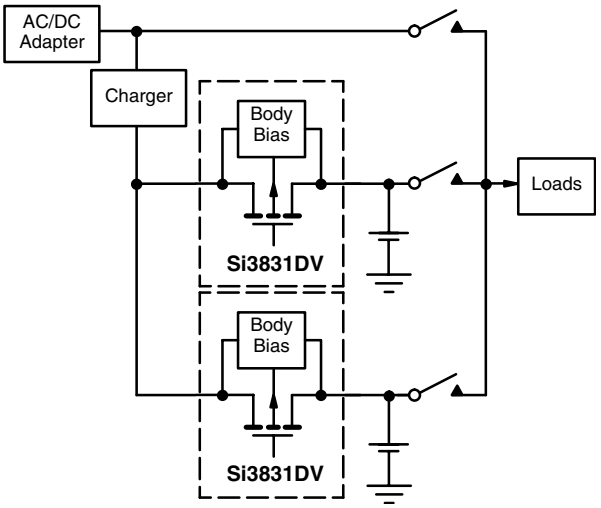


Figure 1. Charger Demultiplexing

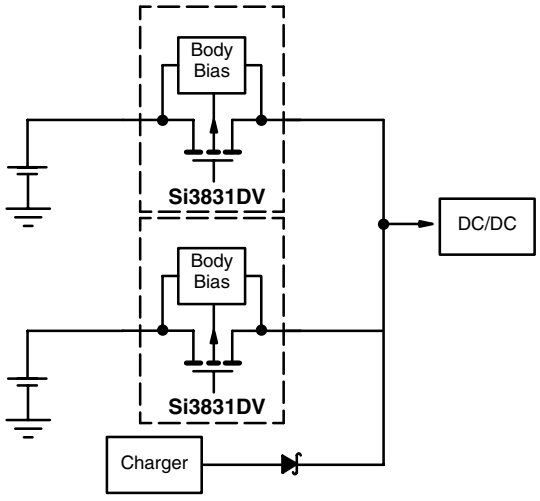


Figure 2. Battery Multiplexing (High-Side Switch)

Note:
a. Patents pending.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

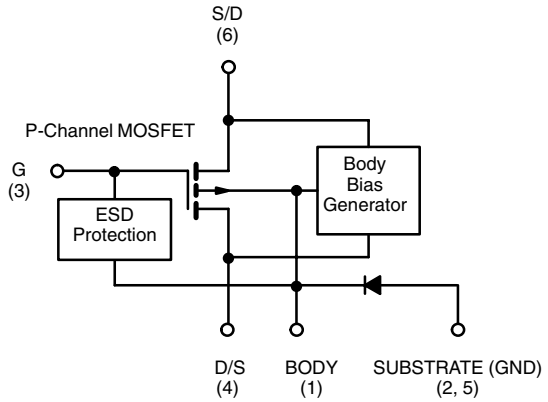


Figure 3.

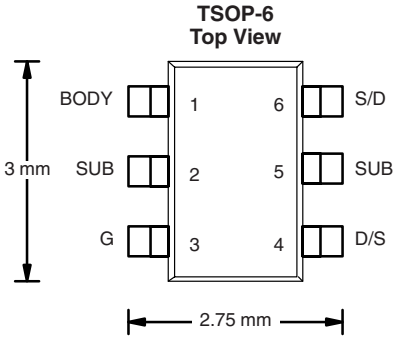


Figure 4.

Ordering Information: Si3831DV-T1-E3 (Lead (Pb)-free)
Si3831DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage, Source-Drain Voltage[a]		V_{DS}	- 7.0 to + 7.0	V
Source-Body, Drain-Body, Gate-Body Voltage		V_{SB}, V_{DB}, V_{GB}	0.3 to - 7.0	
Body-Substrate Voltage		V_{BSUB}	+ 7.0 to - 0.3	
Continuous Drain-to-Source Current (T_J = 150 °C)[a, b]	T_A = 25 °C	I_D	± 2.4	A
	T_A = 70 °C		± 2.0	
Pulsed Drain-to-Source Current[a]		I_{DM}	± 8	
Maximum Power Dissipation[b]	T_A = 25 °C	P_D	1.5	W
	T_A = 70 °C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

RECOMMENDED OPERATING RANGE			
Parameter	**Symbol**	**Range**	**Unit**
Drain-Source Voltage[a]	V_{DS}	- 5.5 to 5.5	V
Gate-Drain, Gate-Source Voltage	V_{GD}, V_{GS}	0 to - 5.5	
Source-Body, Drain-Body, Gate-Body Voltage	V_{SB}, V_{DB}, V_{GB}	0 to - 5.5	
Drain-to-Source Current[a, b]	I_{DS}	± 2.4	A
Body-Source Current	I_{BS}	0 to 10	µA

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Maximum Junction-to-Ambient[b]	R_{thJA}	80	°C/W
		125	

Notes:
a. Bi-directional.
b. Surface Mounted on FR4 board, t ≤ 5 s.
c. Surface Mounted on FR4 board, Steady-State.

SPECIFICATIONS V_{BS} = 0 V, T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.4			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = - 5.5 V to + 0.3 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 5.5 V, V_{GS} = 0 V, V_{SB} = 0 V			- 1	µA
		V_{DS} = - 5.5 V, V_{GS} = 0 V, V_{SB} = 0 V, T_J = 70 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 3 V, V_{GS} = - 4.5 V	- 8			A
		V_{DS} = - 3 V, V_{GS} = - 2.5 V	- 3			
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 2.4 A		0.130	0.170	Ω
		V_{GS} = - 2.5 V, I_D = - 2.0 A		0.180	0.240	
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 5 V, V_{GS} = - 4.5 V, I_D = - 2.4 A		2.0	4.0	nC
Gate-Source Charge	Q_{gs}			0.23		
Gate-Drain Charge	Q_{gd}			0.14		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 3 V, R_L = 3 Ω I_D ≅ - 1.0 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		12	25	ns
Rise Time	t_r			55	110	
Turn-Off Delay Time	$t_{d(off)}$			90	180	
Fall Time	t_f			85	170	

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GATE BUFFER REFERENCE

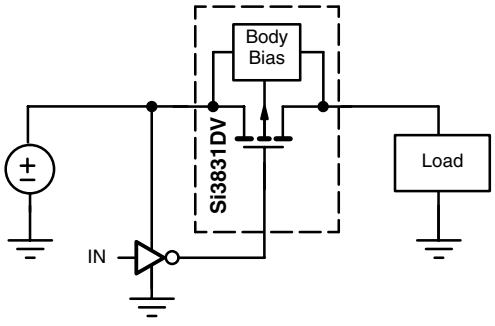


Figure 5. Gate Buffer Referenced to Most Positive Supply

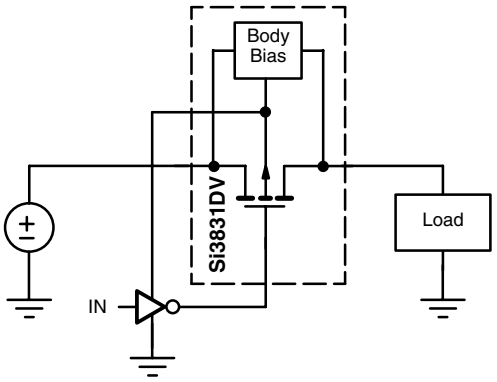
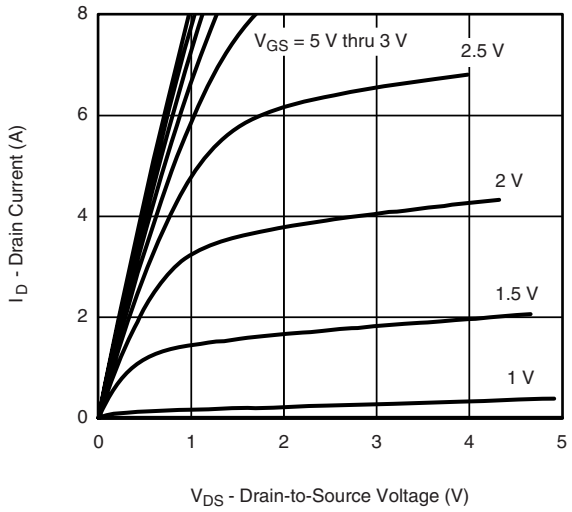
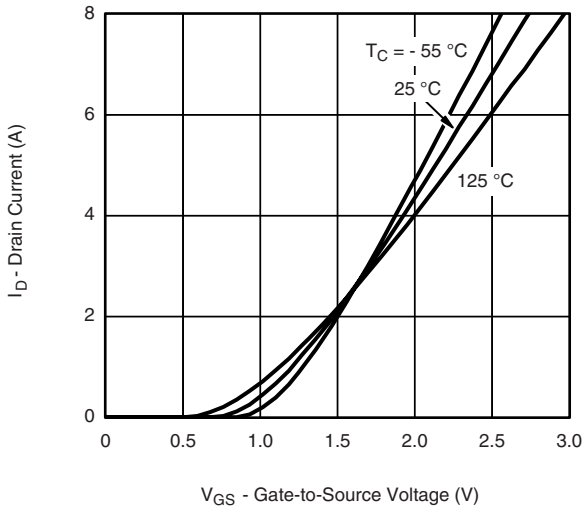


Figure 6. Gate Buffer Referenced to Body Bias Pin

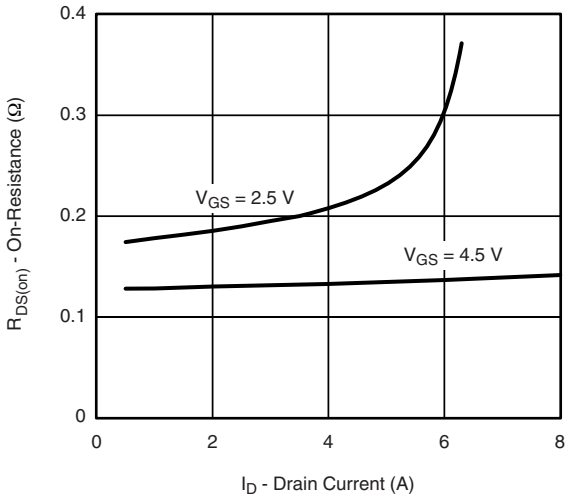
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



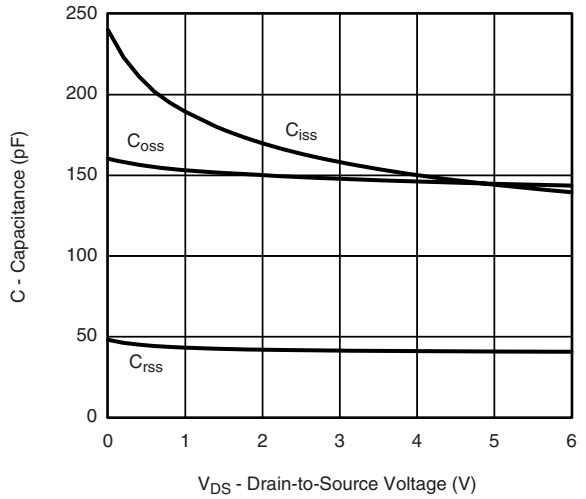
Output Characteristics



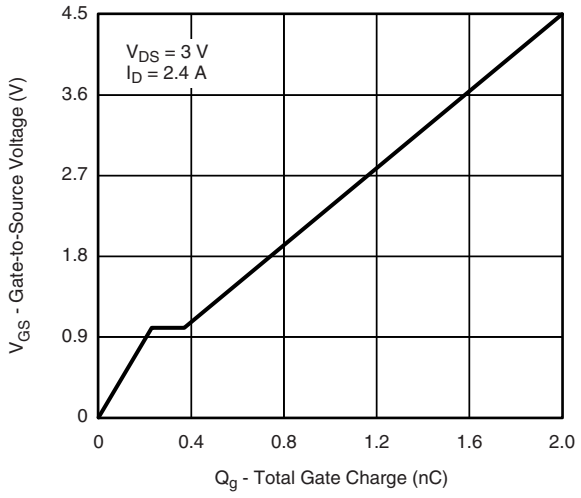
Transfer Characteristics



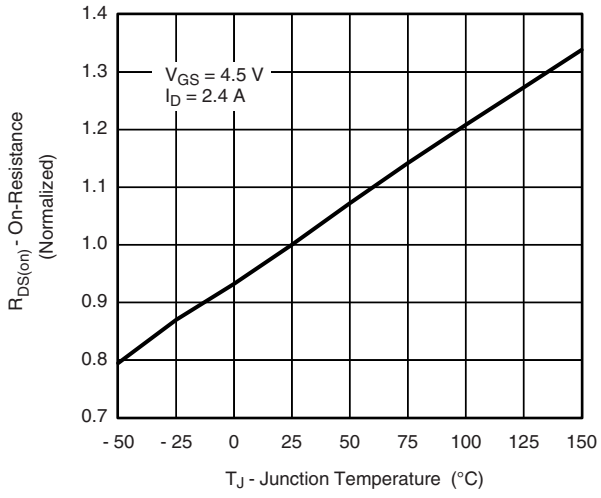
On-Resistance vs. Drain Current



Capacitance

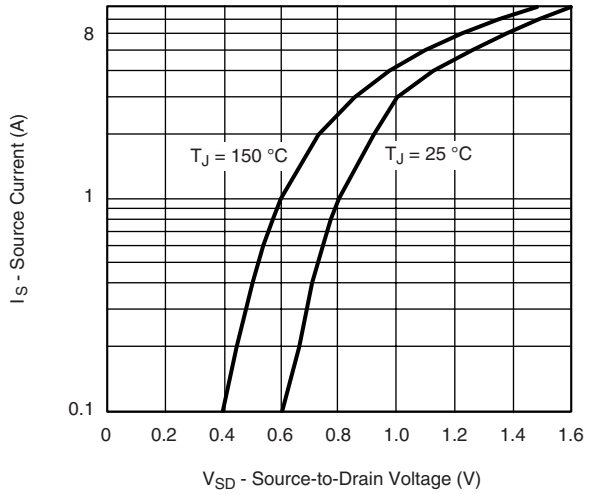


Gate Charge

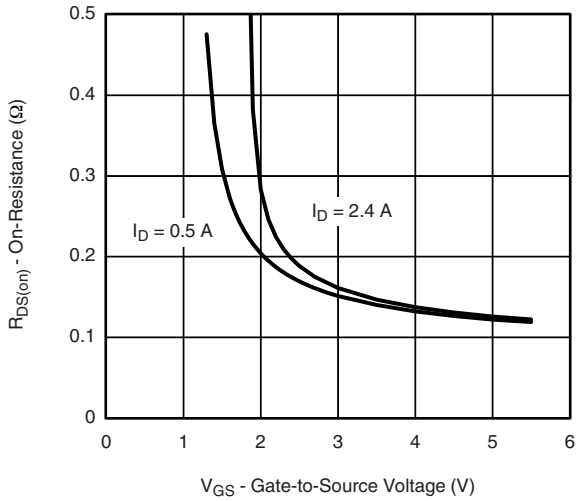


On-Resistance vs. Junction Temperature

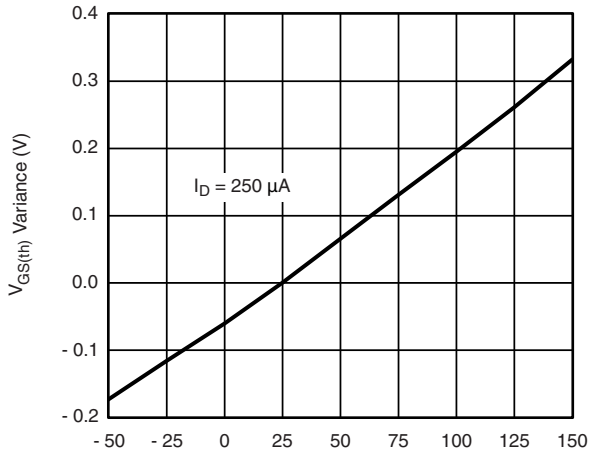
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



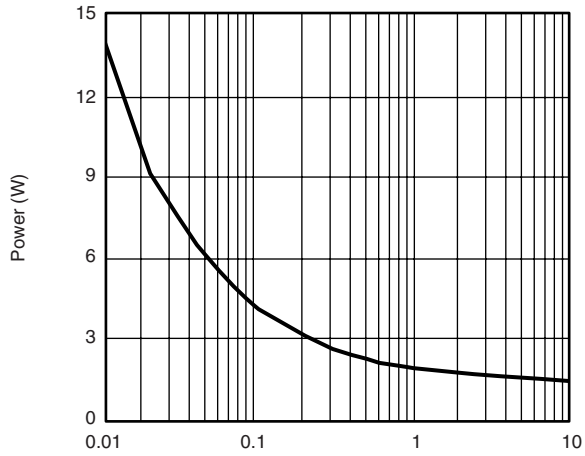
Source-Drain Diode Forward Voltage



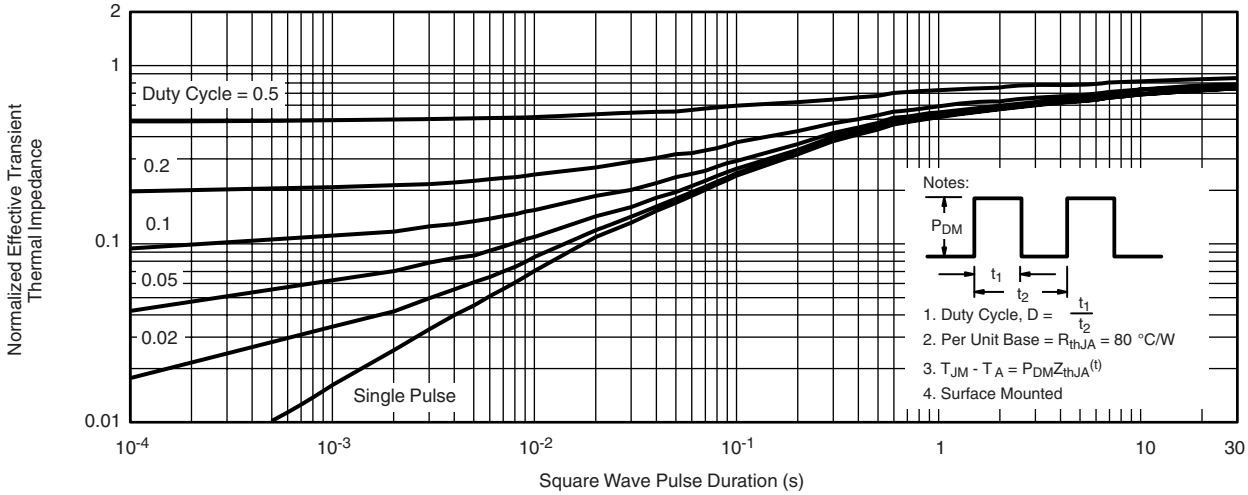
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

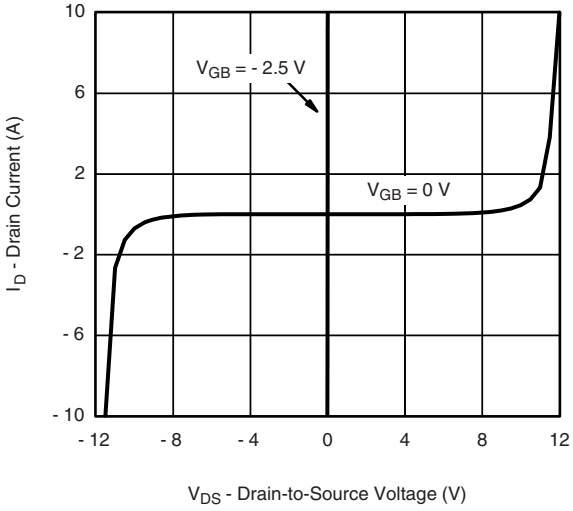


Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Bi-Directional Blocking Drain-Source Voltage

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