High Frequency Programmable Topology Controller

FEATURES

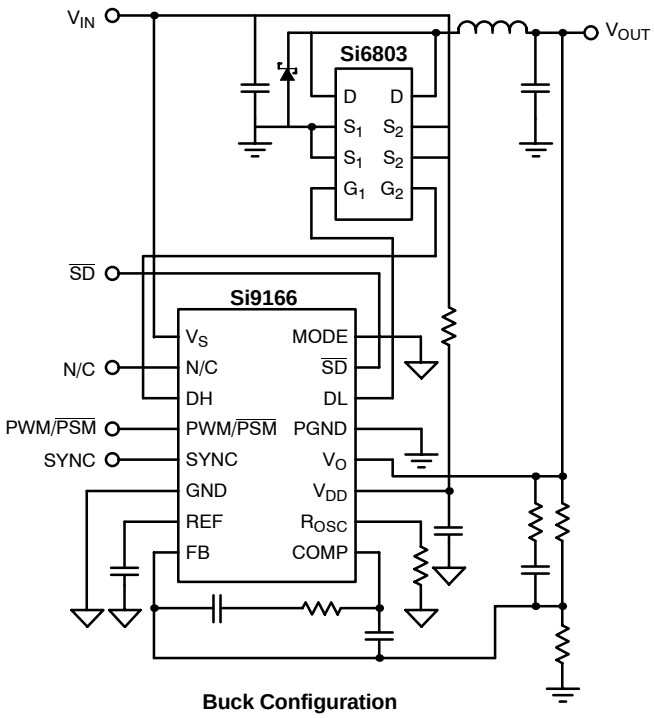
- Buck or Boost Configuration
- Voltage Mode Control
- 2.7-V to 6-V Input Voltage Range for V_{DD} and V_S
- Programmable PWM/$\overline{PSM}$ Control
  - Up to 2-MHz Switching Frequency in PWM
  - Synchronous Rectification in PWM
  - Less than 200-μA I_{DD} in PSM
- Integrated UVLO and POR
- Integrated Soft-Start
- Synchronization
- Shutdown Current <1 μA

DESCRIPTION

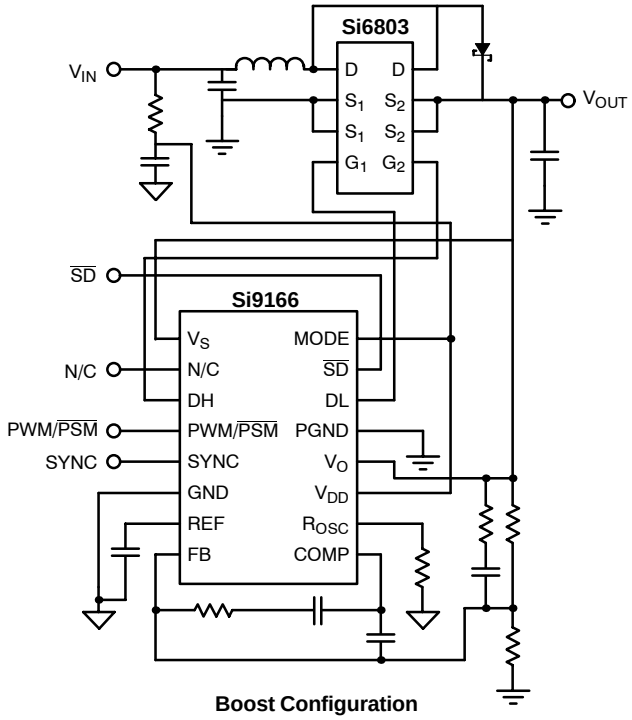
The Si9166 is a programmable topology controller for today's continuous changing portable electronic market. Si9166 provides flexibility of utilizing various battery configurations and chemistries such as NiCd, NiMhy, or Li+ with input voltage range of 2.7 V to 6 V. An additional flexibility is provided with topology programmability to power multiple loads such as power amplifiers, microcontrollers, or baseband logic IC's. The converters can be programmed to be synchronous Buck or Boost topology. For ultra-high efficiency, converters are designed to operate in synchronous rectified PWM mode under full load while transforming into externally controlled pulse skipping mode (PSM) under light load. All these features are provided by the Si9166 without sacrificing system integration requirements of fitting these circuits into ever demanding smaller and smaller space. The Si9166 is capable of switching up to 2 MHz to minimize the output inductor and capacitor size in order to decrease the overall converter size.

The Si9166 is available in both standard and lead (Pb)-free TSSOP-16 pin packages and specified to operate over the industrial temperature range of –25°C to 85°C.

TYPICAL APPLICATION CIRCUITS



Buck Configuration



Boost Configuration

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V_{DD} . . . . . 6.5 V
MODE, PWM/$\overline{PSM}$, SYNC, $\overline{SD}$, V_{REF}, R_{OSC}
COMP, FB . . . . . –0.3 V to V_{DD} + 0.3 V
V_O . . . . . –0.3 V to V_S + 0.3 V
PGND . . . . . ±0.3 V
Voltages Referenced to PGND
V_S. . . . . 6.5 V
DH, DL . . . . . –0.3 V to V_S + 0.3 V

Peak Output Current (DH, DL) . . . . . 1.5 A
Storage Temperature . . . . . –65°C to 150°C
Operating Junction Temperature . . . . . 150°C
Power Dissipation (Package)[a]
16-Pin TSSOP (Q Suffix)[b] . . . . . 925 mW
Thermal Impedance (θ_{JA})
16-Pin TSSOP . . . . . 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Voltages Referenced to AGND
V_{DD} . . . . . 2.7 V to 6 V
MODE, PWM/$\overline{PSM}$, SYNC, $\overline{SD}$ . . . . . 0 V to V_{DD}
Voltages Referenced to PGND
V_S . . . . . 2.7 V to 6 V

F_{osc} . . . . . 200 kHz to 2 MHz
R_{osc} . . . . . 25 kΩ to 300 kΩ
V_{REF} Capacitor . . . . . 0.1 µF

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.7 V ≤ V_{DD}, V_S ≤ 6 V	Limits Min[a]	Typ[b]	Max[a]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = 0A	1.268	1.3	1.332	V
		I_{REF} = 0, T_A = 25°C	1.280	1.3	1.320	
Load Regulation	ΔV_{REF}	V_{DD} = 3.3 V, –500 µA < I_{REF} <0		3		mV
Power Supply Rejection	P_{SRR}			60		dB
UVLO						
Under Voltage Lockout (turn-on)	V_{UVLOLH}		2.3	2.4	2.5	V
Hysteresis	V_{HYS}	V_{UVLOLH} – V_{UVLOHL}		0.1		
Soft-Start Tim						
SS time	tss			6		mS
Mode						
Logic High	V_{IH}		0.7 V_{DD}			V
Logic Low	V_{IL}				0.3 V_{DD}	
Input Current	I_L		–1.0		1.0	µA
$\overline{SD}$, SYNC, PWM/$\overline{PSM}$						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	
Input Current	I_L		–1.0		1.0	µA

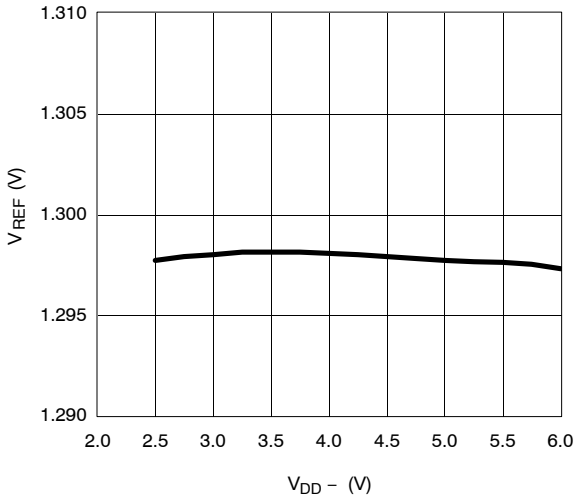
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.7 V ≤ V_{DD}, V_S ≤ 6 V	Limits			Unit
			Min[a]	Typ[b]	Max[a]	
Oscillator						
Maximum Frequency	F_{OSC}		2			MHz
Accuracy		Nominal 1.60 MHz, R_{OSC} = 30 kΩ	−20		20	%
Maximum Duty Cycle—Buck	D_{MAX}	F_{sw} = 2 MHz (non LDO mode)	75	85		
Maximum Duty Cycle—Boost		F_{sw} = 2 MHz	52	65		
SYNC Range	F_{SYNC}/F_{OSC}		1.2		1.5	
SYNC Low Pulse Width			50			ns
SYNC High Pulse Width			50			
SYNC t_r, t_f					50	
Error Amplifier						
Input Bias Current	I_{BIAS}	V_{FB} = 1.4 V	−1		1	µA
Open Loop Voltage Gain	A_{VOL}		50	60		dB
FB Threshold	V_{FB}	T_A = 25°C	1.270	1.30	1.330	V
			1.258	1.30	1.342	
Unity Gain BW	BW			2		MHz
Output Current	I_{EA}	Source (V_{FB} = 1.05 V), V_{COMP} = 0.75 V		−3	−1	mA
		Sink (V_{FB} = 1.55 V), V_{COMP} = 0.75 V	1	3		
Power Supply Rejection	PSRR			60		dB
Output Drive (DH and DL)						
Output High Voltage	V_{OH}	V_S = 3.3 V, I_{OUT} = −20 mA	3.18	3.24		V
Output Low Voltage	V_{OL}	V_S = 3.3 V, I_{OUT} = 20 mA		0.06	0.12	
Peak Output Source	I_{SOURCE}	V_S = 3.3 V, DH = DL = V_S/2		−750	−500	mA
Peak Output Sink	I_{SINK}		500	750		
Break-Before-Make	t_{BBM}	V_S = V_{DD} = 3.3 V		30		ns
Supply						
Normal Mode	I_{DD}	V_{DD} = 3.3 V, F_{OSC} = 2 MHz		500	750	µA
$\overline{PSM}$ Mode		V_{DD} = 3.3 V		180	250	
Shutdown Mode		V_{DD} = 3.3 V, $\overline{SD}$ = 0 V			1	

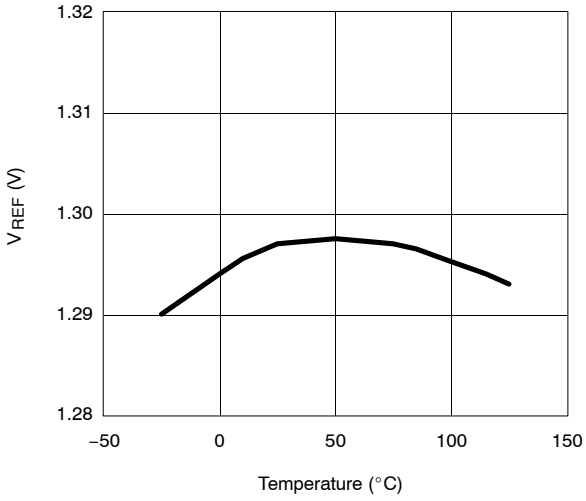
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

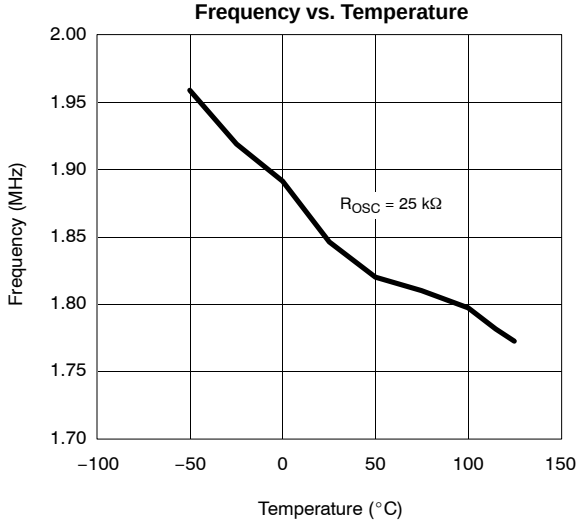
V_{REF} vs. V_{DD}



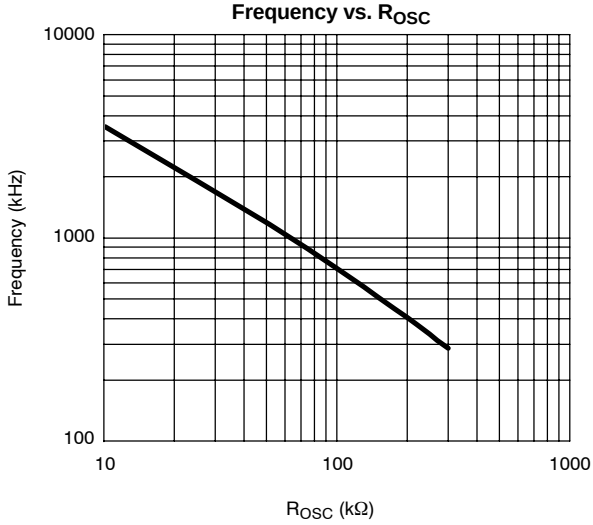
V_{REF} vs. Temperature



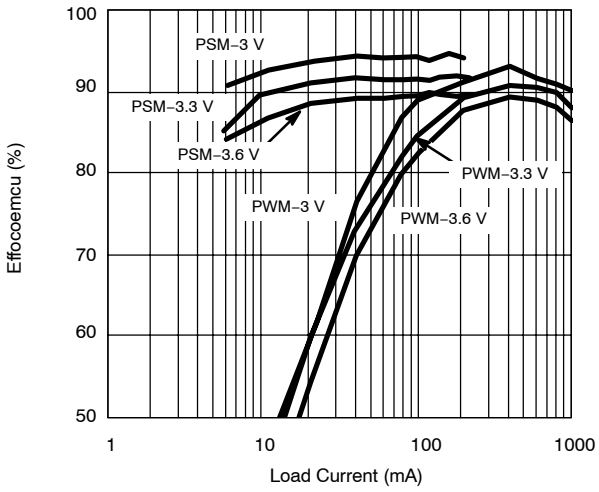
Frequency vs. Temperature



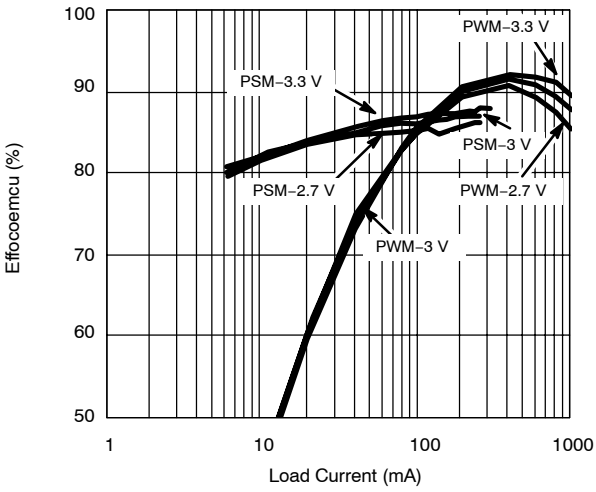
Frequency vs. R_{OSC}



Buck Mode Efficiency, V_O = 2.7 V



Boost Mode Efficiency, V_O = 3.6 V



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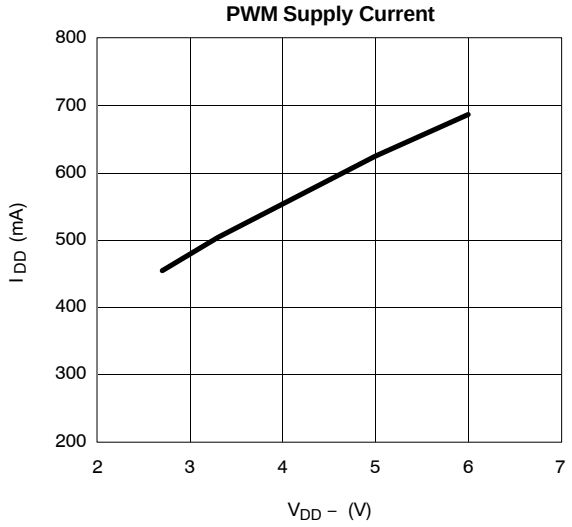
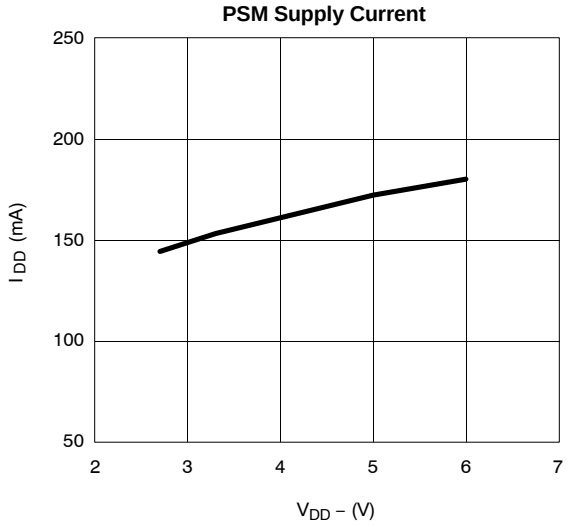
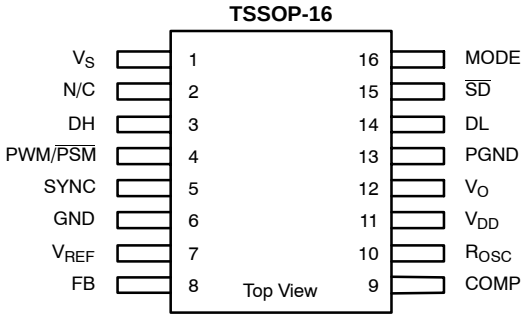
TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)





PIN CONFIGURATION



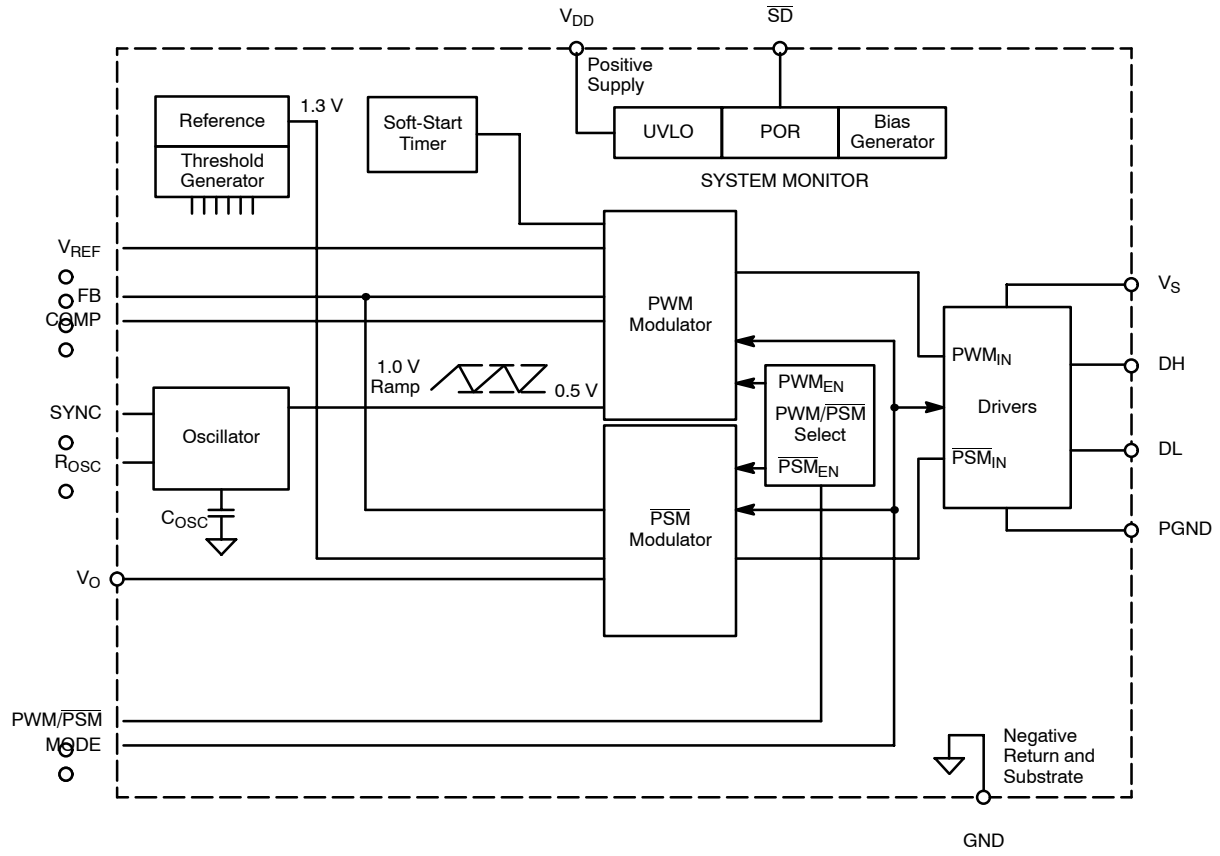
ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9166BQ-T1	–25 to 85°C	Tape and Reel
Si9166BQ-T1—E3		

Eval Kit	Temperature Range	Board Type
Si9166DB	–25 to 85°C	Surface Mount

PIN DESCRIPTION

Pin	Symbol	Description
1	V_S	Input supply voltage for the output driver section. Input voltage range is 2.7 V to 6V
2	N/C	Not Used
3	DH	The gate drive output for the high-side p-channel MOSFET. The p-channel MOSFET is the main switch for buck topology and the synchronous rectifier for the boost topology.
4	PWM/$\overline{PSM}$	Logic high = PWM mode, logic low = PSM mode. In PSM mode, synchronous rectification is disabled.
5	SYNC	Externally controlled synchronization signal. Logic high to low transition forces the clock synchronization. If not used, the pin must be connected to V_{DD}, or logic high.
6	GND	Low power controller ground
7	V_{REF}	1.3-V reference. Decoupled with 0.1-µF capacitor
8	FB	Output voltage feedback connected to the inverting input of an error amplifier.
9	COMP	Error amplifier output for external compensation network.
10	R_{OSC}	External resistor to determine the switching frequency.
11	V_{DD}	Input supply voltage for the analog circuit. Input voltage range is 2.7 V to 6 V.
12	V_O	Direct output voltage sense
13	PGND	Power ground for output drive stage
14	DL	The gate drive output for the low-side n-channel MOSFET. The n-channel MOSFET is the synchronous rectifier for the buck topology and the main switch for the boost topology.
15	$\overline{SD}$	Shuts down the IC completely and decreases current consumed by the IC to < 1 µA.
16	MODE	Determines the converter topology. Connect to AGND for Buck or V_{DD} for Boost.

FUNCTIONAL BLOCK DIAGRAM



DETAIL OPERATIONAL DESCRIPTION

Start-Up

The UVLO circuit prevents the controller output driver and oscillator circuit from turning on, if the voltage on V_{DD} pin is less than 2.5 V. With typical UVLO hysteresis of 0.1 V, controller is continuously powered on until the V_{DD} voltage drops below 2.4 V. This hysteresis prevents the converter from oscillating during the start-up phase and unintentionally locking up the system. Once the V_{DD} voltage exceeds the UVLO threshold, and with no other shutdown condition detected, an internal power-on-reset timer is activated while most circuitry, except the output driver, are turned on. After the POR time-out of about 1 ms, the internal soft-start capacitor is allowed to charge. When the soft-start capacitor voltage reaches 0.5 V, the PWM circuit is enabled. Thereafter, the constant current charging the soft-start capacitor will force the converter output voltage to rise gradually without overshooting. To prevent negative undershoot, the synchronous switch is tri-stated until the duty cycle reaches about 10%. See start-up timing diagram. In tri-state, the high-side p-channel MOSFET is turned off by pulling up the gate voltage (DH) to V_S potential. The low-side n-channel MOSFET is turned off by pulling down the gate voltage (DL) to PGND potential. Note that the Si9166 will always soft start in the PWM mode regardless of the voltage level on the PWM/$\overline{PSM}$ pin.

Shutdown

The Si9166 is designed to conserve battery life by decreasing current consumption of IC during normal operation as well as the shutdown mode. With logic low-level on the SD pin, current consumption of the Si9166 decreases to less than 1 μA by shutting off most of the circuits. The logic high enables the controller and starts up as described in Start-Up section above.

MODE Selection

The Si9166 can be programmed to operate as Buck or Boost converter. If the MODE pin is connected to AGND, it operates in buck mode. If the MODE pin is connected to V_{DD}, it operates in boost mode. The DH gate drive output is designed to drive high-side p-channel MOSFET, acting as the main switch in buck topology and the synchronous rectifier in boost topology. The DL gate drive output is designed to drive low-side n-channel MOSFET, acting as the synchronous rectifier in buck topology and the main switch in boost topology.

PWM Mode

With PWM/$\overline{\text{PSM}}$ mode pin in logic high condition, the Si9166 operates in constant frequency (PWM) mode. As the load and line varies, switching frequency remain constant. The switching frequency is programmed by the R_{OSC} value. In the PWM mode, the synchronous drive is always enabled, even when the output current reaches 0 A. Therefore, the converter always operates in continuous conduction mode (CCM) if a synchronous switch is used. In CCM, transfer function of the converter remains almost constant, providing fast transient response. If the converter operates in discontinuous conduction mode (DCM), overall loop gain decreases and transient response time can be ten times longer than if the converter remain in continuous current mode. This transient response time advantage can significantly decrease the hold-up capacitors needed on the output of dc/dc converter to meet the transient voltage regulation. The PWM/$\overline{\text{PSM}}$ pin is available to dynamically program the controller. If the synchronous rectifier switch is not used, the converter will operate in DCM at light load.

The maximum duty cycle of the Si9166 can reach 100% in buck mode. The duty cycle will continue to increase as the input voltage decreases until it reaches 100%. This allows the system designers to extract the maximum stored energy from the battery. Once the controller delivers 100% duty cycle, the converter operates like a saturated linear regulator. At 100% duty cycle, synchronous rectification is completely turned off. Up to 80% maximum duty cycle at 2-MHz switching frequency, the controller maintains perfect output voltage regulation. If the input voltage drops below the level where the converter requires greater than 80% duty cycle, the controller will deliver 100% duty cycle. This instantaneous jump in duty cycle is due to fixed BBM time, MOSFET delay/rise/fall time, and the internal propagational delays. In order to maintain regulation, controller might fluctuate its duty cycle back and forth from 100% to something lower than 80% while the converter is operating in this input voltage range. If the input voltage drops further, controller will remain on 100%. If the input voltage increases to a point where it's requiring less than 80% duty cycle, synchronous rectification is once again activated.

The maximum duty cycle under boost mode is internally limited to 70% to prevent inductor saturation. If the converter is turned on for 100% duty cycle, inductor never gets a chance to discharge its energy and eventually saturate. In boost mode, synchronous rectifier is always turned on for minimum or greater duration as long as the switch has been turned on. The controller will deliver 0% duty cycle, if the input voltage is greater than the programmed output voltage. Because of signal propagation time and MOSFET delay/rise/fall time, controller will not transition smoothly from minimum controllable duty cycle to 0% duty cycle. For example, controller may decrease its duty cycle from 5% to 0% abruptly, instead of gradual decrease you see from 70% to 5%.

Pulse Skipping Mode

The gate charge losses produced from the Miller capacitance of MOSFETs are the dominant power dissipation parameter during light load (i.e. < 10 mA). Therefore, less gate switching will improve overall converter efficiency. This is exactly why the Si9166 is designed with pulse skipping mode. If the PWM/$\overline{\text{PSM}}$ pin is connected to logic low level, converter operates in pulse skipping modulation (PSM) mode. During the pulse skipping mode, quiescent current of the controller is decreased to approximately 200 μA, instead of 500 μA during the PWM mode. This is accomplished by turning off most of internal control circuitry and utilizing a simple constant on-time control with feedback comparator. The controller is designed to have a constant on-time and a minimum off-time acting as the feedback comparator blanking time. If the output voltage drops below the desired level, the main switch is first turned on and then off. If the applied on-time is insufficient to provide the desired voltage, the controller will force another on and off sequence, until the desired voltage is accomplished. If the applied on-time forces the output to exceed the desired level, as typically found in the light load condition, the converter stays off. The excess energy is delivered to the output slowly, forcing the converter to skip pulses as needed to maintain regulation. The on-time and off-time are set internally based on inductor used (1.5-μH typical), MODE pin selection and maximum load current. Therefore, with this control method, duty cycle ranging from 0 to near 100% is possible depending on whether buck or boost is chosen. In pulse skipping mode, synchronous rectifier drive is also disabled to further decrease the gate charge loss and increase overall converter efficiency.

Reference

The reference voltage for the Si9166 is set at 1.3 V. The reference voltage is internally connected to the non-inverting inputs of the error amplifier. The reference pin requires 0.1-μF decoupling capacitor.

Error Amplifier

The error amplifier gain-bandwidth product and slew rate are critical parameters which determines the transient response of converter. The transient response is function of both small and large signal responses. The small signal response is determined by the feedback compensation network while the large signal is determined by the error amplifier dv/dt and the inductor di/dt slew rate. Besides the inductance value, error amplifier determines the converter response time. In order to minimize the response time, the Si9166 is designed with 2-MHz error amplifier gain-bandwidth product to generate the widest converter bandwidth and 3.5 V/μsec slew rate for ultra-fast large signal response.

Oscillator

The oscillator is designed to operate up to 2-MHz minimal. The 2-MHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. Even with 2-MHz switching frequency, quiescent current is only 500 μA with unique power saving circuit design. The switching frequency is easily programmed by attaching resistor to R_{OSC} pin. See oscillator frequency versus R_{OSC} curve to select the proper timing values for desired operating frequency. The tolerance on the operating frequency is (20% with 1% tolerance resistor).

Synchronization

The synchronization to external clock is easily accomplished by connecting the external clock into the SYNC pin. The logic high-to-low transition synchronizes the clock. The external clock frequency must be within 1.2 to 1.5 times the internal clock frequency.

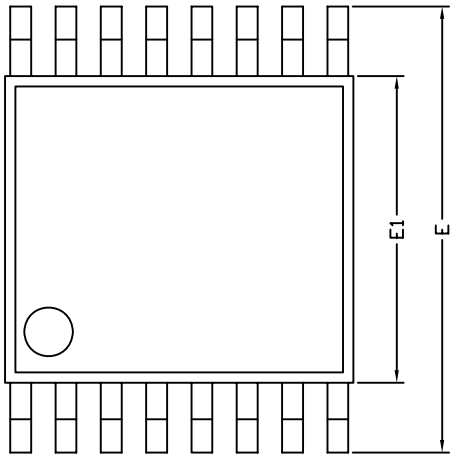
Break-Before-Make Timing

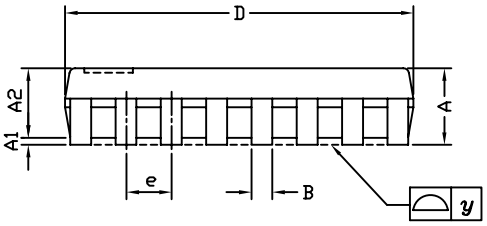
A proper BBM time is essential in order to prevent shoot-through current and to maintain high efficiency. The break-before-make time is set internally at 20 to 60 ns @ V_S = 3.6 V. The high- and low-side gate drive voltages are monitored and when the gate to source voltage reaches 1.75 V above or below the initial starting voltage, 20 to 60 ns BBM time is set before the other gate drive transitions to its proper state. The maximum and minimum duty cycle is limited by the BBM time. Since the BBM time is fixed, controllable maximum duty cycle will vary depending on the switching frequency.

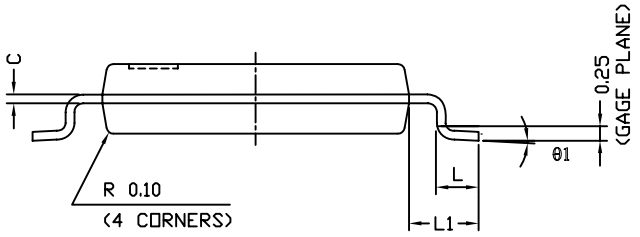
Output Driver Stage

The DH pin is designed to drive the high-side p-channel MOSFET, independent of topology. The DL pin is designed to drive the low-side n-channel MOSFET, independent of topology. The driver stage is sized to sink and source peak currents up to 450 mA with V_S = 3.3 V. The ringing from the gate drive output trace inductance can produce negative voltage on the DH and DL respect to PGND. The gate drive circuit is capable of withstanding these negative voltages without any functional defects.

TSSOP: 16-LEAD

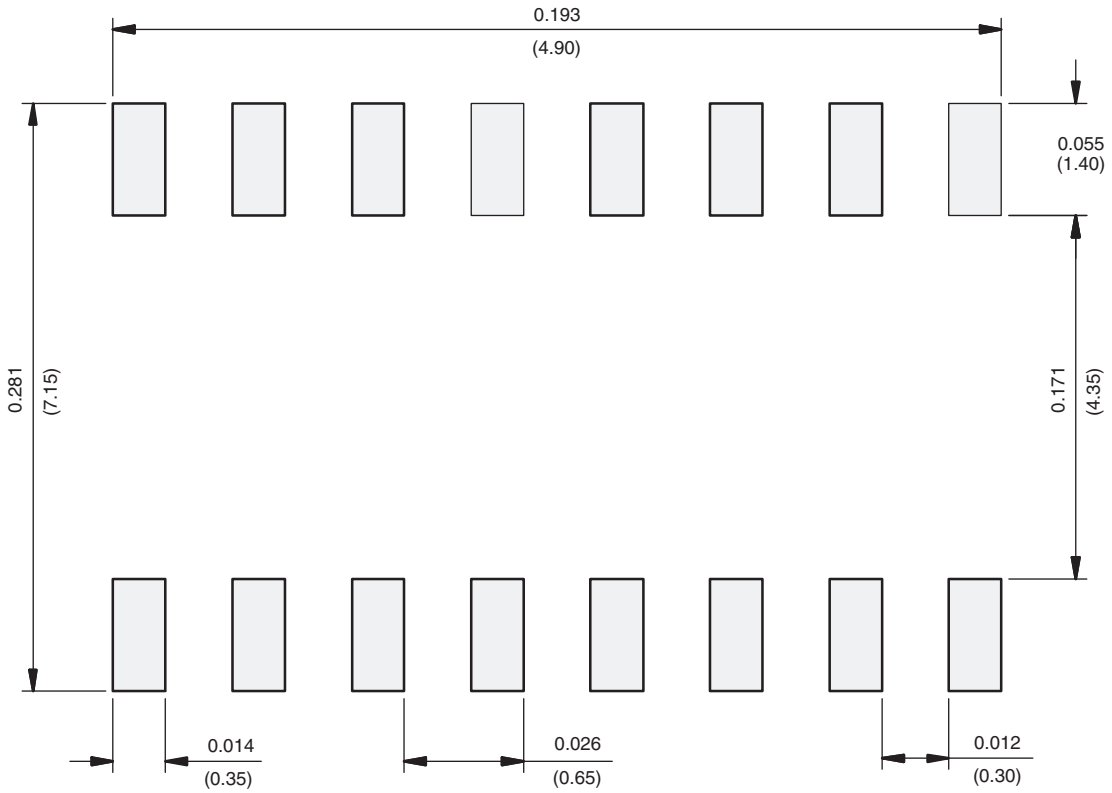






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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