

# High-Speed Quad Monolithic SPST CMOS Analog Switch

## DESCRIPTION

The DG271B high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

Built on the Vishay Siliconix' proprietary high voltage silicon gate process to achieve superior on/off performance, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latchup.

The DG271B has a redesign internal regulator which improves start-up over the DG271.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

## FEATURES

- Fast switching  $t_{ON}$ : 55 ns
- Low charge injection: 5 pC
- Low  $r_{DS(on)}$ : 32  $\Omega$
- TTL/CMOS compatible
- Low leakage: 50 pA

## BENEFITS

- Fast settling times
- Reduced switching glitches
- High precision

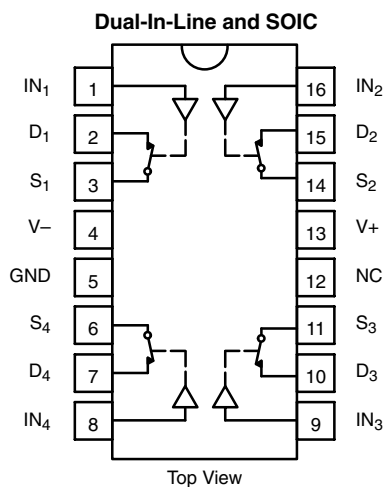
## APPLICATIONS

- High-speed switching
- Sample/hold
- Digital filters
- Op amp gain switching
- Flight control systems
- Automatic test equipment
- Choppers
- Communication systems



Available  
**RoHS\***  
COMPLIANT

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### TRUTH TABLE

Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

\* Pb containing terminations are not RoHS compliant, exemptions may apply.



ORDERING INFORMATION		
Temp. Range	Package	Part Number
0 °C to 70 °C	16-Pin Plastic DIP	DG271BCJ-E3
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG271BDY-E3
		DG271BDY-T1-E3 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ °C}$ , unless otherwise noted			
Parameter	Limit	Unit	
V+ to V-	44	V	
GND to V-	25		
Digital Inputs <sup>a</sup> $V_S, V_D$	(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first		
Current, Any Terminal	30	mA	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)	100		
Storage Temperature	(DY Suffix)	- 65 to 150	°C
	(CJ Suffix)	- 65 to 125	
Power Dissipation (Package) <sup>b</sup>	16-Pin Plastic DIP <sup>c</sup>	470	mW
	16-Pin Plastic Narrow SOIC <sup>d</sup>	600	

Notes:

- a. Signals on  $S_X, D_X,$  or  $IN_X$  exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.



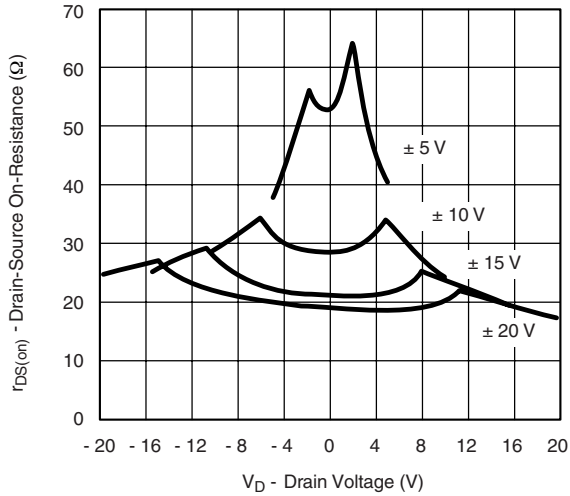
<b>SPECIFICATIONS <sup>a</sup></b>							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$	Temp. <sup>a</sup>	C, D Suffix 0 °C to 70 °C - 40 °C to 85 °C			Unit
				Min. <sup>d</sup>	Typ. <sup>c</sup>	Max. <sup>d</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full	- 15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = 1\text{ mA}$ , $V_D = \pm 10\text{ V}$	Room Full		32	50 75	$\Omega$
Switch Off Leakage Current	$I_{S(off)}$	$V_D = \pm 14\text{ V}$ , $V_S = \pm 14\text{ V}$	Room Full	- 1 - 20	$\pm 0.05$	1 20	nA
	$I_{D(off)}$		Room Full	- 1 - 20	$\pm 0.05$	1 20	
Channel On Leakage Current	$I_{D(on)}^+$ $I_{S(on)}$	$V_S = V_D = 14\text{ V}$	Room Full	- 1 - 20	$\pm 0.05$	1 20	
<b>Digital Control</b>							
Input Current with Voltage High	$I_{INH}$	$V_{IN} = 2\text{ V}$	Full	- 1	0.010	1	$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Full	- 1	0.010	1	
Input Current with Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Full	- 1	0.010	1	
<b>Dynamic Characteristics</b>							
Turn-On Time	$t_{ON}$	$V_S = \pm 10\text{ V}$ See Figure 3	Room Full		55	65 80	ns
Turn-Off Time	$t_{OFF}$		Room Full		50	65 80	
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ , $V_{gen} = 0\text{ V}$ , $R_{gen} = 0\ \Omega$ See Figure 3	Room		- 5		pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $V_{IN} = 5\text{ V}$ $f = 1\text{ MHz}$	Room		8		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		8		
Channel On Capacitance	$C_{D(on)}$	$V_D = V_S = 0\text{ V}$ , $V_{IN} = 0\text{ V}$	Room		30		
Off-Isolation	OIRR	$C_L = 10\text{ pF}$ , $R_L = 1\text{ k}\Omega$ $f = 100\text{ kHz}$ , See Figures 4 and 5	Room		85		dB
Crosstalk	$X_{TALK}$		Room		100		
<b>Power Supply</b>							
Positive Supply Current	$I_+$	All Channels On or Off $V_{IN} = 5\text{ V}$ or $0\text{ V}$	Room Full		5.5	7.5 9	mA
Negative Supply Current	$I_-$		Room Full	- 6 - 8	- 3.4		

Notes :

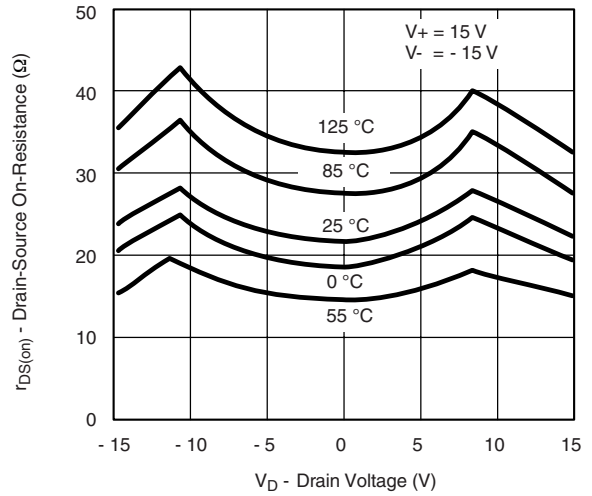
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

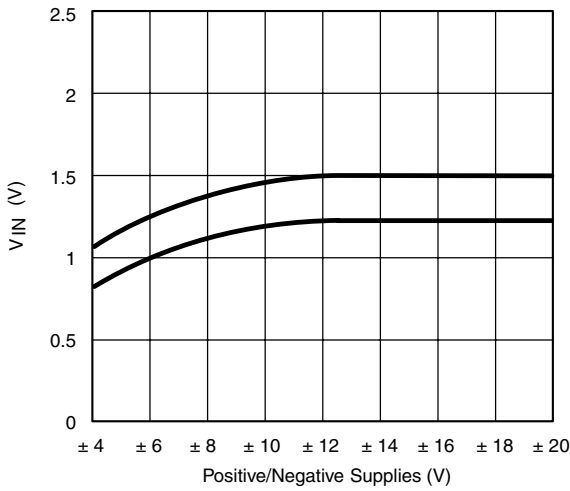
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



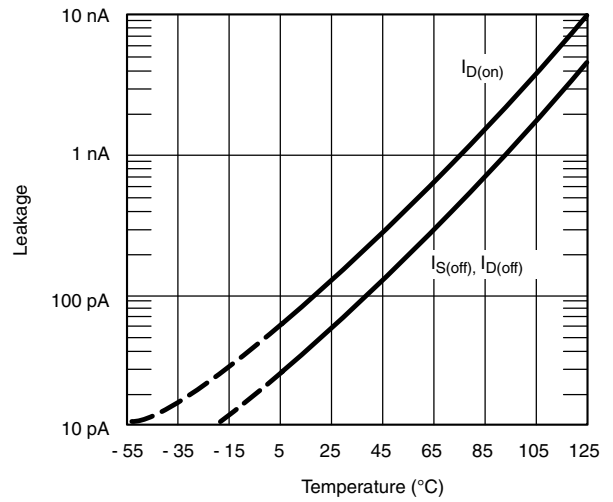
**$r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages**



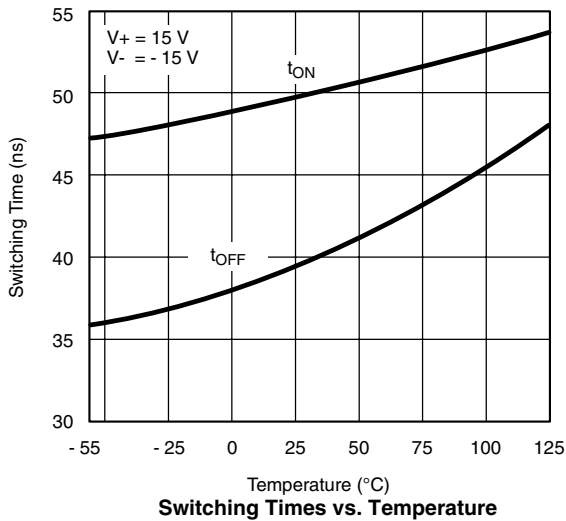
**$r_{DS(on)}$  vs.  $V_D$  and Temperature**



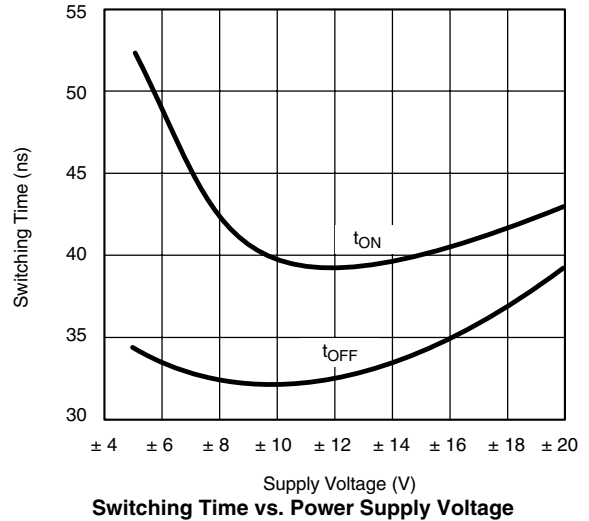
**Input Switching Threshold vs. Supply Voltage**



**Leakage Currents vs. Temperature**



**Switching Times vs. Temperature**



**Switching Time vs. Power Supply Voltage**

**SCHEMATIC DIAGRAM** Typical Channel

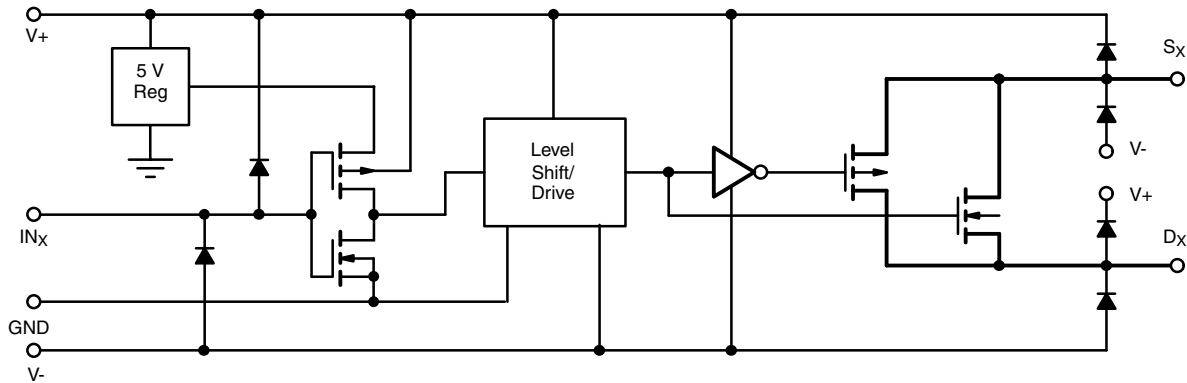


Figure 1.

**TEST CIRCUITS**

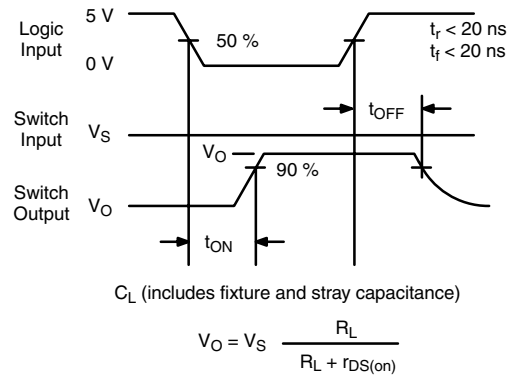
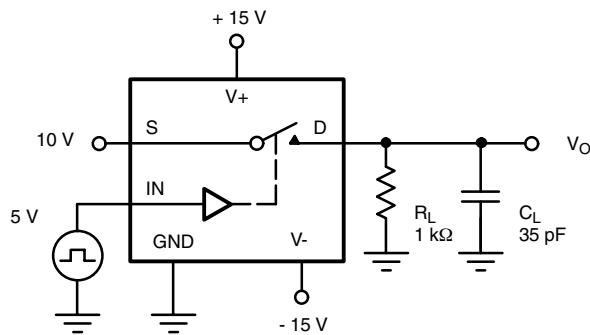


Figure 2. Switching Time

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70966>.

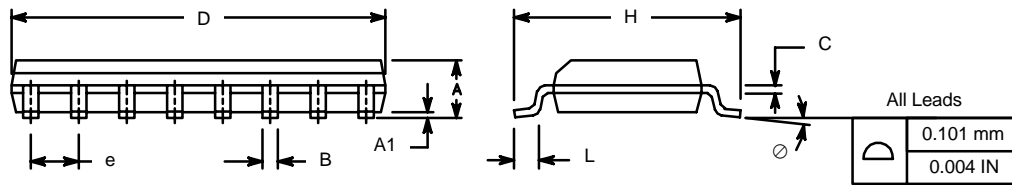


**SOIC (NARROW): 16-LEAD**  
JEDEC Part Number: MS-012

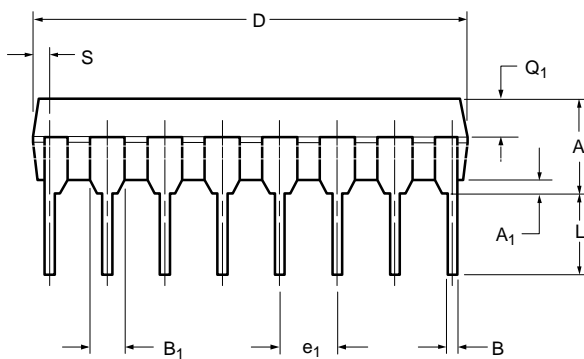


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5300



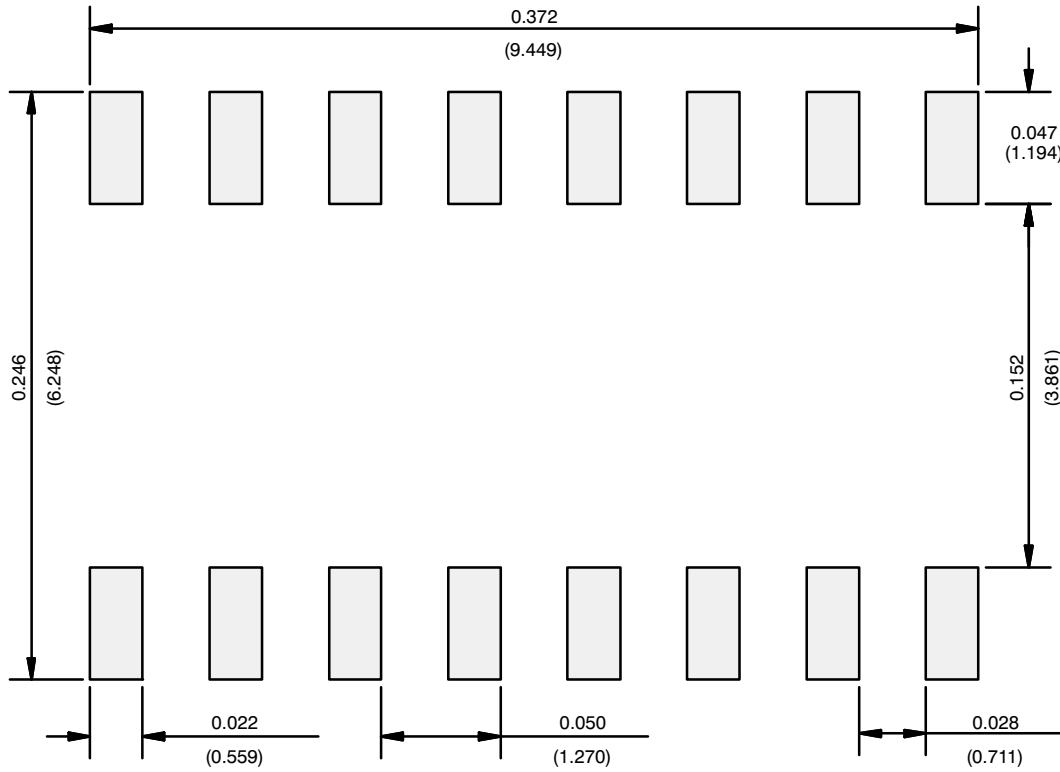
### PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	3.81	5.08	0.150	0.200
<b>A<sub>1</sub></b>	0.38	1.27	0.015	0.050
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	18.93	21.33	0.745	0.840
<b>E</b>	7.62	8.26	0.300	0.325
<b>E<sub>1</sub></b>	5.59	7.11	0.220	0.280
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	7.37	7.87	0.290	0.310
<b>L</b>	2.79	3.81	0.110	0.150
<b>Q<sub>1</sub></b>	1.27	2.03	0.050	0.080
<b>S</b>	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01  
DWG: 5482

## RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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