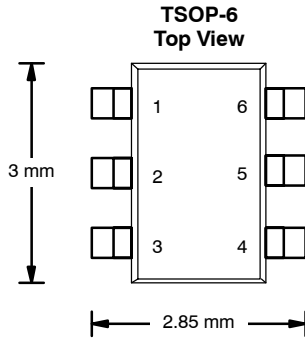


## N-Channel 200-V (D-S) MOSFET

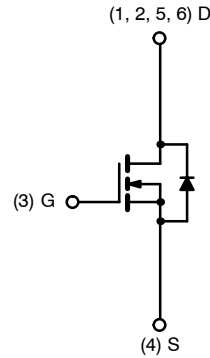
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
200	3.7 @ $V_{GS} = 10$ V	0.5

### FEATURES

- 100%  $R_g$  Tested



Ordering Information: Si3420DV-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	200		V
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	0.5	0.37	A
	$T_A = 70^\circ\text{C}$		0.4	0.29	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)		$I_{DM}$	1		
Avalanche Current		$I_{AS}$	1		mJ
Single Avalanche Energy		$E_{AS}$	0.05		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	1		A
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.1	1.14	W
	$T_A = 70^\circ\text{C}$		1.34	0.73	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ sec	$R_{thJA}$	50	60	$^\circ\text{C}/\text{W}$
	Steady State		90	110	
Maximum Junction-to-Foot	Steady State	$R_{thJF}$	35	42	

**Notes**

a. Surface Mounted on 1" x 1" FR4 Board.

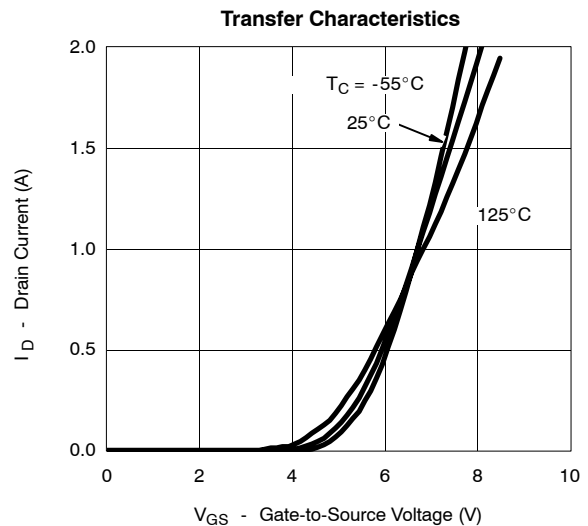
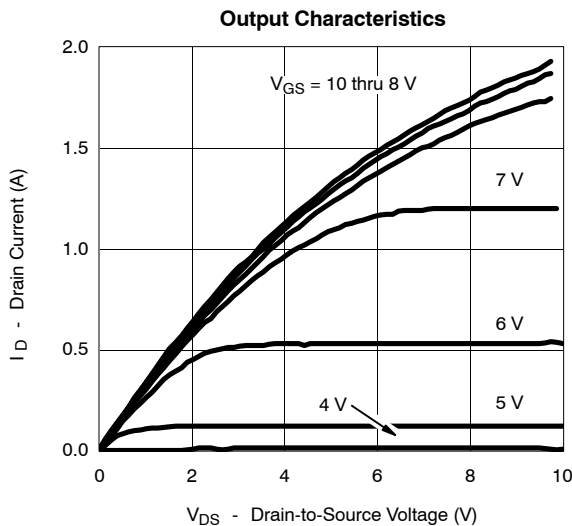


SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			25	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	1			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.35 A			3.7	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1 A		9		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0 V			1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.5 A		2.2	3.5	nC
Gate-Source Charge	Q <sub>gs</sub>		0.65			
Gate-Drain Charge	Q <sub>gd</sub>		0.95			
Gate Resistance	R <sub>g</sub>		0.5		2.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, R <sub>L</sub> = 100 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		7	12	ns
Rise Time	t <sub>r</sub>		8	13		
Turn-Off Delay Time	t <sub>d(off)</sub>		10	15		
Fall Time	t <sub>f</sub>		30	50		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 1 A, di/dt = 100 A/μs		140	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

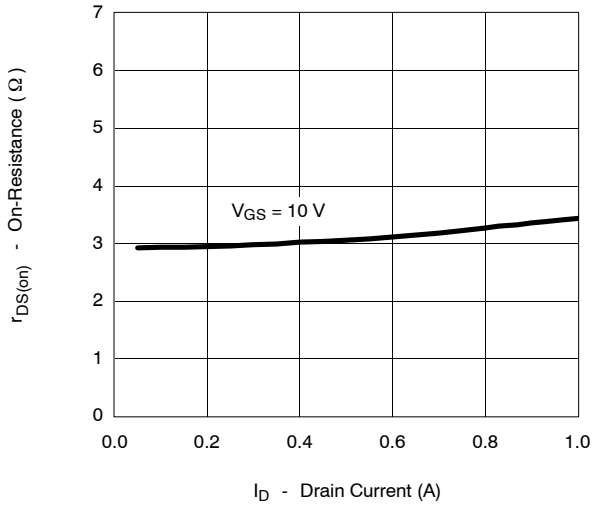
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



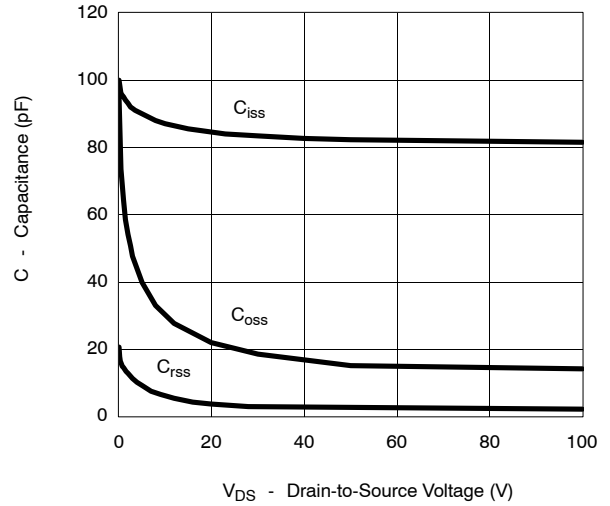


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

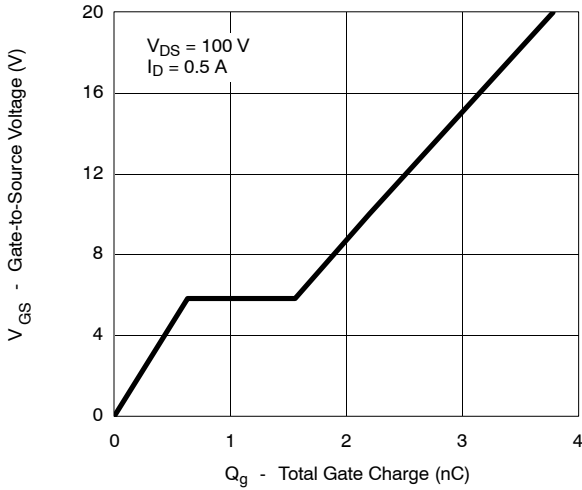
**On-Resistance vs. Drain Current**



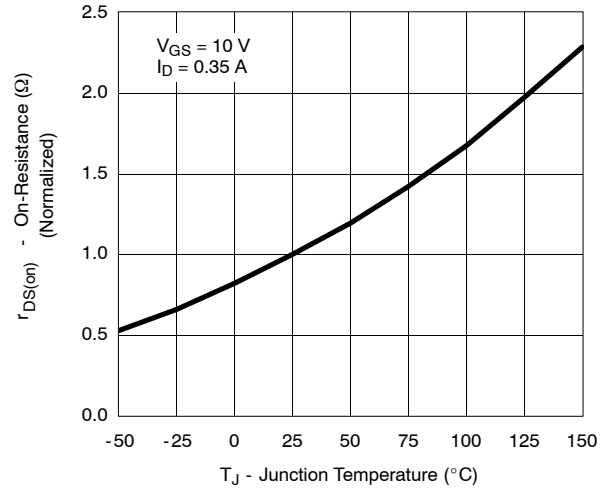
**Capacitance**



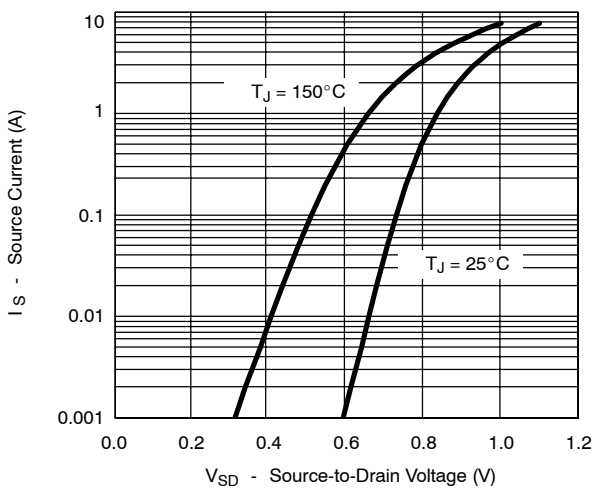
**Gate Charge**



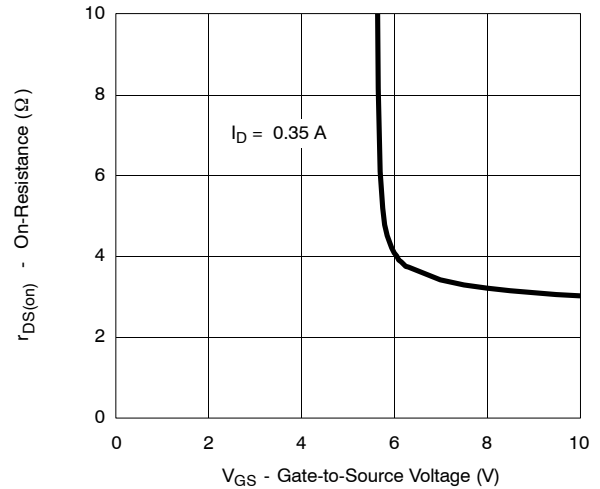
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

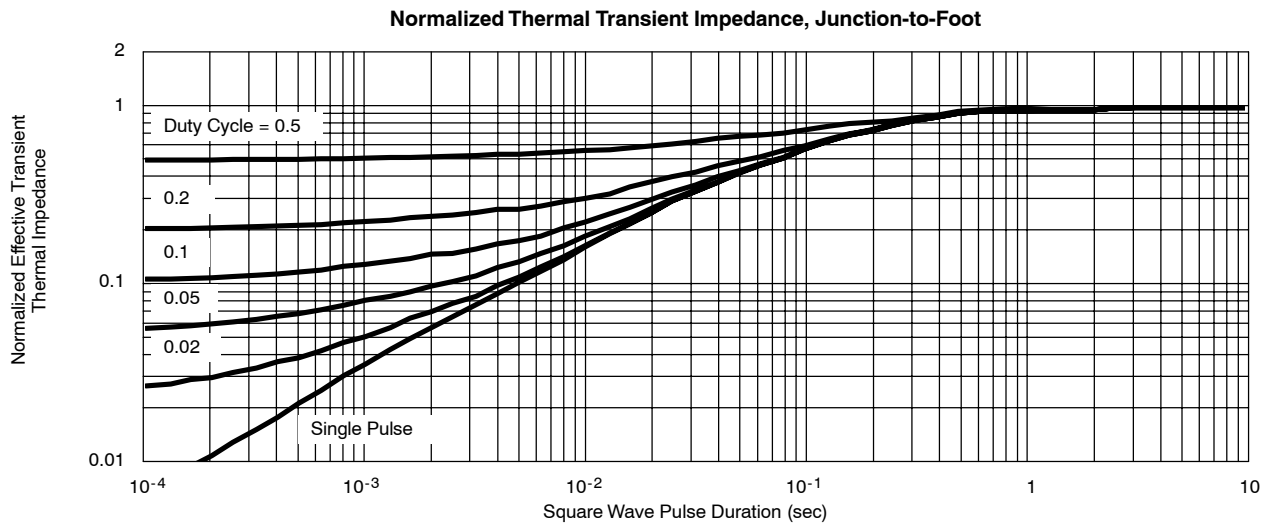
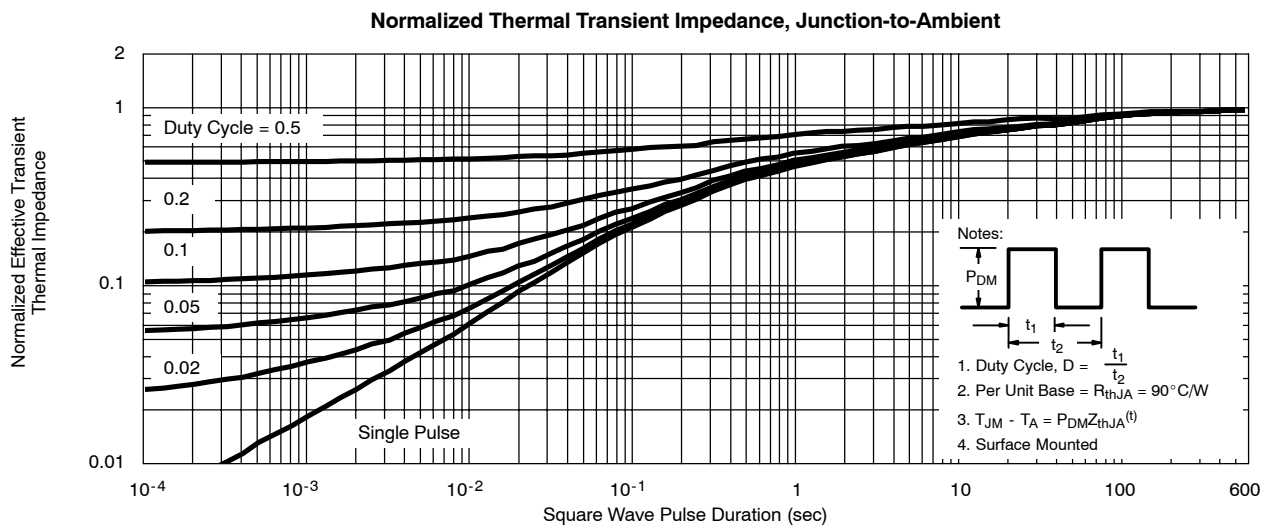
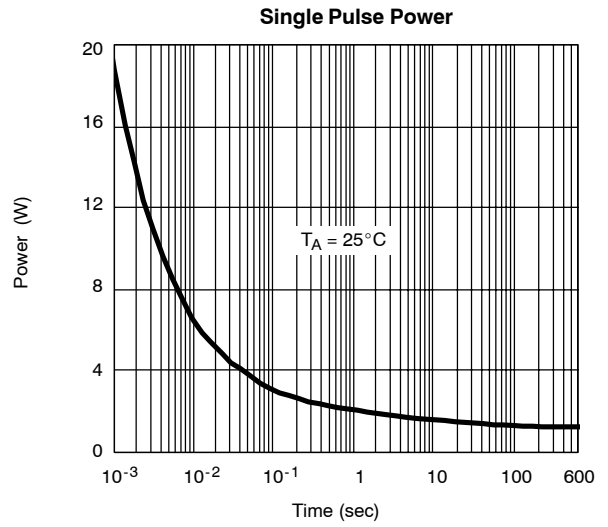
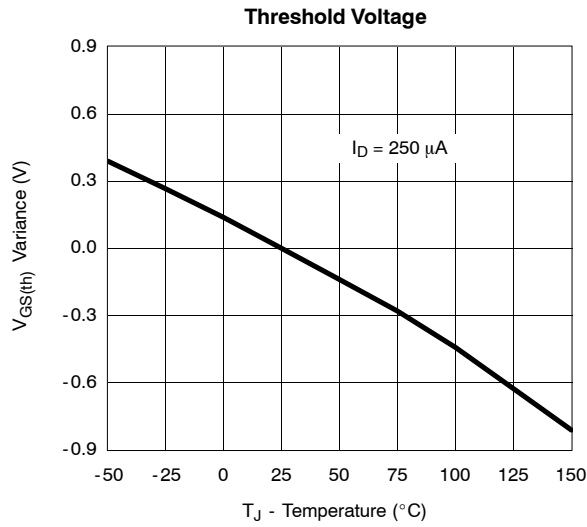


**On-Resistance vs. Gate-to-Source Voltage**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**





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