

Precision Monolithic Quad SPST Low-Voltage CMOS Analog Switches

DESCRIPTION

The DG441L, DG442L are low voltage pin-for-pin compatible companion devices to the industry standard DG441L, DG442L with improved performance.

Using BiCMOS wafer fabrication technology allows the DG441L, DG442L to operate on single and dual supplies. Single supply voltage ranges from 3 V to 12 V while dual supply operation is recommended with ± 3 V to ± 6 V.

Combining high speed (t_{ON} : 20 ns), flat $R_{DS(on)}$ over the analog signal range (5Ω), minimal insertion loss (-3 dB at 280 MHz), and excellent crosstalk and off-isolation performance (-50 dB at 50 MHz), the DG441L, DG442L are ideally suited for audio and video signal switching.

The DG441L, DG442L responds to opposite control logic as shown in the Truth Table open and two normally closed switches.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- 2.7 V thru 12 V single supply or ± 3 V thru ± 6 V dual supply
- On-resistance - $R_{DS(on)}$: 17Ω
- Fast switching - t_{ON} : 20 ns
- t_{OFF} : 12 ns
- TTL, CMOS compatible
- Low leakage: 0.25 nA
- 2000 V ESD protection
- **Compliant to RoHS Directive 2002/95/EC**



RoHS
COMPLIANT
HALOGEN
FREE

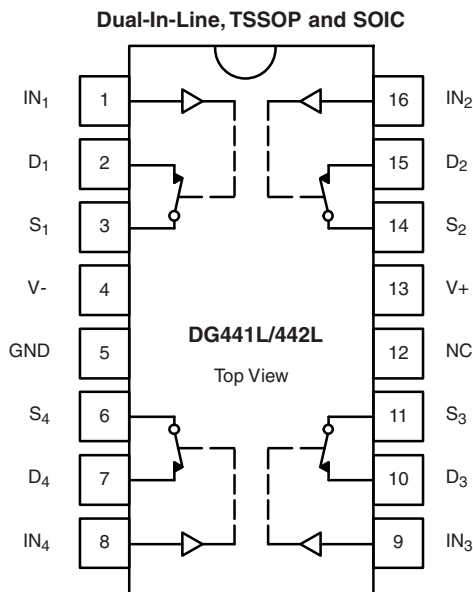
BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing

APPLICATIONS

- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals
- SDSL, DSLAM
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	DG441L	DG442L
0	On	Off
1	Off	On

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-pin TSSOP	DG441LDQ-T1-E3
		DG442LDQ-T1-E3
	16-pin narrow SOIC	DG441LDY-T1-E3 DG442LDY-T1-E3
- 55 °C to 125 °C	16-pin CerDIP	DG441LAK, DG441LAK/883 DG442LAK, DG442LAK/883
		LCC-20

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
V + to V -		- 0.3 to 13	V
GND to V - A		7	
Digital Inputs ^a V_S, V_D		GND - 0.3 to (V +) + 0.3 or 30 mA, whichever occurs first	
Continuous Current (any terminal)		30	mA
Current, S or D (pulsed 1 ms, 10 % duty cycle)		100	
Storage Temperature	(DQ, DY suffix)	- 65 to 125	°C
	(AK suffix)	- 65 to 150	
Power Dissipation (Packages) ^b	16-pin TSSOP ^c	450	mW
	16-pin narrow Body SOIC ^d	650	
	16-pin CerDIP ^e	900	

Notes:

- a. Signals on $S_X, D_X,$ or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 7 mW/°C above 75 °C
- d. Derate 7.6 mW/°C above 75 °C
- e. Derate 12 mW/°C above 75 °C.

SPECIFICATIONS^a (Single Supply 12 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp. ^b	Typ. ^c	A Suffix Limits - 55 °C to 125 °C		D Suffix Limits - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_+ = 10.8\text{ V}, V_- = 0\text{ V}$ $I_S = 10\text{ mA}, V_D = 2/9\text{ V}$	Room Full	20		30 45		30 40	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_S = 10\text{ mA}, V_D = 9\text{ V}$	Room	0.1		0.5		0.5	
Switch Off Leakage Current	$I_{S(off)}$	$V_D = 1/11\text{ V}, V_S = 11/1\text{ V}$	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	nA
	$I_{D(off)}$		Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Channel On Leakage Current	$I_{D(on)}$	$V_S = V_D = 11/1\text{ V}$	Room Full		- 1 - 15	1 15	- 1 - 10	1 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.01	- 1.5	1.5	- 1	1	μA
Input Current, V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V	Full		- 1.5	1.5	- 1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300\text{ } \Omega, C_L = 35\text{ pF}$ $V_S = 5\text{ V},$ see figure 2	Room Full	20		60 80		60 70	ns
Turn-Off Time	t_{OFF}		Room Full	12		35 50		35 45	
Charge Injection ^e	Q	$V_g = 0\text{ V}, R_g = 0\text{ } \Omega, C_L = 10\text{ nF}$	Room	5					pC
Off Isolation ^e	OIRR	$R_L = 50\text{ } \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room	71					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	95					
Source Off Capacitance ^e	$C_{S(off)}$	f = 1 MHz	Room	5					pF
Drain Off Capacitance ^e	$C_{D(off)}$		Room	6					
Channel On Capacitance ^e	$C_{D(on)}$		Room	15					
Power Supplies									
Positive Supply Current	I+	$V_{IN} = 0\text{ V or }12\text{ V}$	Full	0.03		1.5		1	μA
Negative Supply Current	I-		Room Full	- 0.002	- 1 - 7.5		- 1 - 5		
Ground Current	I_{GND}		Full	- 0.002	- 1.5		- 1		



SPECIFICATIONS^a (Dual Supply ± 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = +5$ V, $V_- = -5$ V $V_{IN} = 2.4$ V, 0.8 V ^f	Temp. ^b	Typ. ^c	A Suffix Limits -55 °C to 125 °C		D Suffix Limits -40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		-5	5	-5	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_+ = +5$ V, $V_- = -5$ V $I_S = 10$ mA, $V_D = \pm 3.5$ V	Room Full	20		33 45		33 40	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_S = 10$ mA, $V_D = \pm 3.5$ V	Room	0.1		0.5		0.5	
Switch Off Leakage Current ^g	$I_{S(off)}$	$V_+ = +5.5$ V, $V_- = -5.5$ V $V_D = \pm 4.5$ V, $V_S = \pm 4.5$ V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^g	$I_{D(on)}$	$V_+ = +5.5$ V, $V_- = -5.5$ V $V_S = V_D = \pm 4.5$ V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V_{IN} Low ^e	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.05	-1.5	1.5	-1	1	μ A
Input Current, V_{IN} High ^e	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.05	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300$ Ω , $C_L = 35$ pF $V_S = \pm 3.5$ V, see figure 2	Room Full	21		60 83		60 70	ns
Turn-Off Time	t_{OFF}		Room Full	16		35 55		35 45	
Charge Injection ^e	Q	$V_g = 0$ V, $R_g = 0$ Ω , $C_L = 10$ nF	Room	5					pC
Off Isolation ^e	OIRR	$R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz	Room	68					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	85					
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1$ MHz	Room	9					pF
Drain Off Capacitance ^e	$C_{D(off)}$		Room	9					
Channel On Capacitance ^e	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current ^e	I_+	$V_{IN} = 0$ V or 5 V	Full	0.002		1.5		1	μ A
Negative Supply Current ^e	-		Room Full	-0.002	-1 -7.5		-1 -5		
Ground Current ^e	I_{GND}		Full	-0.002	-1.5		-1		

SPECIFICATIONS^a (Single Supply 5 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}$, $V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}$, 0.8 V^f	Temp. ^b	Typ. ^c	A Suffix Limits - 55 °C to 125 °C		D Suffix Limits - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full			5		5	V
Drain-Source On-Resistance ^e	$R_{DS(on)}$	$V_+ = 4.5\text{ V}$ $I_S = 5\text{ mA}$, $V_D = 1\text{ V}$, 3.5 V	Room Full	35		50 88		50 75	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_S = 10\text{ mA}$, $V_D = 3.5\text{ V}$	Room	0.5		1		1	
Dynamic Characteristics									
Turn-On Time ^e	t_{ON}	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3.5\text{ V}$, see figure 2	Room Hot	27		50 90		50 60	ns
Turn-Off Time ^e	t_{OFF}		Room Hot	15		30 55		30 40	
Charge Injection ^e	Q	$V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 10\text{ nF}$	Room	0.5					pC
Power Supplies									
Positive Supply Current ^e	I +	$V_{IN} = 0\text{ V}$ or 5 V	Full	10		200		100	μA
Negative Supply Current ^e	I -		Room Full	- 0.002		- 1 - 7.5		- 1 - 5	
Ground Current ^e	I_{GND}		Full	- 10		- 200		- 100	



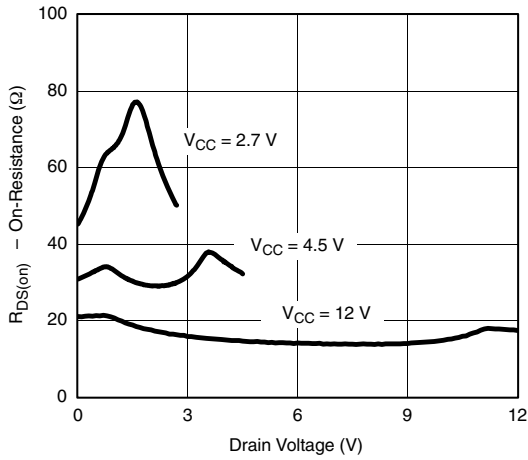
SPECIFICATIONS ^a (Single Supply 3 V)									
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 0.4\text{ V}^f$	Temp. ^b	Typ. ^c	A Suffix Limits -55 °C to 125 °C		D Suffix Limits -40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_+ = 2.7\text{ V}, V_- = 0\text{ V}$ $I_S = 5\text{ mA}, V_D = 0.5, 2.2\text{ V}$	Room Full	65		80 115		80 100	Ω
On-Resistance Match Between Channels ^e	$\Delta R_{DS(on)}$	$I_S = 5\text{ mA}, V_D = 2.2\text{ V}$	Room	1		3		3	
Switch Off Leakage Current ^g	$I_{S(off)}$	$V_+ = 3.3, V_- = 0\text{ V}$ $V_D = 1, 2\text{ V}, V_S = 2, 1\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^g	$I_{D(on)}$	$V_+ = 3.3\text{ V}, V_- = 0\text{ V}$ $V_S = V_D = 1, 2\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V_{IN} Low ^e	I_{IL}	V_{IN} under test = 0.4 V	Full	0.005	-1.5	1.5	-1	1	μA
Input Current, V_{IN} High ^e	I_{IH}	V_{IN} under test = 2.4 V	Full	0.005	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, see figure 2	Room Full	50		136 175		136 151	ns
Turn-Off Time	t_{OFF}		Room Full	30		100 140		100 125	
Charge Injection ^e	Q	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$	Room	1					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room	68					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	85					
Source Off Capacitance ^e	$C_{S(off)}$	f = 1 MHz	Room	6					pF
Drain Off Capacitance ^e	$C_{D(off)}$		Room	6					
Channel On Capacitance ^e	$C_{D(on)}$		Room	20					

Notes:

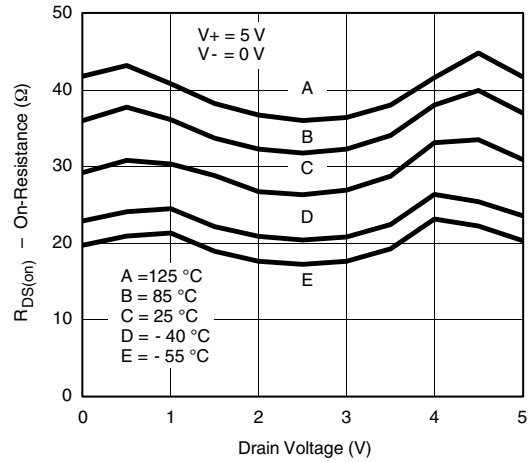
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

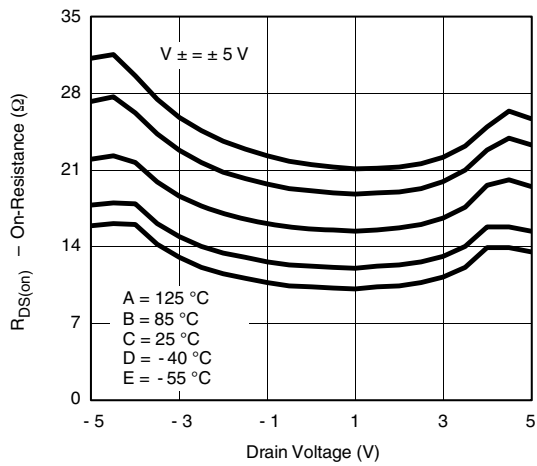
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



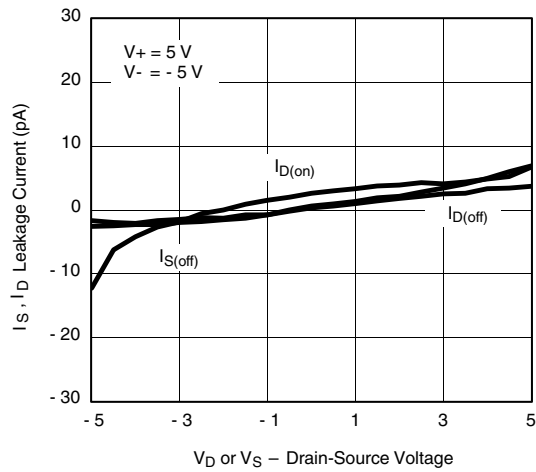
$R_{DS(on)}$ vs. Drain Voltage (Single Supply)



$R_{DS(on)}$ vs. Drain Voltage and Temperature (Single Supply)



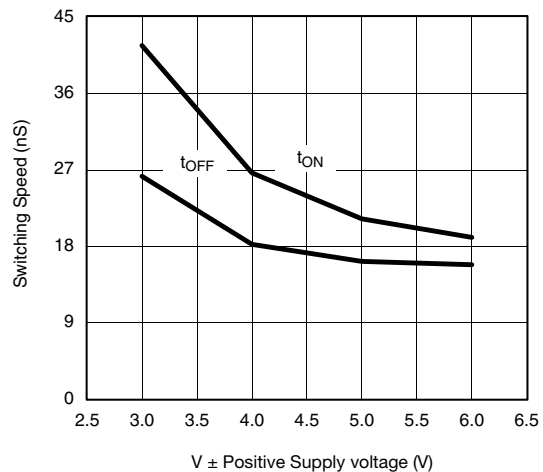
$R_{DS(on)}$ vs. Drain Voltage and Temperature (Dual Supply)



Leakage Current vs. Analog Voltage (Dual Supply)

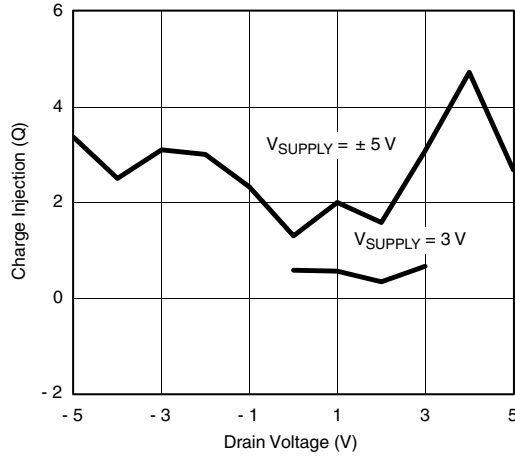


Switching Time vs. Single Supply

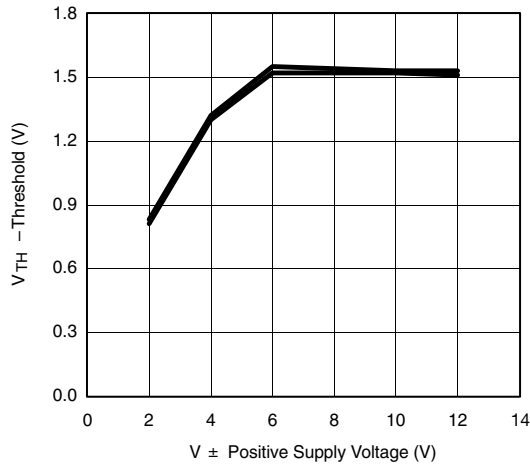


Switching Time vs. Dual Supply

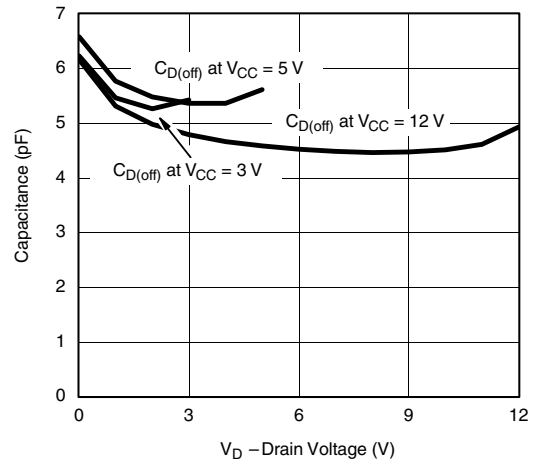
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



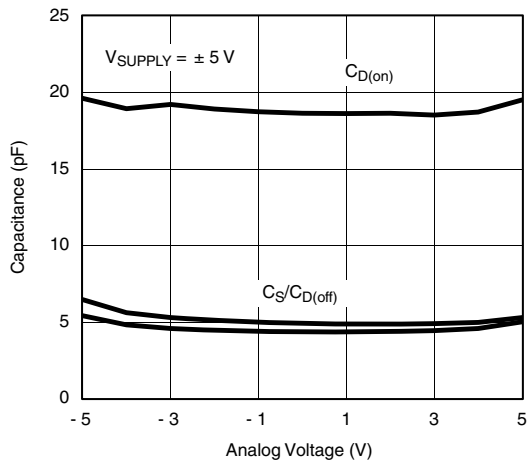
Charge Injection vs. Drain Voltage



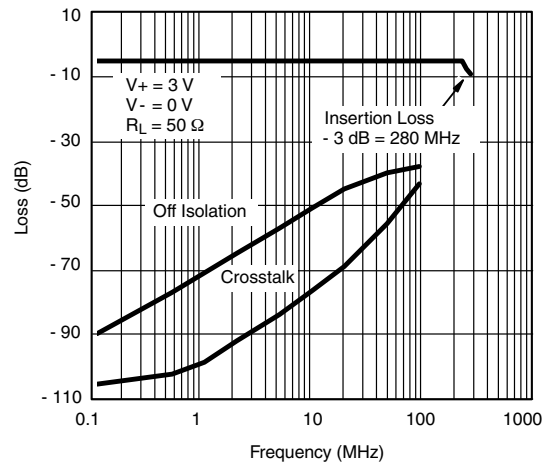
Input Threshold vs. Single Supply Voltage



Drain Capacitance vs. Drain Voltage (Single Supply)



Capacitance vs. Analog Signal (Dual Supply)



Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

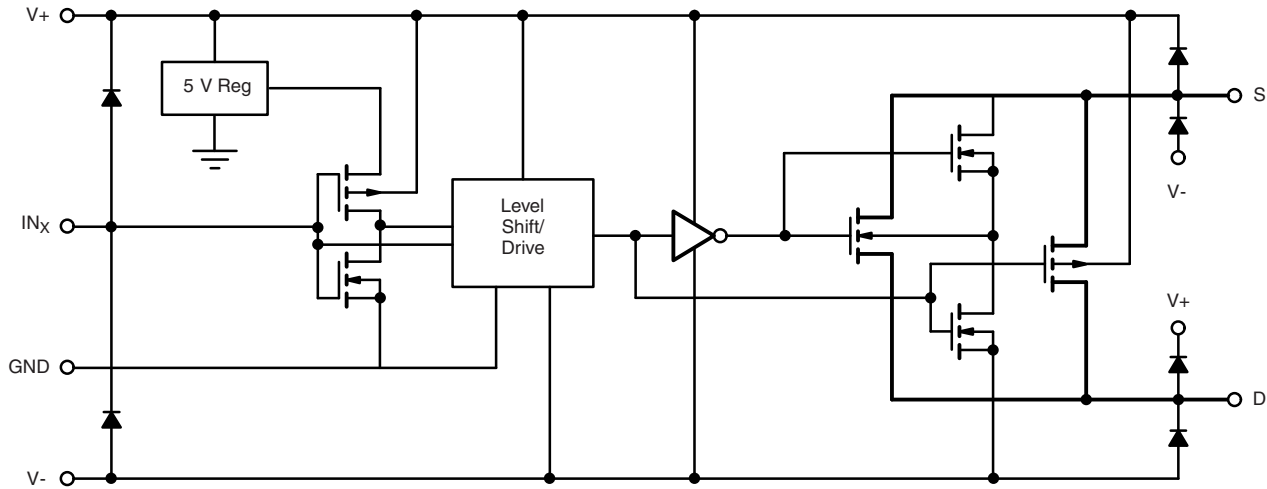
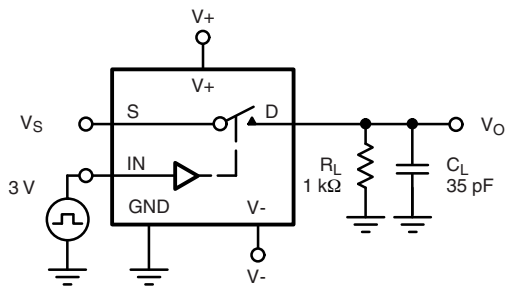
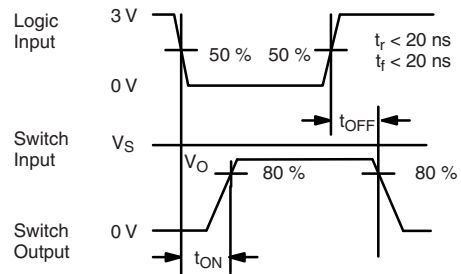


Figure 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

Figure 2. Switching Time

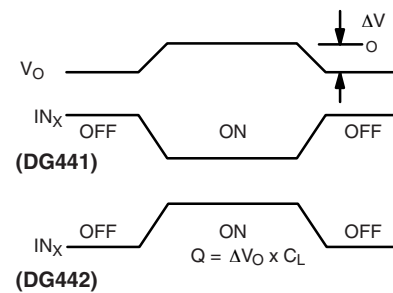
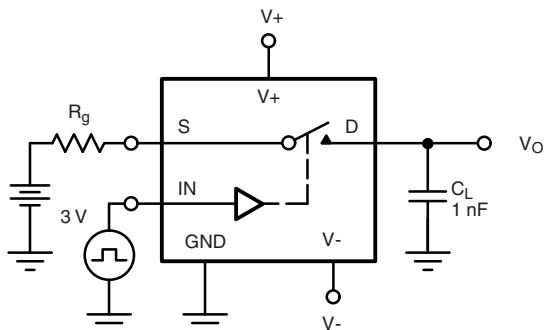


Figure 3. Charge Injection

TEST CIRCUITS

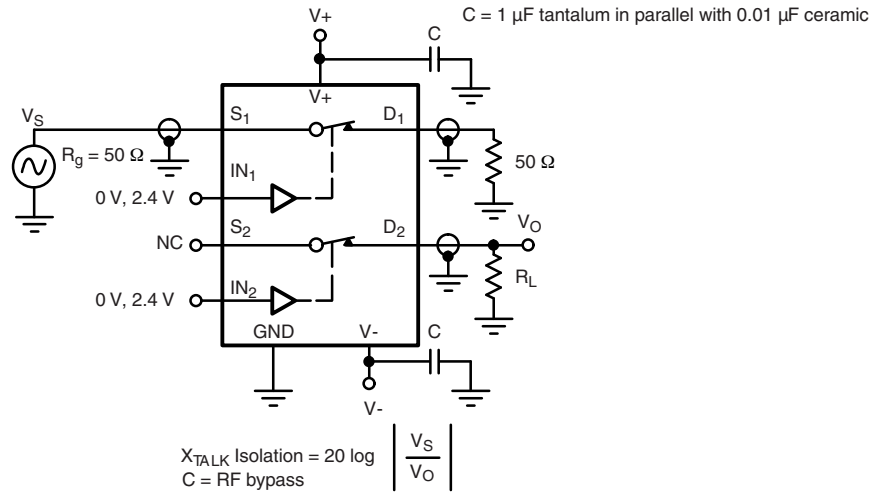


Figure 4. Crosstalk

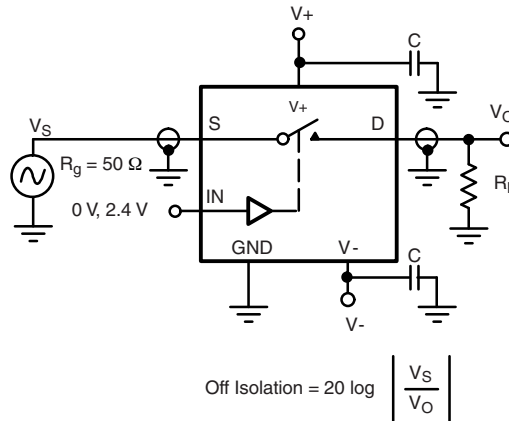


Figure 5. Off Isolation

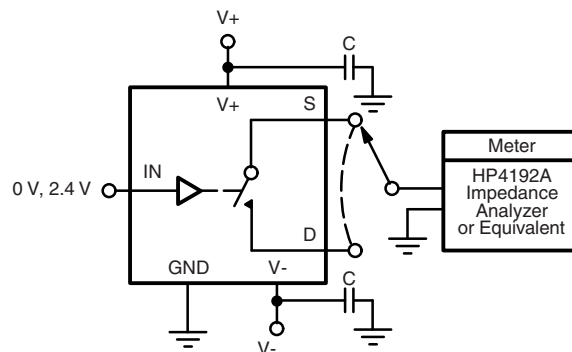


Figure 6. Source/Drain Capacitances

APPLICATIONS

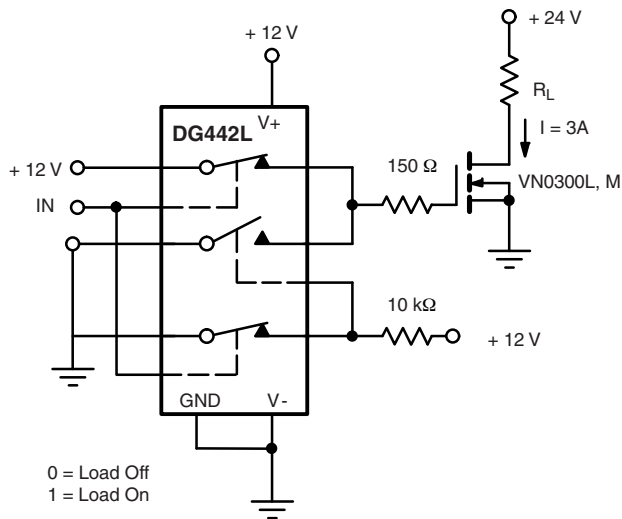


Figure 7. Power MOSFET Driver

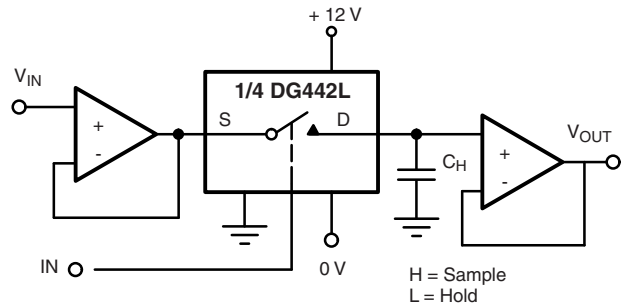


Figure 8. Open Loop Sample-and-Hold

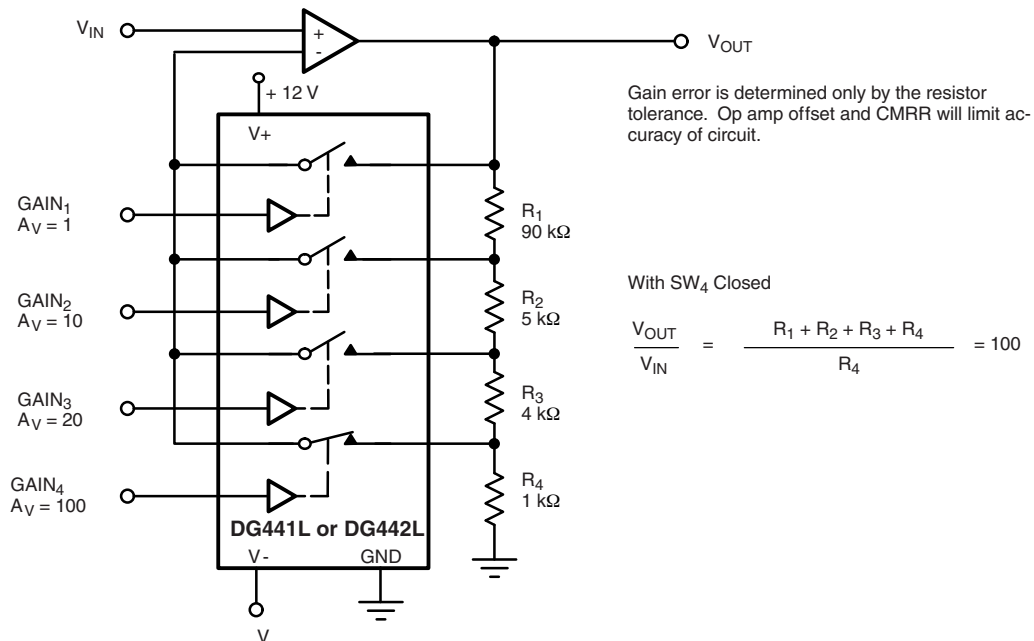


Figure 9. Precision-Weighted Resistor Programmable-Gain Amplifier

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71399.



SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624



RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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